Infineon Technologies - MB96F348RWCPQC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

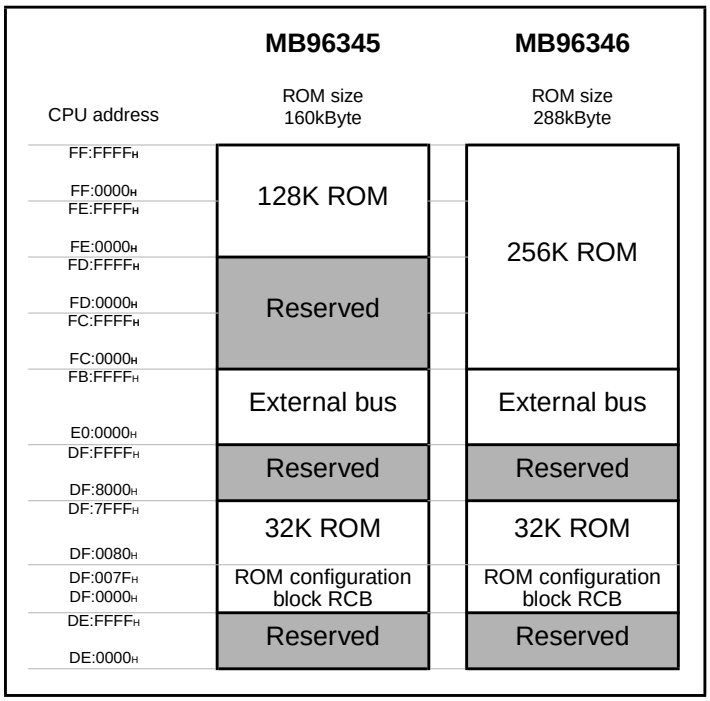
Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	80
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f348rwcpqc-gse2

■ PIN FUNCTION DESCRIPTION

Pin Function description (1 of 2)

Pin name	Feature	Description
ADn	External bus	External bus interface (multiplexed mode) address output and data input/output
ADTG	ADC	A/D converter trigger input
ADTG_R	ADC	Relocated A/D converter trigger input
ALARMn	Alarm comparator	Alarm Comparator n input
ALE	External bus	External bus Address Latch Enable output
An	External bus	External bus address output
ANn	ADC	A/D converter channel n input
AV_{CC}	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AVRH2	ADC	Alternative A/D converter high reference voltage input
AVRL	ADC	A/D converter low reference voltage input
AV_{SS}	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
ECLK	External bus	External bus clock output
CSn	External bus	External bus chip select n output
FRCKn	Free Running Timer	Free Running Timer n input
HAKX	External bus	External bus Hold Acknowledge
HRQ	External bus	External bus Hold Request
INn	ICU	Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
LBX	External bus	External Bus Interface Lower Byte select strobe output
MDn	Core	Input pins for specifying the operating mode.
NMI	External Interrupt	Non-Maskable Interrupt input
NMI_R	External Interrupt	Relocated Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output

■ USER ROM MEMORY MAP FOR MASK ROM DEVICES



I/O map MB96(F)34x (7 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000AB$_H$	PPG5 - Control status register High	PCNH5		R/W
0000AC$_H$	I2C0 - Bus Status Register	IBSR0		R
0000AD$_H$	I2C0 - Bus Control Register	IBCR0		R/W
0000AE$_H$	I2C0 - Ten bit Slave address Register Low	ITBAL0	ITBA0	R/W
0000AF$_H$	I2C0 - Ten bit Slave address Register High	ITBAH0		R/W
0000B0$_H$	I2C0 - Ten bit Address mask Register Low	ITMKL0	ITMK0	R/W
0000B1$_H$	I2C0 - Ten bit Address mask Register High	ITMKH0		R/W
0000B2$_H$	I2C0 - Seven bit Slave address Register	ISBA0		R/W
0000B3$_H$	I2C0 - Seven bit Address mask Register	ISMK0		R/W
0000B4$_H$	I2C0 - Data Register	IDAR0		R/W
0000B5$_H$	I2C0 - Clock Control Register	ICCR0		R/W
0000B6$_H$	I2C1 - Bus Status Register	IBSR1		R
0000B7$_H$	I2C1 - Bus Control Register	IBCR1		R/W
0000B8$_H$	I2C1 - Ten bit Slave address Register Low	ITBAL1	ITBA1	R/W
0000B9$_H$	I2C1 - Ten bit Slave address Register High	ITBAH1		R/W
0000BA$_H$	I2C1 - Ten bit Address mask Register Low	ITMKL1	ITMK1	R/W
0000BB$_H$	I2C1 - Ten bit Address mask Register High	ITMKH1		R/W
0000BC$_H$	I2C1 - Seven bit Slave address Register	ISBA1		R/W
0000BD$_H$	I2C1 - Seven bit Address mask Register	ISMK1		R/W
0000BE$_H$	I2C1 - Data Register	IDAR1		R/W
0000BF$_H$	I2C1 - Clock Control Register	ICCR1		R/W
0000C0$_H$	USART0 - Serial Mode Register	SMR0		R/W
0000C1$_H$	USART0 - Serial Control Register	SCR0		R/W
0000C2$_H$	USART0 - TX Register	TDR0		W
0000C2$_H$	USART0 - RX Register	RDR0		R
0000C3$_H$	USART0 - Serial Status	SSR0		R/W
0000C4$_H$	USART0 - Control/Com. Register	ECCR0		R/W
0000C5$_H$	USART0 - Ext. Status Register	ESCR0		R/W
0000C6$_H$	USART0 - Baud Rate Generator Register Low	BGRL0	BGR0	R/W
0000C7$_H$	USART0 - Baud Rate Generator Register High	BGRH0		R/W

I/O map MB96(F)34x (9 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000E3H	USART3 - Ext. Status Register	ESCR3		R/W
0000E4H	USART3 - Baud Rate Generator Register Low	BGRL3	BGR3	R/W
0000E5H	USART3 - Baud Rate Generator Register High	BGRH3		R/W
0000E6H	USART3 - Extended Serial Interrupt Register	ESIR3		R/W
0000E7H-0000EFH	Reserved			-
0000F0H-0000FFH	External Bus area	EXTBUS0		R/W
000100H	DMA0 - Buffer address pointer low byte	BAPL0		R/W
000101H	DMA0 - Buffer address pointer middle byte	BAPM0		R/W
000102H	DMA0 - Buffer address pointer high byte	BAPH0		R/W
000103H	DMA0 - DMA control register	DMACS0		R/W
000104H	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	R/W
000105H	DMA0 - I/O register address pointer high byte	IOAH0		R/W
000106H	DMA0 - Data counter low byte	DCTL0	DCT0	R/W
000107H	DMA0 - Data counter high byte	DCTH0		R/W
000108H	DMA1 - Buffer address pointer low byte	BAPL1		R/W
000109H	DMA1 - Buffer address pointer middle byte	BAPM1		R/W
00010AH	DMA1 - Buffer address pointer high byte	BAPH1		R/W
00010BH	DMA1 - DMA control register	DMACS1		R/W
00010CH	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	R/W
00010DH	DMA1 - I/O register address pointer high byte	IOAH1		R/W
00010EH	DMA1 - Data counter low byte	DCTL1	DCT1	R/W
00010FH	DMA1 - Data counter high byte	DCTH1		R/W
000110H	DMA2 - Buffer address pointer low byte	BAPL2		R/W
000111H	DMA2 - Buffer address pointer middle byte	BAPM2		R/W
000112H	DMA2 - Buffer address pointer high byte	BAPH2		R/W
000113H	DMA2 - DMA control register	DMACS2		R/W
000114H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W
000115H	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116H	DMA2 - Data counter low byte	DCTL2	DCT2	R/W

I/O map MB96(F)34x (24 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0006E4H	External Bus - Area configuration register 2 Low	EACL2	EAC2	R/W
0006E5H	External Bus - Area configuration register 2 High	EACH2		R/W
0006E6H	External Bus - Area configuration register 3 Low	EACL3	EAC3	R/W
0006E7H	External Bus - Area configuration register 3 High	EACH3		R/W
0006E8H	External Bus - Area configuration register 4 Low	EACL4	EAC4	R/W
0006E9H	External Bus - Area configuration register 4 High	EACH4		R/W
0006EAH	External Bus - Area configuration register 5 Low	EACL5	EAC5	R/W
0006EBH	External Bus - Area configuration register 5 High	EACH5		R/W
0006ECH	External Bus - Area select register 2	EAS2		R/W
0006EDH	External Bus - Area select register 3	EAS3		R/W
0006EEH	External Bus - Area select register 4	EAS4		R/W
0006EFH	External Bus - Area select register 5	EAS5		R/W
0006F0H	External Bus - Mode register	EBM		R/W
0006F1H	External Bus - Clock and Function register	EBCF		R/W
0006F2H	External Bus - Address output enable register 0	EBAE0		R/W
0006F3H	External Bus - Address output enable register 1	EBAE1		R/W
0006F4H	External Bus - Address output enable register 2	EBAE2		R/W
0006F5H	External Bus - Control signal register	EBCS		R/W
0006F6H-0006FFH	Reserved			-
000700H	CAN0 - Control register Low	CTRLRL0	CTRLR0	R/W
000701H	CAN0 - Control register High (reserved)	CTRLRH0		R
000702H	CAN0 - Status register Low	STATRL0	STATR0	R/W
000703H	CAN0 - Status register High (reserved)	STATRH0		R
000704H	CAN0 - Error Counter Low (Transmit)	ERRCNTL0	ERRCNT0	R
000705H	CAN0 - Error Counter High (Receive)	ERRCNTH0		R
000706H	CAN0 - Bit Timing Register Low	BTRL0	BTR0	R/W
000707H	CAN0 - Bit Timing Register High	BTRH0		R/W
000708H	CAN0 - Interrupt Register Low	INTRL0	INTR0	R
000709H	CAN0 - Interrupt Register High	INTRH0		R

I/O map MB96(F)34x (27 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000790H	CAN0 - New Data 1 Register Low	NEWDT1L0	NEWDT10	R
000791H	CAN0 - New Data 1 Register High	NEWDT1H0		R
000792H	CAN0 - New Data 2 Register Low	NEWDT2L0	NEWDT20	R
000793H	CAN0 - New Data 2 Register High	NEWDT2H0		R
000794H-00079FH	Reserved			-
0007A0H	CAN0 - Interrupt Pending 1 Register Low	INTPND1L0	INTPND10	R
0007A1H	CAN0 - Interrupt Pending 1 Register High	INTPND1H0		R
0007A2H	CAN0 - Interrupt Pending 2 Register Low	INTPND2L0	INTPND20	R
0007A3H	CAN0 - Interrupt Pending 2 Register High	INTPND2H0		R
0007A4H-0007AFH	Reserved			-
0007B0H	CAN0 - Message Valid 1 Register Low	MSGVAL1L0	MSGVAL10	R
0007B1H	CAN0 - Message Valid 1 Register High	MSGVAL1H0		R
0007B2H	CAN0 - Message Valid 2 Register Low	MSGVAL2L0	MSGVAL20	R
0007B3H	CAN0 - Message Valid 2 Register High	MSGVAL2H0		R
0007B4H-0007CDH	Reserved			-
0007CEH	CAN0 - Output enable register	COER0		R/W
0007CFH-0007FFH	Reserved			-
000800H	CAN1 - Control register Low	CTRLRL1	CTRLR1	R/W
000801H	CAN1 - Control register High (reserved)	CTRLRH1		R
000802H	CAN1 - Status register Low	STATRL1	STATR1	R/W
000803H	CAN1 - Status register High (reserved)	STATRH1		R
000804H	CAN1 - Error Counter Low (Transmit)	ERRCNTL1	ERRCNT1	R
000805H	CAN1 - Error Counter High (Receive)	ERRCNTH1		R
000806H	CAN1 - Bit Timing Register Low	BTRL1	BTR1	R/W
000807H	CAN1 - Bit Timing Register High	BTRH1		R/W
000808H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809H	CAN1 - Interrupt Register High	INTRH1		R

I/O map MB96(F)34x (29 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000840H	CAN1 - IF2 Command request register Low	IF2CREQL1	IF2CREQ1	R/W
000841H	CAN1 - IF2 Command request register High	IF2CREQH1		R/W
000842H	CAN1 - IF2 Command Mask register Low	IF2CMSKL1	IF2CMSK1	R/W
000843H	CAN1 - IF2 Command Mask register High (reserved)	IF2CMSKH1		R
000844H	CAN1 - IF2 Mask 1 Register Low	IF2MSK1L1	IF2MSK11	R/W
000845H	CAN1 - IF2 Mask 1 Register High	IF2MSK1H1		R/W
000846H	CAN1 - IF2 Mask 2 Register Low	IF2MSK2L1	IF2MSK21	R/W
000847H	CAN1 - IF2 Mask 2 Register High	IF2MSK2H1		R/W
000848H	CAN1 - IF2 Arbitration 1 Register Low	IF2ARB1L1	IF2ARB11	R/W
000849H	CAN1 - IF2 Arbitration 1 Register High	IF2ARB1H1		R/W
00084AH	CAN1 - IF2 Arbitration 2 Register Low	IF2ARB2L1	IF2ARB21	R/W
00084BH	CAN1 - IF2 Arbitration 2 Register High	IF2ARB2H1		R/W
00084CH	CAN1 - IF2 Message Control Register Low	IF2MCTRL1	IF2MCTR1	R/W
00084DH	CAN1 - IF2 Message Control Register High	IF2MCTRH1		R/W
00084EH	CAN1 - IF2 Data A1 Low	IF2DTA1L1	IF2DTA11	R/W
00084FH	CAN1 - IF2 Data A1 High	IF2DTA1H1		R/W
000850H	CAN1 - IF2 Data A2 Low	IF2DTA2L1	IF2DTA21	R/W
000851H	CAN1 - IF2 Data A2 High	IF2DTA2H1		R/W
000852H	CAN1 - IF2 Data B1 Low	IF2DTB1L1	IF2DTB11	R/W
000853H	CAN1 - IF2 Data B1 High	IF2DTB1H1		R/W
000854H	CAN1 - IF2 Data B2 Low	IF2DTB2L1	IF2DTB21	R/W
000855H	CAN1 - IF2 Data B2 High	IF2DTB2H1		R/W
000856H-00087FH	Reserved			-
000880H	CAN1 - Transmission Request 1 Register Low	TREQR1L1	TREQR11	R
000881H	CAN1 - Transmission Request 1 Register High	TREQR1H1		R
000882H	CAN1 - Transmission Request 2 Register Low	TREQR2L1	TREQR21	R
000883H	CAN1 - Transmission Request 2 Register High	TREQR2H1		R
000884H-00088FH	Reserved			-

■ HANDLING DEVICES

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Serial communication
- Handling of Data Flash

1. Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

2. Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.

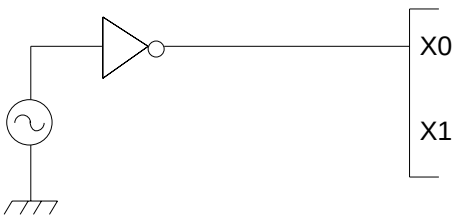
Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

3. External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

1. Single phase external clock

- When using a single phase external clock, X0 (X0A) pin must be driven and X1 (X1A) pin left open.



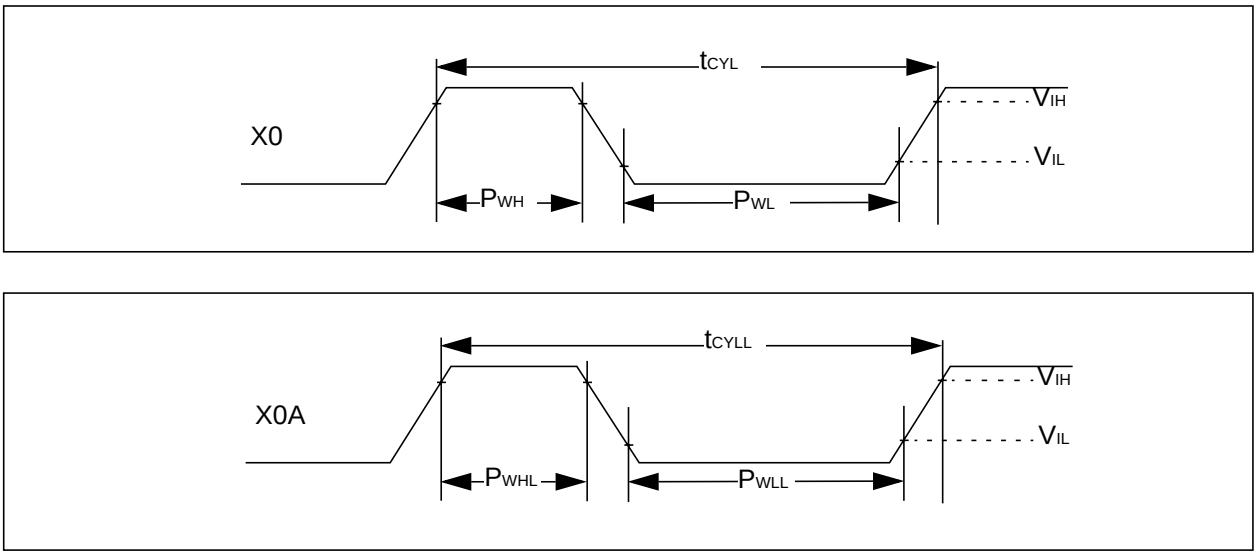
2. Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.0	-	5.5	V	
Smoothing capacitor at C pin	C_S	3.5	4.7	15	µF	Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.


tCYL
X0
VIH
VIL
PWH
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tCYLL
X0A
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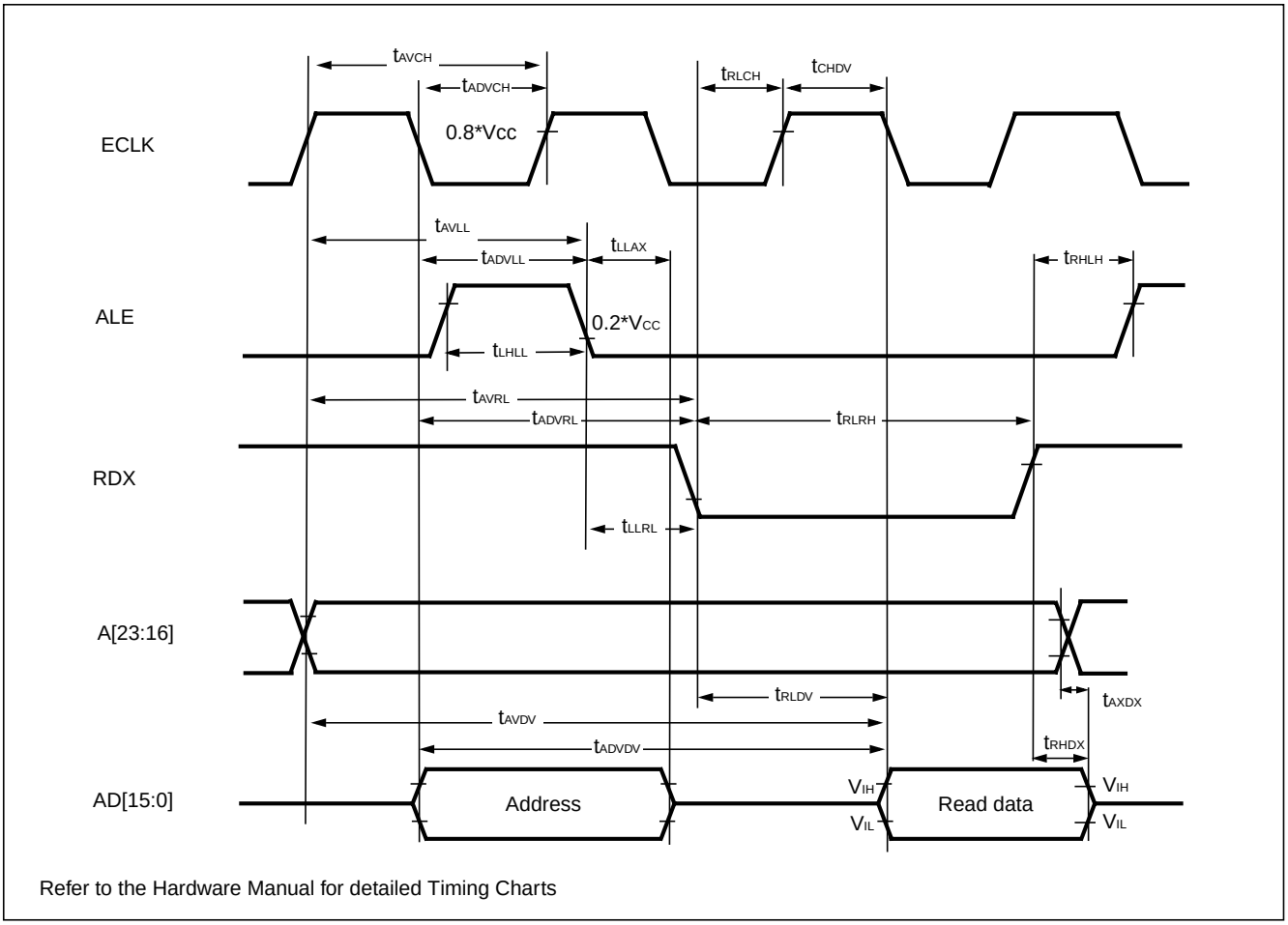
VIL
PWHL
PWLL



Refer to the Hardware Manual for detailed Timing Charts

Bus Timing (Write)

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2$ – 15	—	ns	
			EACL:ACE=1	$5t_{CYC}/2$ – 15	—		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	t_{CYC} – 15	—	ns	
			EACL:ACE=1	$2t_{CYC}$ – 15	—		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	—	t_{CYC} – 5	—	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	—	t_{CYC} – 20	—	ns	w/o cycle extension

I²C Timing

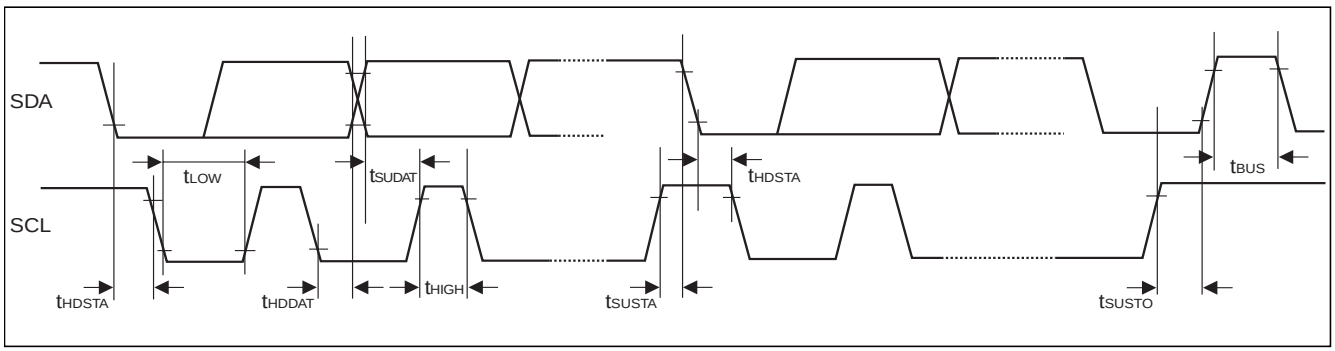
(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V,V_{SS} = AV_{SS} =0V)

Parameter	Symbol	Standard-mode		Fast-mode*1		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t_{HDSTA}	4.0	—	0.6	—	µs
“L” width of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
“H” width of the SCL clock	t_{HIGH}	4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL↑→SDA↓	t_{SUSTA}	4.7	—	0.6	—	µs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}	0	3.45	0	0.9	µs
Data set-up time SDA↓↑→SCL↑	t_{SUDAT}	250	—	100	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t_{SUSTO}	4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUS}	4.7	—	1.3	—	µs
Output fall time from 0.7*Vcc to 0.3*Vcc with a bus capacitance from 10 pF to 400 pF	t_{of}	20 + 0.1*C_b *2	250	20 + 0.1*C_b *2	250	ns
Capacitive load for each bus line	C_b	—	400	—	400	pF
Pulse width of spikes which will be suppressed by input noise filter	t_{SP}	n/a	n/a	0	1*t_{CLKP1}*3	ns

*1 : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.

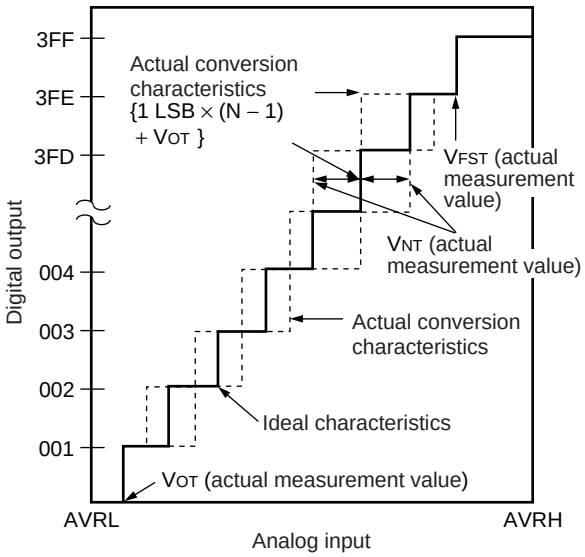
*2 : C_b = capacitance of one bus line in pF.

*3 : t_{CLKP1} is the cycle time of the periperal clock CLKP1.

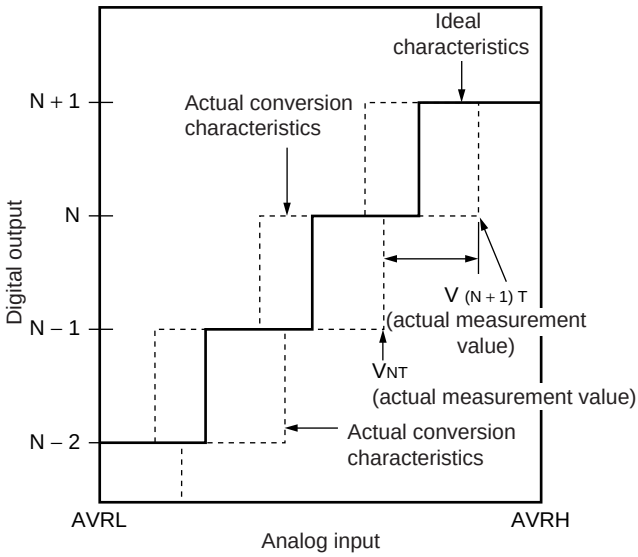


- V_{OH} = 0.7 * V_{CC}
- V_{OL} = 0.3 * V_{CC}
- CMOS Hysteresis 0.7/0.3 input selected

Nonlinearity error



Differential nonlinearity error



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times\ (N - 1)\ + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB [LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST} : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

6. Alarm Comparator

(T_A = -40 ˚C to +125 ˚C, V_{CC} = AV_{CC} = 3.0V - 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	AV_{CC}	-	25	45	µA	Alarm comparator enabled in fast mode (one channel)
	I_{A5ALMS}		-	7	13	µA	Alarm comparator enabled in slow mode (one channel)
	I_{A5ALMH}		-	-	5	µA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM0, ALARM1	-1	-	+1	µA	T_A = 25 ˚C
			-3	-	+3	µA	T_A = 125 ˚C
ALARM pin input voltage range	V_{ALIN}		0	-	AV_{CC}	V	
External low threshold high->low transition	$V_{EVTL(H->L)}$		0.36 * AV_{CC} -0.25	0.36 * AV_{CC} -0.1	-	V	INTREF = 0
External low threshold low->high transition	$V_{EVTL(L->H)}$		-	0.36 * AV_{CC} +0.1	0.36 * AV_{CC} +0.25	V	
External high threshold high->low transition	$V_{EVTH(H->L)}$		0.78 * AV_{CC} -0.25	0.78 * AV_{CC} -0.1	-	V	
External high threshold low->high transition	$V_{EVTH(L->H)}$			0.78 * AV_{CC} +0.1	0.78 * AV_{CC} +0.25	V	
Internal low threshold high->low transition	$V_{IVTL(H->L)}$		0.9	1.1	-	V	INTREF = 1
Internal low threshold low->high transition	$V_{IVTL(L->H)}$		-	1.3	1.55	V	
Internal high threshold high->low transition	$V_{IVTH(H->L)}$		2.2	2.4	-	V	
Internal high threshold low->high transition	$V_{IVTH(L->H)}$		-	2.6	2.85	V	
Switching hysteresis	V_{HYS}		50	-	300	mV	
Comparison time	t_{COMPF}		-	0.1	1	µs	CMD = 1 (fast)
	t_{COMPS}		-	1	10	µs	CMD = 0 (slow)
Power-up stabilization time after enabling alarm comparator	t_{PD}		-	1	10	ms	Threshold levels specified above are not guaranteed within this time
Slow/Fast mode transition time	t_{CMD}		-	100	500	µs	

7. Low Voltage Detector characteristics

(T_A = -40 ˚C to +125 ˚C, V_{cc} = AV_{cc} = 3.0V - 5.5V, V_{ss} = AV_{ss} = 0V)

Parameter	Symbol	Value *1		Value *2		Unit	Remarks
		Min	Max	Min	Max		
Stabilization time	$T_{LVDSTAB}$	-	75	-	110	µs	After power-up or change of detection level
Level 0	V_{DL0}	2.7	2.9	2.5	2.9	V	CILCR:LVL[3:0]=”0000”
Level 1	V_{DL1}	2.9	3.1	2.8	3.2	V	CILCR:LVL[3:0]=”0001”
Level 2	V_{DL2}	3.1	3.3	3	3.4	V	CILCR:LVL[3:0]=”0010”
Level 3	V_{DL3}	3.5	3.75	3.35	3.8	V	CILCR:LVL[3:0]=”0011”
Level 4	V_{DL4}	3.6	3.85	3.5	3.95	V	CILCR:LVL[3:0]=”0100”
Level 5	V_{DL5}	3.7	3.95	3.6	4.1	V	CILCR:LVL[3:0]=”0101”
Level 6	V_{DL6}	3.8	4.05	3.7	4.2	V	CILCR:LVL[3:0]=”0110”
Level 7	V_{DL7}	3.9	4.15	3.8	4.3	V	CILCR:LVL[3:0]=”0111”
Level 8	V_{DL8}	4.0	4.25	3.9	4.4	V	CILCR:LVL[3:0]=”1000”
Level 9	V_{DL9}	4.1	4.35	3.95	4.5	V	CILCR:LVL[3:0]=”1001”
Level 10	V_{DL10}	not used		not used			
Level 11	V_{DL11}	not used		not used			
Level 12	V_{DL12}	not used		2.6	3	V	CILCR:LVL[3:0]=”1100”
Level 13	V_{DL13}	not used		not used			
Level 14	V_{DL14}	not used		not used			
Level 15	V_{DL15}	not used		not used			

*1: valid for all devices except devices listed under “*2”

*2: valid for: MB96F345

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

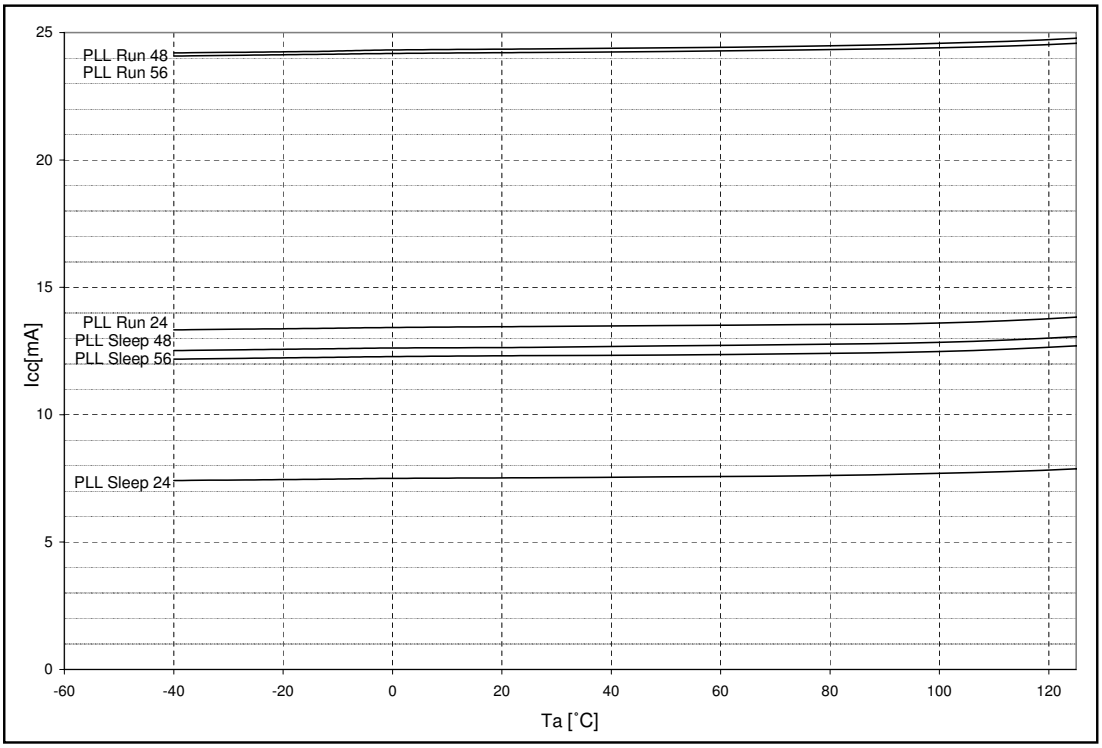
For correct detection, the slope of the voltage level must satisfy $\left|\frac{dV}{dt}\right| \leq 0.004\frac{V}{\mu s}$.

Faster variations are regarded as noise and may not be detected.

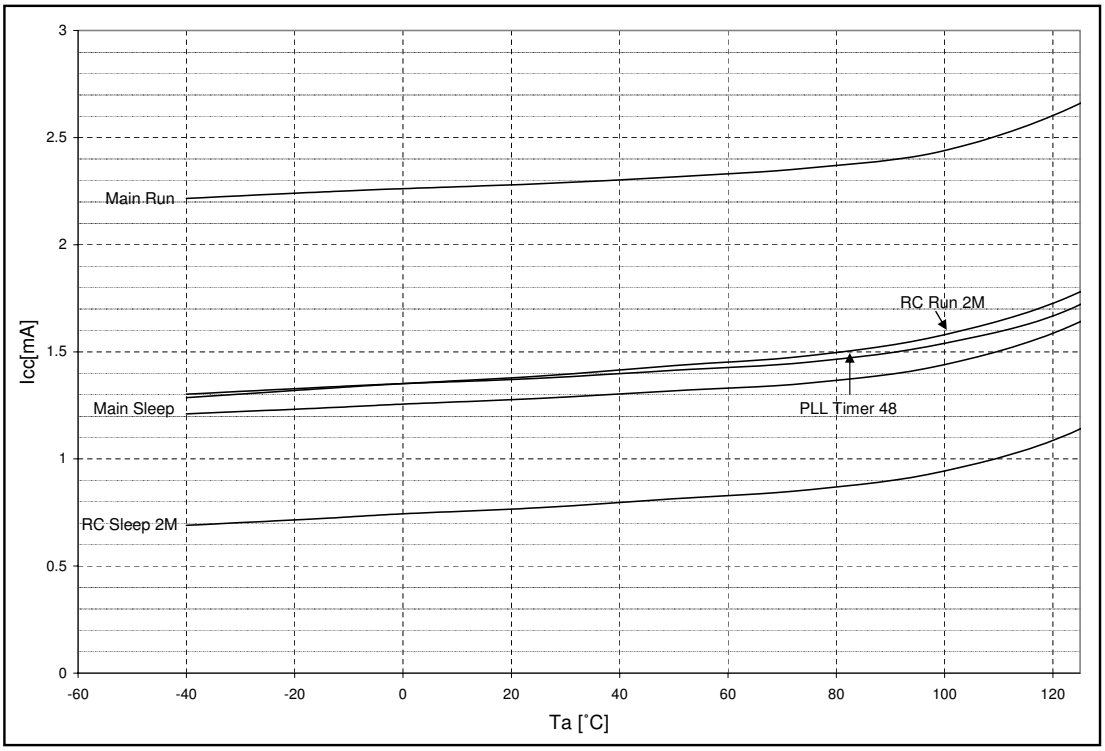
The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of “Level 0” (V_{DL0_MIN}). The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

Mode name	Details
PLL Sleep 48	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2} = 96MHz$ • $f_{CLKP1} = 48MHz$ • $f_{CLKP2} = 24MHz$ • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • RC oscillator and Sub oscillator stopped
PLL Sleep 40	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2} = 80MHz$ • $f_{CLKP1} = 40MHz$ • $f_{CLKP2} = 20MHz$ • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • RC oscillator and Sub oscillator stopped
PLL Sleep 36	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2} = 72MHz$ • $f_{CLKP1} = 36MHz$ • $f_{CLKP2} = 18MHz$ • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • RC oscillator and Sub oscillator stopped
PLL Sleep 24	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2} = 48MHz$ • $f_{CLKP1} = f_{CLKP2} = 24MHz$ • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • RC oscillator and Sub oscillator stopped
Main Sleep	Main Sleep mode current $I_{CCSMAIN}$ with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2} = 4MHz$ • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • PLL, RC oscillator and Sub oscillator stopped
RC Sleep 2M	RC Sleep mode current I_{CCSRCH} with the following settings: • RC oscillator set to 2MHz (CKFCR:RCFS = 1) • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2} = 2MHz$ • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • PLL, Main oscillator and Sub oscillator stopped
RC Sleep 100k	RC Sleep mode current I_{CCSRCL} with the following settings: • RC oscillator set to 100kHz (CKFCR:RCFS = 0) • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2} = 100kHz$ • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped

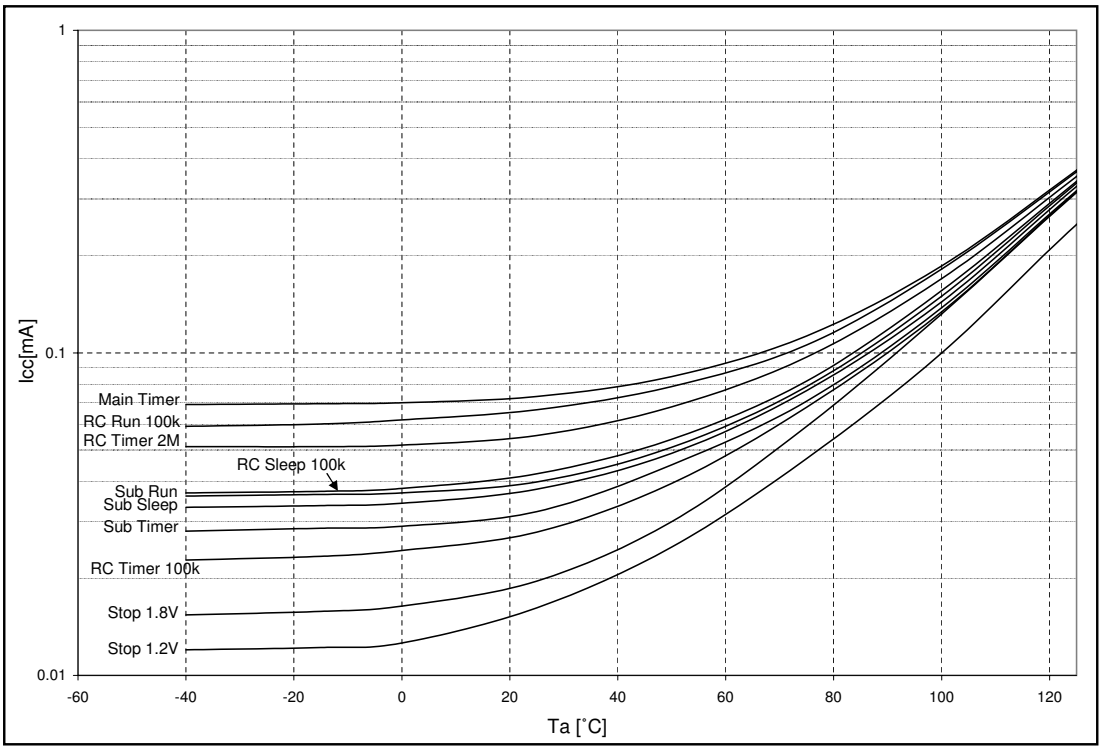
MB96345/346 PLL Run and Sleep mode currents



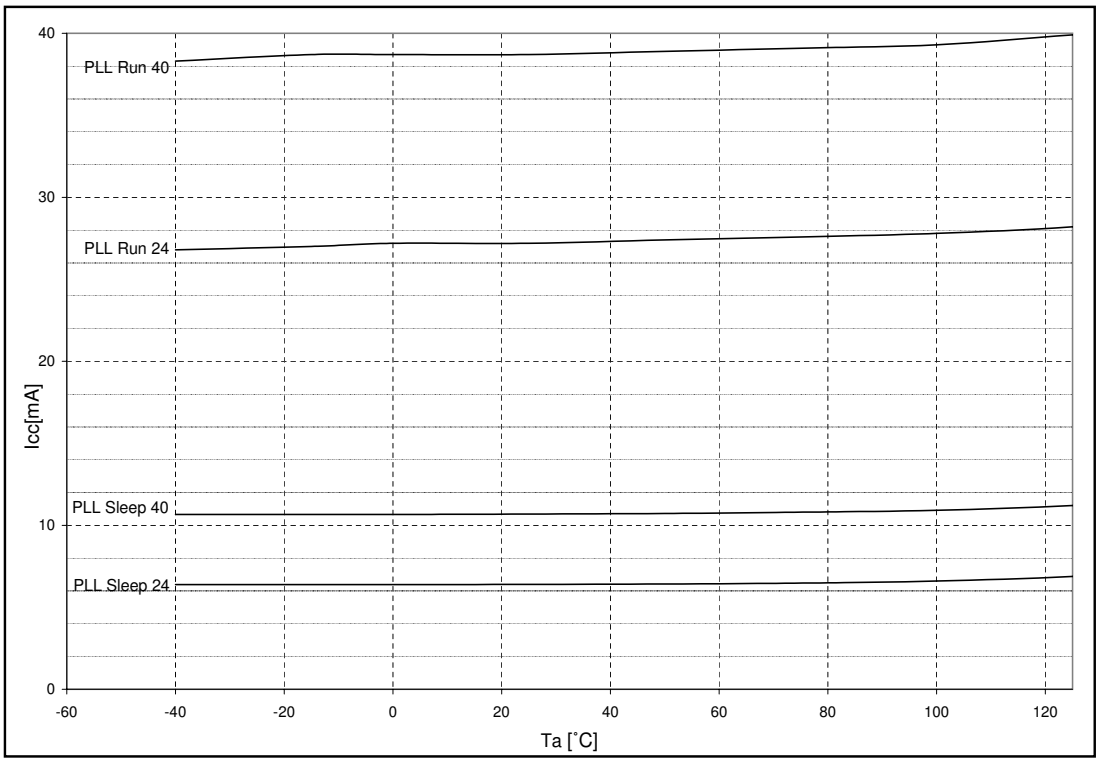
MB96345/346 operation modes with medium currents



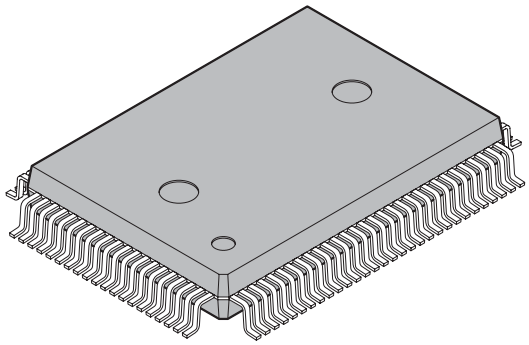
MB96345/346 Low power mode currents

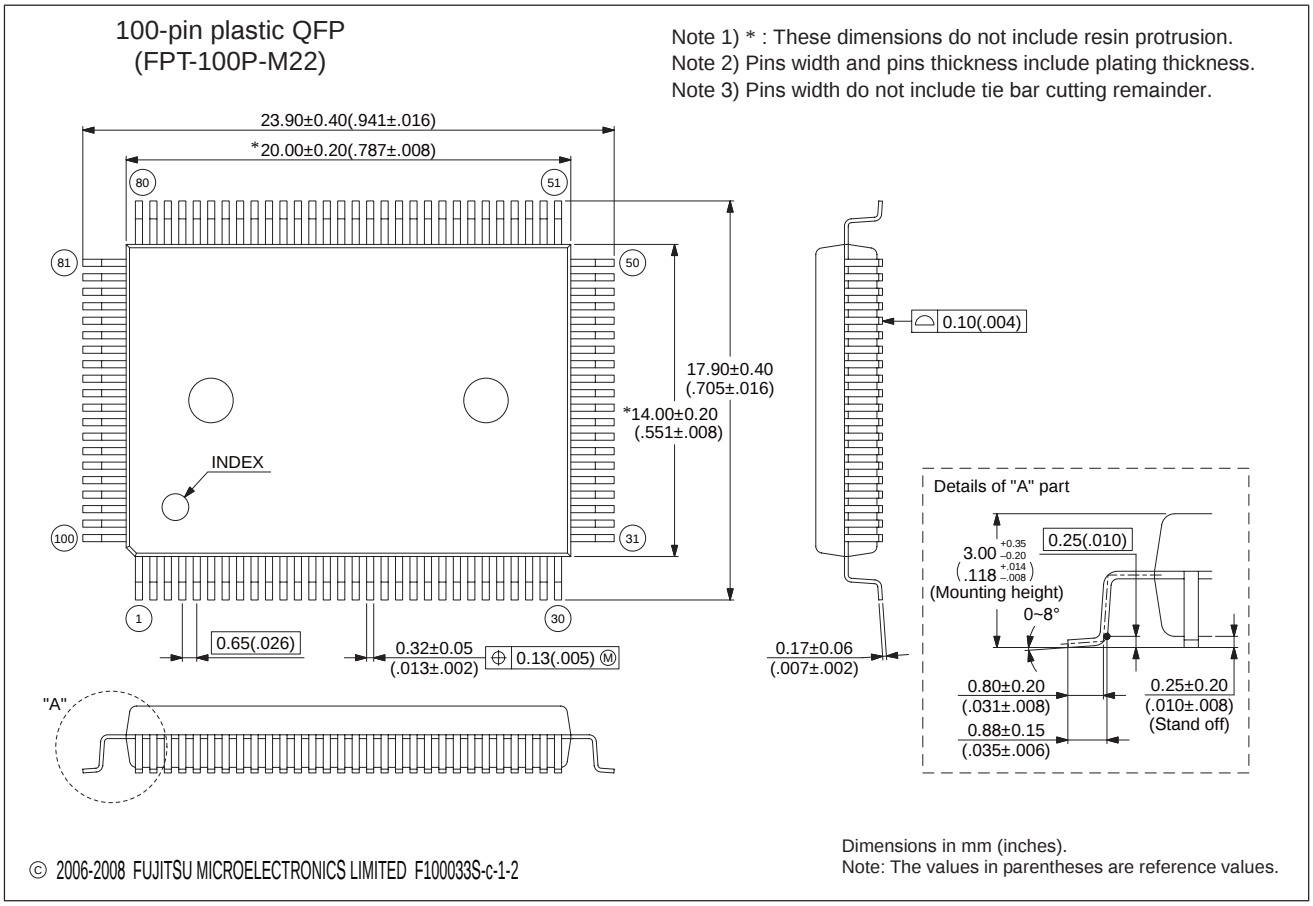


MB96F345 PLL Run and Sleep mode currents



■ PACKAGE DIMENSION MB96(F)34x QFP 100P

100-pin plastic QFP		
	Lead pitch	0.65 mm
	Package width × package length	14.00 mm × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65
(FPT-100P-M22)		



Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ ORDERING INFORMATION

MCU with CAN controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96345YSA PQC-GSE2 *1	ROM (160KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96345RSA PQC-GSE2 *1			No	
MB96345YWA PQC-GSE2 *1		Yes	Yes	
MB96345RWA PQC-GSE2 *1			No	
MB96345YSA PMC-GSE2 *1		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96345RSA PMC-GSE2 *1			No	
MB96345YWA PMC-GSE2 *1		Yes	Yes	
MB96345RWA PMC-GSE2 *1			No	
MB96346YSA PQC-GSE2 *1	ROM (288KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96346RSA PQC-GSE2 *1			No	
MB96346YWA PQC-GSE2 *1		Yes	Yes	
MB96346RWA PQC-GSE2 *1			No	
MB96346YSA PMC-GSE2 *1		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96346RSA PMC-GSE2 *1			No	
MB96346YWA PMC-GSE2 *1		Yes	Yes	
MB96346RWA PMC-GSE2 *1			No	
MB96F345FSB PQC-GSE2 *1	Flash A (160KB) Data Flash A (64KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F345DSB PQC-GSE2 *1			No	
MB96F345FWB PQC-GSE2 *1		Yes	Yes	
MB96F345DWB PQC-GSE2 *1			No	
MB96F345FSB PMC-GSE2 *1		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F345DSB PMC-GSE2 *1			No	
MB96F345FWB PMC-GSE2 *1		Yes	Yes	
MB96F345DWB PMC-GSE2 *1			No	