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Applications of "Embedded - Microcontrollers"

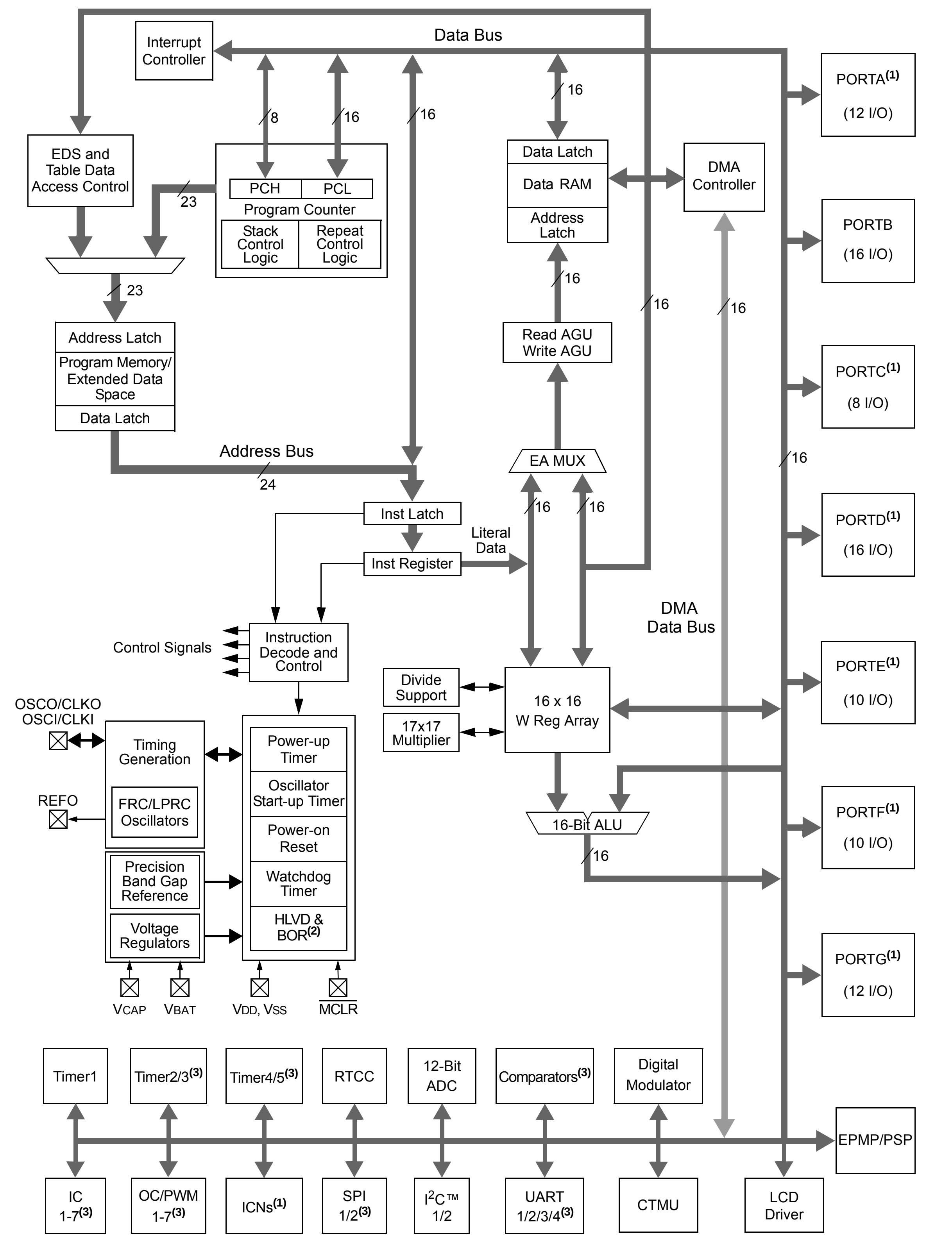
Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128ga308t-i-pt

TABLE 1-1: DEVICE FEATURES FOR THE PIC24FJ128GA310 FAMILY: 64-PIN

Features	PIC24FJ64GA306	PIC24FJ128GA306
Operating Frequency	DC – 32 MHz	
Program Memory (bytes)	64K	128K
Program Memory (instructions)	22,016	44,032
Data Memory (bytes)	8K	
Interrupt Sources (soft vectors/ NMI traps)	65 (61/4)	
I/O Ports	Ports B, C, D, E, F, G	
Total I/O Pins	53	
Remappable Pins	30 (29 I/Os, 1 input only)	
Timers:		
Total Number (16-bit)	5(1)	
32-Bit (from paired 16-bit timers)	2	
Input Capture Channels	7(1)	
Output Compare/PWM Channels	7(1)	
Input Change Notification Interrupt	52	
Serial Communications:		
UART	4(1)	
SPI (3-wire/4-wire)	2(1)	
I^2C™	2	
Digital Signal Modulator	Yes	
Parallel Communications (EPMP/PSP)	Yes	
JTAG Boundary Scan	Yes	
12/10-Bit Analog-to-Digital Converter (ADC) Module (input channels)	16	
Analog Comparators	3	
CTMU Interface	Yes	
LCD Controller (available pixels)	240 (30 SEG x 8 COM)	
Resets (and Delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)	
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations	
Packages	64-Pin TQFP and QFN	

Note 1: Peripherals are accessible through remappable pins.

FIGURE 1-1: PIC24FJ128GA310 FAMILY GENERAL BLOCK DIAGRAM



Note 1: Not all I/O pins or features are implemented on all device pinout configurations. See Table 1-4 for specific implementations by pin count.

2: BOR functionality is provided when the on-board voltage regulator is enabled.

3: These peripheral I/Os are only accessible through remappable pins.

TABLE 4-10: UART REGISTER MAPS

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART1 Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UART1 Receive Register									0000
U1BRG	0228	Baud Rate Generator Prescaler Register																0000
U2MODE	0230	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	—	—	—	—	—	—	—	UART2 Transmit Register									xxxx
U2RXREG	0236	—	—	—	—	—	—	—	UART2 Receive Register									0000
U2BRG	0238	Baud Rate Generator Prescaler Register																0000
U3MODE	0250	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U3STA	0252	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U3TXREG	0254	—	—	—	—	—	—	—	UART3 Transmit Register									xxxx
U3RXREG	0256	—	—	—	—	—	—	—	UART3 Receive Register									0000
U3BRG	0258	Baud Rate Generator Prescaler Register																0000
U4MODE	02B0	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U4STA	02B2	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U4TXREG	02B4	—	—	—	—	—	—	—	UART4 Transmit Register									xxxx
U4RXREG	02B6	—	—	—	—	—	—	—	UART4 Receive Register									0000
U4BRG	02B8	Baud Rate Generator Prescaler Register																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 5-3: DMAINTx: DMA CHANNEL x INTERRUPT REGISTER

R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DBUFWF[(1)]	—	CHSEL5	CHSEL4	CHSEL3	CHSEL2	CHSEL1	CHSEL0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
HIGHIF[(1,2)]	LOWIF[(1,2)]	DONEIF[(1)]	HALFIF[(1)]	OVRUNIF[(1)]	—	—	HALFEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **DBUFWF:** Buffered Data Write Flag bit[(1)]
1 = The contents of the DMA buffer have not been written to the location specified in DMADSTx or DMASRCx in Null Write mode
0 = The contents of the DMA buffer have been written to the location specified in DMADSTx or DMASRCx in Null Write mode

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **CHSEL<5:0>:** DMA Channel Trigger Selection bits
See Table 5-1 for a complete list.

bit 7 **HIGHIF:** DMA High Address Limit Interrupt Flag bit[(1,2)]
1 = The DMA channel has attempted to access an address higher than DMAH or the upper limit of the data RAM space
0 = The DMA channel has not invoked the high address limit interrupt

bit 6 **LOWIF:** DMA Low Address Limit Interrupt Flag bit[(1,2)]
1 = The DMA channel has attempted to access the DMA SFR address lower than DMAL, but above the SFR range (07FFh)
0 = The DMA channel has not invoked the low address limit interrupt

bit 5 **DONEIF:** DMA Complete Operation Interrupt Flag bit[(1)]
If CHEN = 1:
1 = The previous DMA session has ended with completion
0 = The current DMA session has not yet completed
If CHEN = 0:
1 = The previous DMA session has ended with completion
0 = The previous DMA session has ended without completion

bit 4 **HALFIF:** DMA 50% Watermark Level Interrupt Flag bit[(1)]
1 = DMACNTx has reached the halfway point to 0000h
0 = DMACNTx has not reached the halfway point

bit 3 **OVRUNIF:** DMA Channel Overrun Flag bit[(1)]
1 = The DMA channel is triggered while it is still completing the operation based on the previous trigger
0 = The overrun condition has not occurred

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **HALFEN:** Halfway Completion Watermark bit
1 = Interrupts are invoked when DMACNTx has reached its halfway point and is at completion
0 = An interrupt is invoked only at the completion of the transfer

Note 1: Setting these flags in software does not generate an interrupt.
2: Testing for address limit violations (DMASRCx or DMADSTx is either greater than DMAH or less than DMAL) is NOT done before the actual access.

7.0 RESETS

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Reset"** (DS39712) in the *"dsPIC33/PIC24 Family Reference Manual"*, . The information in this data sheet supersedes the information in the FRM.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{\text{SYSRST}}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- $\overline{\text{MCLR}}$: Pin Reset
- SWR: RESET Instruction
- WDT: Watchdog Timer Reset
- BOR: Brown-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Opcode Reset
- UWR: Uninitialized W Register Reset

A simplified block diagram of the Reset module is shown in Figure 7-1.

Any active source of Reset will make the $\overline{\text{SYSRST}}$ signal active. Many registers associated with the CPU and peripherals are forced to a known Reset state. Most registers are unaffected by a Reset; their status is unknown on POR and unchanged by all other Resets.

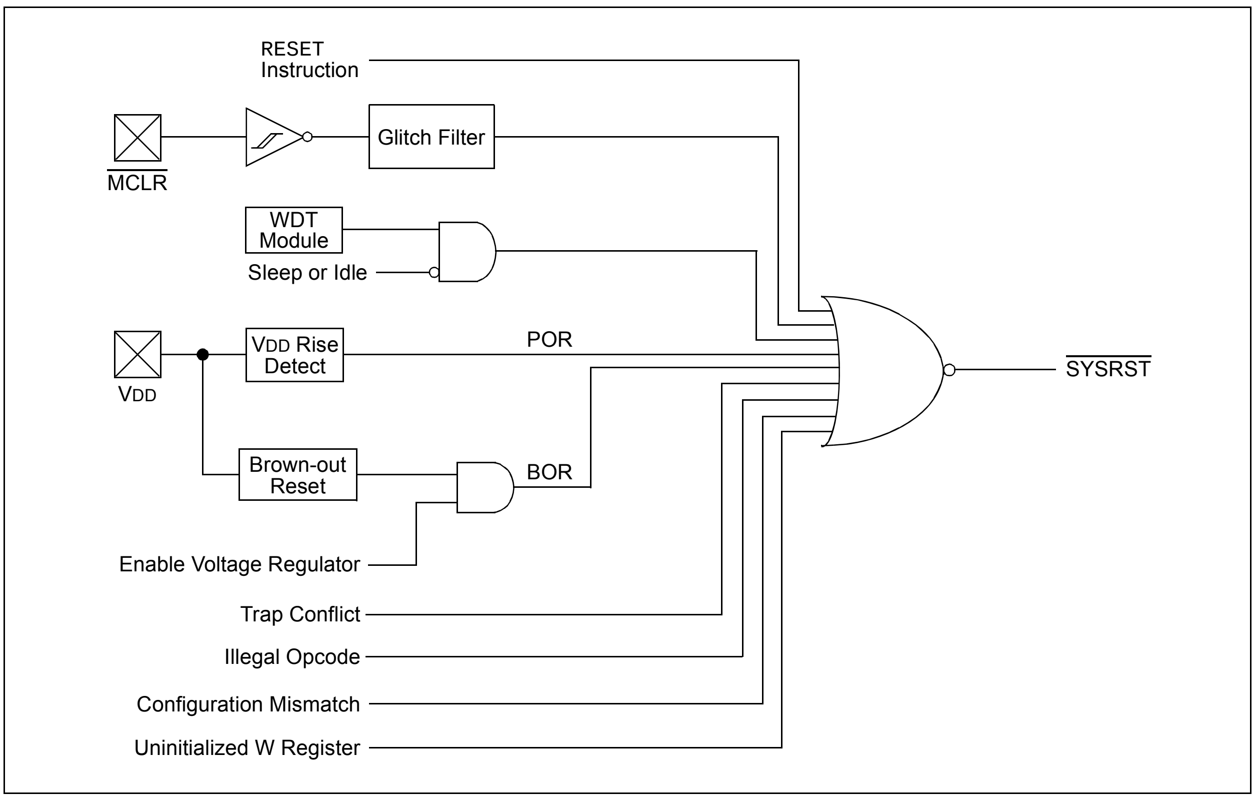
Note:	Refer to the specific peripheral or CPU section of this manual for register Reset states.

All types of device Reset will set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 7-1). In addition, Reset events occurring while an extreme power-saving feature is in use (such as VBAT) will set one or more status bits in the RCON2 register (Register 7-2). A POR will clear all bits, except for the BOR and POR (RCON<1:0>) bits, which are set. The user may set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software will not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this data sheet.

Note:	The status bits in the RCON registers should be cleared after they are read so that the next RCON register values after a device Reset will be meaningful.

FIGURE 7-1: RESET SYSTEM BLOCK DIAGRAM



REGISTER 8-7: IFS2: INTERRUPT FLAG STATUS REGISTER 2

U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DMA4IF	PMPIF	—	OC7IF	OC6IF	OC5IF	IC6IF
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
IC5IF	IC4IF	IC3IF	DMA3IF	—	—	SPI2IF	SPF2IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14 **DMA4IF:** DMA Channel 4 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13 **PMPIF:** Parallel Master Port Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12 **Unimplemented:** Read as ‘0’

bit 11 **OC7IF:** Output Compare Channel 7 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 10 **OC6IF:** Output Compare Channel 6 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 9 **OC5IF:** Output Compare Channel 5 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 8 **IC6IF:** Input Capture Channel 6 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 7 **IC5IF:** Input Capture Channel 5 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6 **IC4IF:** Input Capture Channel 4 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5 **IC3IF:** Input Capture Channel 3 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4 **DMA3IF:** DMA Channel 3 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1 **SPI2IF:** SPI2 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 8-13: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0 (CONTINUED)

bit 2	**OC1IE:** Output Compare Channel 1 Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 1	**IC1IE:** Input Capture Channel 1 Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 0	**INT0IE:** External Interrupt 0 Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled

REGISTER 8-19: IEC6: INTERRUPT ENABLE CONTROL REGISTER 6

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0
—	—	—	LCDIE	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4 **LCDIE:** LCD Controller Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 3-0 **Unimplemented:** Read as '0'

REGISTER 8-20: IEC7: INTERRUPT ENABLE CONTROL REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	JTAGIE	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5 **JTAGIE:** JTAG Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 4-0 **Unimplemented:** Read as '0'

15.0 OUTPUT COMPARE WITH DEDICATED TIMERS

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Output Compare with Dedicated Timer"** (DS39723) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

Devices in the PIC24FJ128GA310 family all feature seven independent output compare modules. Each of these modules offers a wide range of configuration and operating options for generating pulse trains on internal device events, and can produce Pulse-Width Modulated waveforms for driving power applications.

Key features of the output compare module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 31 user-selectable trigger/sync sources available
- Two separate Period registers (a main register, OCxR, and a secondary register, OCxRS) for greater flexibility in generating pulses of varying widths
- Configurable for single pulse or continuous pulse generation on an output event, or continuous PWM waveform generation
- Up to 6 clock sources available for each module, driving a separate internal 16-bit counter

15.1 General Operating Modes

15.1.1 SYNCHRONOUS AND TRIGGER MODES

When the output compare module operates in a Free-Running mode, the internal 16-bit counter, OCxTMR, counts up continuously, wrapping around from 0xFFFF to 0x0000 on each overflow. Its period is synchronized to the selected external clock source. Compare or PWM events are generated each time a match between the internal counter and one of the Period registers occurs.

In Synchronous mode, the module begins performing its compare or PWM operation as soon as its selected clock source is enabled. Whenever an event occurs on the selected sync source, the module's internal counter is reset. In Trigger mode, the module waits for a sync event from another internal module to occur before allowing the counter to run.

Free-Running mode is selected by default or any time that the SYNCSELx bits (OCxCON2<4:0>) are set to '00000'. Synchronous or Trigger modes are selected any time the SYNCSELx bits are set to any value except '00000'. The OCTRIG bit (OCxCON2<7>) selects either Synchronous or Trigger mode; setting the bit selects Trigger mode operation. In both modes, the SYNCSELx bits determine the sync/trigger source.

15.1.2 CASCADED (32-BIT) MODE

By default, each module operates independently with its own set of 16-Bit Timer and Duty Cycle registers. To increase resolution, adjacent even and odd modules can be configured to function as a single 32-bit module. (For example, Modules 1 and 2 are paired, as are Modules 3 and 4, and so on.) The odd numbered module (OCx) provides the Least Significant 16 bits of the 32-bit register pairs and the even module (OCy) provides the Most Significant 16 bits. Wraparounds of the OCx registers cause an increment of their corresponding OCy registers.

Cascaded operation is configured in hardware by setting the OC32 bit (OCxCON2<8>) for both modules. For more details on cascading, refer to **"Output Compare with Dedicated Timer"** (DS39723) in the *"dsPIC33/PIC24 Family Reference Manual"*.

17.0 INTER-INTEGRATED CIRCUIT™ (I^2C™)

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Inter-Integrated Circuit™ (I^2C™)"** (DS70000195) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The Inter-Integrated Circuit™ (I^2C™) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, display drivers, ADC Converters, etc.

The I^2C module supports these features:

- Independent master and slave logic
- 7-bit and 10-bit device addresses
- General call address as defined in the I^2C protocol
- Clock stretching to provide delays for the processor to respond to a slave data request
- Both 100 kHz and 400 kHz bus specifications
- Configurable address masking
- Multi-Master modes to prevent loss of messages in arbitration
- Bus Repeater mode, allowing the acceptance of all messages as a slave regardless of the address
- Automatic SCL

A block diagram of the module is shown in Figure 17-1.

17.1 Communicating as a Master in a Single Master Environment

The details of sending a message in Master mode depends on the communications protocol for the device being communicated with. Typically, the sequence of events is as follows:

1. Assert a Start condition on SDAx and SCLx.
2. Send the I^2C device address byte to the slave with a write indication.
3. Wait for and verify an Acknowledge from the slave.
4. Send the first data byte (sometimes known as the command) to the slave.
5. Wait for and verify an Acknowledge from the slave.
6. Send the serial memory address low byte to the slave.
7. Repeat Steps 4 and 5 until all data bytes are sent.
8. Assert a Repeated Start condition on SDAx and SCLx.
9. Send the device address byte to the slave with a read indication.
10. Wait for and verify an Acknowledge from the slave.
11. Enable master reception to receive serial memory data.
12. Generate an ACK or NACK condition at the end of a received byte of data.
13. Generate a Stop condition on SDAx and SCLx.

17.2 Setting Baud Rate When Operating as a Bus Master

To compute the Baud Rate Generator reload value, use Equation 17-1.

EQUATION 17-1: COMPUTING BAUD RATE RELOAD VALUE(1,2)

$$FSCL = \frac{FCY}{I2CxBRG + 1 + \frac{FCY}{10,000,000}}$$

or:

$$I2CxBRG = \left(\frac{FCY}{FSCL} - \frac{FCY}{10,000,000} - 1\right)$$

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

2: These clock rate values are for guidance only. The actual clock rate can be affected by various system level parameters. The actual clock rate should be measured in its intended application.

17.3 Slave Address Masking

The I2CxMSK register (Register 17-3) designates address bit positions as "don't care" for both 7-Bit and 10-Bit Addressing modes. Setting a particular bit location (= `1`) in the I2CxMSK register causes the slave module to respond whether the corresponding address bit value is a '`0`' or a '`1`'. For example, when I2CxMSK is set to '`00100000`', the slave module will detect both addresses, '`0000000`' and '`0100000`'.

To enable address masking, the Intelligent Peripheral Management Interface (IPMI) must be disabled by clearing the IPMIEN bit (I2CxCON<11>).

Note: As a result of changes in the I2C™ protocol, the addresses in Table 17-2 are reserved and will not be Acknowledged in Slave mode. This includes any address mask settings that include any of these addresses.

TABLE 17-1: I2C™ CLOCK RATES(1,2)

Required System FSCL	FCY	I2CxBRG Value		Actual FSCL
		(Decimal)	(Hexadecimal)	
100 kHz	16 MHz	157	9D	100 kHz
100 kHz	8 MHz	78	4E	100 kHz
100 kHz	4 MHz	39	27	99 kHz
400 kHz	16 MHz	37	25	404 kHz
400 kHz	8 MHz	18	12	404 kHz
400 kHz	4 MHz	9	9	385 kHz
400 kHz	2 MHz	4	4	385 kHz
1 MHz	16 MHz	13	D	1.026 MHz
1 MHz	8 MHz	6	6	1.026 MHz
1 MHz	4 MHz	3	3	0.909 MHz

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

2: These clock rate values are for guidance only. The actual clock rate can be affected by various system level parameters. The actual clock rate should be measured in its intended application.

TABLE 17-2: I^{2}C™ RESERVED ADDRESSES(1)

Slave Address	R/$\overline{W}$ Bit	Description
`0000 000`	`0`	General Call Address(2)
`0000 000`	`1`	Start Byte
`0000 001`	`x`	CBus Address
`0000 01x`	`x`	Reserved
`0000 1xx`	`x`	HS Mode Master Code
`1111 0xx`	`x`	10-Bit Slave Upper Byte(3)
`1111 1xx`	`x`	Reserved

Note 1: The address bits listed here will never cause an address match, independent of address mask settings.

2: The address will be Acknowledged only if GCEN = `1`.

3: A match on this address can only occur on the upper byte in 10-Bit Addressing mode.

REGISTER 17-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I^2C master; applicable during master receive)
Value that will be transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit (when operating as I^2C master; applicable during master receive)
1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits the ACKDT data bit. Hardware is clear at the end of the master Acknowledge sequence.
0 = Acknowledge sequence is not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as I^2C master)
1 = Enables Receive mode for I^2C. Hardware is clear at the end of the eighth bit of the master receive data byte.
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I^2C master)
1 = Initiates Stop condition on the SDAx and SCLx pins. Hardware is clear at the end of the master Stop sequence.
0 = Stop condition is not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Repeated Start condition on the SDAx and SCLx pins. Hardware is clear at the end of the master Repeated Start sequence.
0 = Repeated Start condition is not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Start condition on SDAx and SCLx pins. Hardware is clear at the end of the master Start sequence.
0 = Start condition is not in progress

REGISTER 17-2: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10
bit 15							bit 8

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D/$\overline{\text{A}}$	P	S	R/$\overline{\text{W}}$	RBF	TBF
bit 7							bit 0

Legend:	C = Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown
HSC = Hardware Settable/Clearable bit			

bit 15 **ACKSTAT:** Acknowledge Status bit
1 = NACK was detected last
0 = ACK was detected last
Hardware is set or cleared at the end of Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit
(when operating as I^{2}C™ master; applicable to master transmit operation.)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware is set at the beginning of master transmission; hardware is clear at the end of slave Acknowledge.

bit 13-11 **Unimplemented:** Read as ‘0’

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware is set at the detection of a bus collision.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware is set when the address matches the general call address; hardware is clear at Stop detection.

bit 8 **ADD10:** 10-Bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware is set at the match of the 2nd byte of the matched 10-bit address; hardware is clear at Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the I^{2}C module is busy
0 = No collision
Hardware is set at an occurrence of write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

bit 5 **D/$\overline{\text{A}}$:** Data/$\overline{\text{Address}}$ bit (when operating as I^{2}C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was a device address
Hardware is clear at the device address match. Hardware is set after a transmission finishes or by reception of a slave byte.

NOTES:

20.0 ENHANCED PARALLEL MASTER PORT (EPMP)

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Enhanced Parallel Master Port (EPMP)"** (DS39730) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The Enhanced Parallel Master Port (EPMP) module provides a parallel, 4-bit (Master mode only), 8-bit (Master and Slave modes) or 16-bit (Master mode only) data bus interface to communicate with off-chip modules, such as memories, FIFOs, LCD controllers and other microcontrollers. This module can serve as either the master or the slave on the communication bus.

For EPMP Master modes, all external addresses are mapped into the internal Extended Data Space (EDS). This is done by allocating a region of the EDS for each Chip Select, and then assigning each Chip Select to a particular external resource, such as a memory or external controller. This region should not be assigned to another device resource, such as RAM or SFRs. To perform a write or read on an external resource, the CPU simply performs a write or read within the address range assigned for the EPMP.

Key features of the EPMP module are:

- Extended Data Space (EDS) Interface allows Direct Access from the CPU
- Up to 23 Programmable Address Lines
- Up to 2 Chip Select Lines
- Up to 2 Acknowledgment Lines (one per Chip Select)
- 4-Bit, 8-Bit or 16-Bit-Wide Data Bus
- Programmable Strobe Options (per Chip Select):
  - Individual Read and Write Strobes or;
  - Read/Write Strobe with Enable Strobe
- Programmable Address/Data Multiplexing
- Programmable Address Wait States
- Programmable Data Wait States (per Chip Select)
- Programmable Polarity on Control Signals (per Chip Select)
- Legacy Parallel Slave Port Support
- Enhanced Parallel Slave Support:
  - Address Support
  - 4-Byte Deep Auto-Incrementing Buffer

20.1 Specific Package Variations

While all PIC24FJ128GA310 family devices implement the EPMP, I/O pin constraints place some limits on 16-Bit Master mode operations in some package types. This is reflected in the number of dedicated Chip Select pins implemented and the number of dedicated address lines that are available. The differences are summarized in Table 20-1. All available EPMP pin functions are summarized in Table 20-2.

For 64-pin devices, the dedicated Chip Select pins (PMCS1 and PMCS2) are not implemented. In addition, only 16 address lines (PMA<15:0>) are available. If required, PMA14 and PMA15 can be remapped to function as PMCS1 and PMCS2, respectively.

For 80-pin devices, the dedicated PMCS2 pin is not implemented. It also only implements 16 address lines (PMA<15:0>). If required, PMA15 can be remapped to function as PMCS2.

The memory space addressable by the device depends on the number of address lines available, as well as the number of Chip Select signals required for the application. Devices with lower pin counts are more affected by Chip Select requirements, as these take away address lines. Table 20-1 shows the maximum addressable range for each pin count.

TABLE 20-1: EPMP FEATURE DIFFERENCES BY DEVICE PIN COUNT

Device	Dedicated Chip Select		Address Lines	Address Range (bytes)		
	CS1	CS2		No CS	1 CS	2 CS
PIC24FJXXXGA306 (64-pin)	—	—	16	64K	32K	16K
PIC24FJXXXGA308 (80-pin)	X	—	16	64K		32K
PIC24FJXXXGA310 (100-pin)	X	X	23	16M		

FIGURE 22-2: ALARM MASK SETTINGS

Alarm Mask Setting (AMASK<3:0>)	Day of the Week	Month	Day	Hours	Minutes	Seconds
`0000` - Every half second `0001` - Every second						
`0010` - Every 10 seconds						s
`0011` - Every minute						s s
`0100` - Every 10 minutes					m	s s
`0101` - Every hour					m m	s s
`0110` - Every day				h h	m m	s s
`0111` - Every week	d			h h	m m	s s
`1000` - Every month			d d	h h	m m	s s
`1001` - Every year[(1)]		m m	d d	h h	m m	s s

Note 1: Annually, except when configured for February 29.

22.6 Power Control

The RTCC includes a power control feature that allows the device to periodically wake-up an external device, wait for the device to be stable before sampling wake-up events from that device, and then shut down the external device. This can be done completely autonomously by the RTCC, without the need to wake from the current lower power mode (Sleep, Deep Sleep, etc.).

To use this feature:

1. Enable the RTCC (RTCEN = `1`).
2. Set the PWCEN bit (RTCPWC<15>).
3. Configure the RTCC pin to drive the PWC control signal (RTCOE = `1` and RTCOUT<1:0> = `11`).

The polarity of the PWC control signal may be chosen using the PWCPOL bit (RTCPWC<14>). An active-low or active-high signal may be used with the appropriate external switch to turn on or off the power to one or more external devices. The active-low setting may also be used in conjunction with an open-drain setting on the RTCC pin, in order to drive the ground pin(s) of the external device directly (with the appropriate external VDD pull-up device), without the need for external switches. Finally, the CHIME bit should be set to enable the PWC periodicity.

22.7 RTCC VBAT Operation

The RTCC can operate in VBAT mode when there is a power loss on the VDD pin. The RTCC will continue to operate if the VBAT pin is powered on (it is usually connected to the battery).

> **Note:** It is recommended to connect the VBAT pin to VDD if the VBAT mode is not used (not connected to the battery).

The VBAT BOR can be enabled/disabled using the VBTBOR bit in the CW3 Configuration register (CW3<7>). If the VBTBOR enable bit is cleared, the VBAT BOR is always disabled and there will be no indication of a VBAT BOR. If the VBTBOR bit is set, the RTCC can receive a Reset and the RTCEN bit will get cleared when the voltage reaches VBTRTC.

NOTES:

REGISTER 29-2: CW2: FLASH CONFIGURATION WORD 2

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R/PO-1	r-1	r-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
IESO	r	r	$\overline{\text{ALTVRF1}}$	$\overline{\text{ALTVRF0}}$	FNOSC2	FNOSC1	FNOSC0
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-1	R/PO-1	R/PO-1
FCKSM1	FCKSM0	OSCIOFCN	IOL1WAY	BOREN1	r	POSCMD1	POSCMD0
bit 7							bit 0

Legend:	r = Reserved bit	PO = Program once bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-16 **Unimplemented:** Read as ‘1’

bit 15 **IESO:** Internal External Switchover bit
1 = IESO mode (Two-Speed Start-up) is enabled
0 = IESO mode (Two-Speed Start-up) is disabled

bit 14-13 **Reserved:** Always maintain as ‘1’

bit 12-11 **$\overline{\text{ALTVRF}}$<1:0>:** Alternate VREF/CVREF Pins Selection bits
00 = Comparator Voltage reference input VREF+ is RB0, VREF- is RB1, ADC VREF+ is RB0 and ADC VREF- is RB1
01 = Comparator Voltage reference input VREF+ is RB0, VREF- is RB1, ADC VREF+ is RA10 and ADC VREF- is RA9
10 = Comparator Voltage reference input VREF+ is RA10, VREF- is RA9, ADC VREF+ is RB0 and ADC VREF- is RB1
11 = Comparator Voltage reference input VREF+ is RA10, VREF- is RA9, ADC VREF+ is RA10 and ADC VREF- is RA9

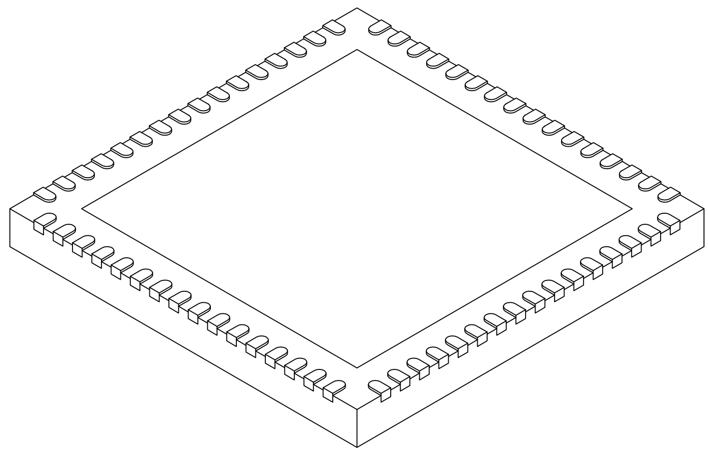
bit 10-8 **FNOSC<2:0>:** Initial Oscillator Select bits
111 = Fast RC Oscillator with Postscaler (FRCDIV)
110 = Reserved
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator with Postscaler and PLL module (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 7-6 **FCKSM<1:0>:** Clock Switching and Fail-Safe Clock Monitor Configuration bits
1x = Clock switching and Fail-Safe Clock Monitor are disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 5 **OSCIOFCN:** OSCO Pin Configuration bit
If POSCMD<1:0> = 11 or 00:
1 = OSCO/CLKO/RC15 functions as CLKO (FOSC/2)
0 = OSCO/CLKO/RC15 functions as port I/O (RC15)
If POSCMD<1:0> = 10 or 01:
OSCIOFCN has no effect on OSCO/CLKO/RC15.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.15 x 7.15 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	7.05	7.15	7.50
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	7.05	7.15	7.50
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-149C Sheet 2 of 2

NOTES:

