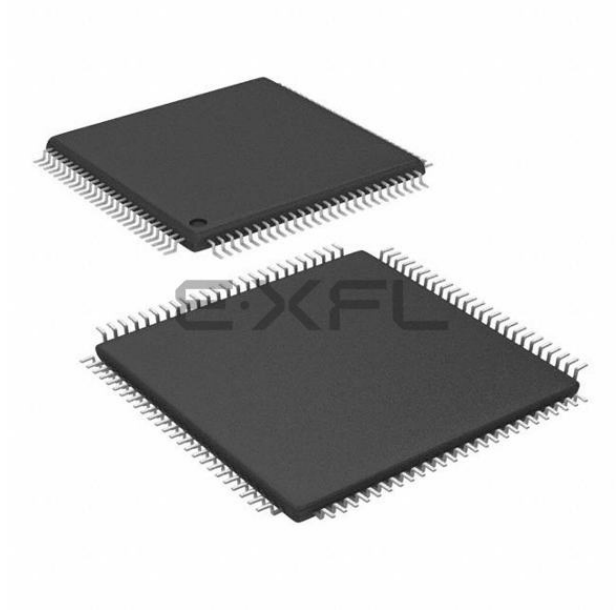
Microchip Technology - PIC24FJ64GA310T-I/PF Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64ga310t-i-pf

TABLE 1-4: PIC24FJ128GA310 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locater				I/O	Input Buffer	Description
	64-Pin TQFP	80-Pin TQFP	100-Pin TQFP	121-Pin BGA			
COM0	63	79	99	A2	O	—	LCD Driver Common Outputs.
COM1	62	78	98	B3	O	—	
COM2	61	77	94	B4	O	—	
COM3	60	76	93	A4	O	—	
COM4	59	73	88	A6	O	—	
COM5	23	29	34	L5	O	—	
COM6	22	28	33	L4	O	—	
COM7	21	27	32	K4	O	—	
CS1	45	57	71	C11	I/O	ST/TTL	Parallel Master Port Chip Select 1 Strobe (shared with PMA14).
CS2	44	56	70	D11	O	—	Parallel Master Port Chip Select 2 Strobe (shared with PMA15).
CTCMP	14	18	23	J2	I	ANA	CTMU Comparator 2 Input (Pulse mode).
CTED0	—	—	17	G3	I	DIG	CTMU External Edge Inputs.
CTED1	28	34	42	L7	I	DIG	
CTED2	27	33	41	J7	I	DIG	
CTED3	—	—	1	B2	I	DIG	
CTED4	1	1	3	D3	I	DIG	
CTED5	29	35	43	K7	I	DIG	
CTED6	30	36	44	L8	I	DIG	
CTED7	—	—	40	47	I	DIG	
CTED8	64	80	100	A1	I	DIG	
CTED9	63	79	99	A2	I	DIG	
CTED10	—	—	97	A3	I	DIG	
CTED11	—	—	95	C4	I	DIG	
CTED12	15	19	24	K1	I	DIG	
CTED13	14	18	23	J2	I	DIG	
CTPLS	29	35	43	K7	O	—	CTMU Pulse Output.
CV_{REF}	23	29	34	L5	O	—	Comparator Voltage Reference Output.
CV_{REF+}	16	20	25	K2	I	ANA	Comparator/ADC Reference Voltage (high) Input.
CV_{REF-}	15	19	24	K1	I	ANA	Comparator/ADC Reference Voltage (low) Input.
INT0	35	45	55	H9	I	ST	External Interrupt Input 0.
LCDBIAS0	3	3	5	D2	I	ANA	Bias Inputs for LCD Driver Charge Pump.
LCDBIAS1	2	2	4	C1	I	ANA	
LCDBIAS2	1	1	3	D3	I	ANA	
LCDBIAS3	17	21	26	L1	I	ANA	
HLVDIN	64	80	100	A1	I	ANA	High/Low-Voltage Detect Input.
$\overline{MCLR}$	7	9	13	F1	I	ST	Master Clear (device Reset) Input. This line is brought low to cause a Reset.
OSCI	39	49	63	F9	I	ANA	Main Oscillator Input Connection.
OSCO	40	50	64	F11	O	—	Main Oscillator Output Connection.

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C™ = I^2C/SMBus input buffer

TABLE 4-4: ICN REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNPD1	0056	CN15PDE	CN14PDE	CN13PDE	CN12PDE	CN11PDE	CN10PDE	CN9PDE	CN8PDE	CN7PDE	CN6PDE	CN5PDE	CN4PDE	CN3PDE	CN2PDE	—	—	0000
CNPD2	0058	CN31PDE	CN30PDE	CN29PDE	CN28PDE	CN27PDE	CN26PDE	CN25PDE	CN24PDE	CN23PDE	CN22PDE	CN21PDE(1)	CN20PDE(1)	CN19PDE(1)	CN18PDE	CN17PDE	CN16PDE	0000
CNPD3	005A	CN47PDE(1)	CN46PDE(2)	CN45PDE(1)	CN44PDE(1)	CN43PDE(1)	CN42PDE(1)	CN41PDE(1)	CN40PDE(2)	CN39PDE(2)	CN38PDE(2)	CN37PDE(2)	CN36PDE(2)	CN35PDE(2)	CN34PDE(2)	CN33PDE(2)	CN32PDE	0000
CNPD4	005C	CN63PDE	CN62PDE	CN61PDE	CN60PDE	CN59PDE	CN58PDE	CN57PDE	CN56PDE	CN55PDE	CN54PDE	CN53PDE	CN52PDE	CN51PDE	CN50PDE	CN49PDE	CN48PDE(2)	0000
CNPD5	005E	CN79PDE(2)	CN78PDE(1)	CN77PDE(1)	CN76PDE(2)	CN75PDE(2)	CN74PDE(1)	CN73PDE	CN72PDE	CN71PDE	CN70PDE	CN69PDE	CN68PDE	CN67PDE(1)	CN66PDE(1)	CN65PDE	CN64PDE	0000
CNPD6	0060	—	—	—	—	—	—	—	—	—	—	—	CN84PDE	CN83PDE(1)	CN82PDE(2)	CN81PDE(2)	CN80PDE(2)	0000
CNEN1	0062	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	—	—	0000
CNEN2	0064	CN31IE	CN30IE	CN29IE	CN28IE	CN27IE	CN26IE	CN25IE	CN24IE	CN23IE	CN22IE	CN21IE(1)	CN20IE(1)	CN19IE(1)	CN18IE	CN17IE	CN16IE	0000
CNEN3	0066	CN47IE(1)	CN46IE(1)	CN45IE(1)	CN44IE(1)	CN43IE(1)	CN42IE(1)	CN41IE(1)	CN40IE(2)	CN39IE(2)	CN38IE(2)	CN37IE(2)	CN36IE(2)	CN35IE(2)	CN34IE(2)	CN33IE(2)	CN32IE	0000
CNEN4	0068	CN63IE	CN62IE	CN61IE	CN60IE	CN59IE	CN58IE	CN57IE	CN56IE	CN55IE	CN54IE	CN53IE	CN52IE	CN51IE	CN50IE	CN49IE	CN48IE(2)	0000
CNEN5	006A	CN79IE(2)	CN78IE(1)	CN77IE(1)	CN76IE(2)	CN75IE(2)	CN74IE(1)	CN73IE	CN72IE	CN71IE	CN70IE	CN69IE	CN68IE	CN67IE(1)	CN66IE(1)	CN65IE	CN64IE	0000
CNEN6	006C	—	—	—	—	—	—	—	—	—	—	—	CN84IE	CN83IE(1)	CN82IE(2)	CN81IE(2)	CN80IE(2)	0000
CNPU1	006E	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	—	—	0000
CNPU2	0070	CN31PUE	CN30PUE	CN29PUE	CN28PUE	CN27PUE	CN26PUE	CN25PUE	CN24PUE	CN23PUE	CN22PUE	CN21PUE(1)	CN20PUE(1)	CN19PUE(1)	CN18PUE	CN17PUE	CN16PUE	0000
CNPU3	0072	CN47PUE(1)	CN46PUE(1)	CN45PUE(1)	CN44PUE(1)	CN43PUE(1)	CN42PUE(1)	CN41PUE(1)	CN40PUE(2)	CN39PUE(2)	CN38PUE(2)	CN37PUE(2)	CN36PUE(2)	CN35PUE(2)	CN34PUE(2)	CN33PUE(2)	CN32PUE	0000
CNPU4	0074	CN63PUE	CN62PUE	CN61PUE	CN60PUE	CN59PUE	CN58PUE	CN57PUE	CN56PUE	CN55PUE	CN54PUE	CN53PUE	CN52PUE	CN51PUE	CN50PUE	CN49PUE	CN48PUE(2)	0000
CNPU5	0076	CN79PUE(2)	CN78PUE(1)	CN77PUE(1)	CN76PUE(2)	CN75PUE(2)	CN74PUE(1)	CN73PUE	CN72PUE	CN71PUE	CN70PUE	CN69PUE	CN68PUE	CN67PUE(1)	CN66PUE(1)	CN65PUE	CN64PUE	0000
CNPU6	0078	—	—	—	—	—	—	—	—	—	—	—	CN84PUE	CN83PUE(1)	CN82PUE(2)	CN81PUE(2)	CN80PUE(2)	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These bits are unimplemented in 64-pin devices, read as '0'.

2: These bits are unimplemented in 64-pin and 80-pin devices, read as '0'.

6.6.2 PROGRAMMING A SINGLE WORD OF FLASH PROGRAM MEMORY

If a Flash location has been erased, it can be programmed using Table Write instructions to write an instruction word (24-bit) into the write latch. The TBLPAG register is loaded with the 8 Most Significant Bytes (MSBs) of the Flash address. The TBLWTL and TBLWTH instructions write the desired data into the write latches and specify the lower 16 bits of the program memory address to write to. To configure the NVMCON register for a word write, set the NVMOPx bits (NVMCON<3:0>) to '0011'. The write is performed by executing the unlock sequence and setting the WR bit (see Example 6-5). An equivalent procedure in 'C' compiler, using the MPLAB® C30 compiler and built-in hardware functions, is shown in Example 6-6.

EXAMPLE 6-5: PROGRAMMING A SINGLE WORD OF FLASH PROGRAM MEMORY

```
; Setup a pointer to data Program Memory
    MOV     #tblpage(PROG_ADDR), W0       ;
    MOV     W0, TBLPAG                    ;Initialize PM Page Boundary SFR
    MOV     #tbloffset(PROG_ADDR), W0     ;Initialize a register with program memory address

    MOV     #LOW_WORD_N, W2               ;
    MOV     #HIGH_BYTE_N, W3              ;
    TBLWTL  W2, [W0]                      ; Write PM low word into program latch
    TBLWTH  W3, [W0++]                    ; Write PM high byte into program latch

; Setup NVMCON for programming one word to data Program Memory
    MOV     #0x4003, W0                   ;
    MOV     W0, NVMCON                    ; Set NVMOP bits to 0011

    DISI    #5                            ; Disable interrupts while the KEY sequence is written
    MOV.B   #0x55, W0                     ; Write the key sequence
    MOV     W0, NVMKEY
    MOV.B   #0xAA, W0
    MOV     W0, NVMKEY
    BSET    NVMCON, #WR                   ; Start the write cycle
    NOP                                   ; Required delays
    NOP
```

EXAMPLE 6-6: PROGRAMMING A SINGLE WORD OF FLASH PROGRAM MEMORY ('C' LANGUAGE CODE)

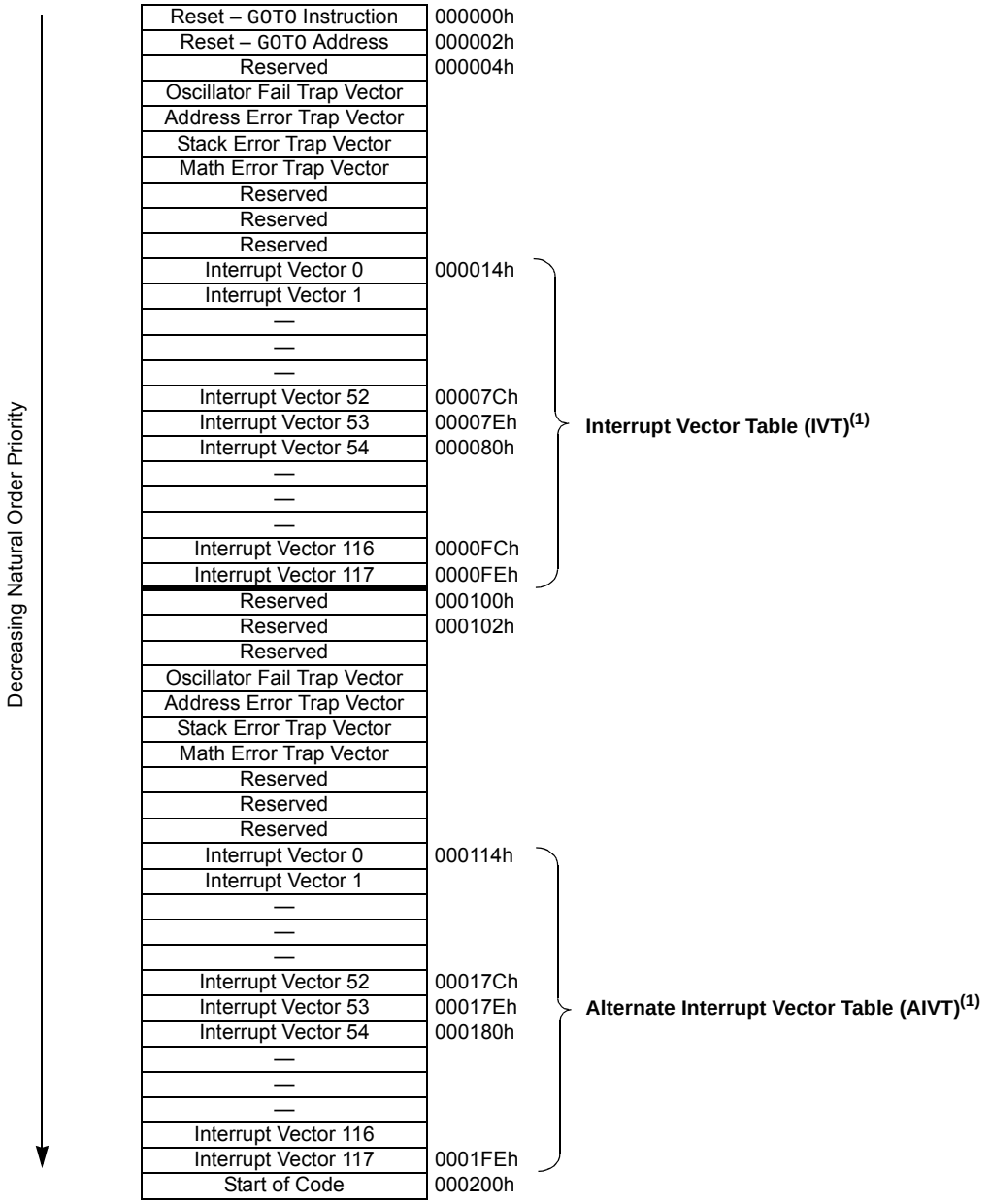
```
// C example using MPLAB C30
unsigned int offset;
unsigned long progAddr = 0xXXXXXX;          // Address of word to program
unsigned int progDataL = 0xXXXX;            // Data to program lower word
unsigned char progDataH = 0xXX;             // Data to program upper byte

//Set up NVMCON for word programming
NVMCON = 0x4003;                            // Initialize NVMCON

//Set up pointer to the first memory location to be written
TBLPAG = progAddr>>16;                      // Initialize PM Page Boundary SFR
offset = progAddr & 0xFFFF;                 // Initialize lower word of address

//Perform TBLWT instructions to write latches
__builtin_tblwtl(offset, progDataL);        // Write to address low word
__builtin_tblwth(offset, progDataH);        // Write to upper byte
asm("DISI #5");                             // Block interrupts with priority <7
                                            // for next 5 instructions
__builtin_write_NVM();                      // C30 function to perform unlock
                                            // sequence and set WR
```

FIGURE 8-1: PIC24F INTERRUPT VECTOR TABLE



Note 1: See Table 8-2 for the interrupt vector list.

TABLE 8-1: TRAP VECTOR DETAILS

Vector Number	IVT Address	AIVT Address	Trap Source
0	000004h	000104h	Reserved
1	000006h	000106h	Oscillator Failure
2	000008h	000108h	Address Error
3	00000Ah	00010Ah	Stack Error
4	00000Ch	00010Ch	Math Error
5	00000Eh	00010Eh	Reserved
6	000010h	000110h	Reserved
7	000012h	000112h	Reserved

REGISTER 8-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0 (CONTINUED)

bit 2 **OC1IF:** Output Compare Channel 1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **IC1IF:** Input Capture Channel 1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **INT0IF:** External Interrupt 0 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 8-11: IFS6: INTERRUPT FLAG STATUS REGISTER 6

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0
—	—	—	LCDIF	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4 **LCDIF:** LCD Controller Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3-0 **Unimplemented:** Read as '0'

REGISTER 8-12: IFS7: INTERRUPT FLAG STATUS REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	JTAGIF	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5 **JTAGIF:** JTAG Controller Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4-0 **Unimplemented:** Read as '0'

REGISTER 8-32: IPC11: INTERRUPT PRIORITY CONTROL REGISTER 11

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	DMA4IP2	DMA4IP1	DMA4IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	PMPIP2	PMPIP1	PMPIP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-8 **DMA4IP<2:0>:** DMA Channel 4 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **PMPIP<2:0>:** Parallel Master Port Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

REGISTER 8-39: IPC20: INTERRUPT PRIORITY CONTROL REGISTER 20

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U3TXIP2	U3TXIP1	U3TXIP0	—	U3RXIP2	U3RXIP1	U3RXIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	U3ERIP2	U3ERIP1	U3ERIP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **U3TXIP<2:0>:** UART3 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **U3RXIP<2:0>:** UART3 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **U3ERIP<2:0>:** UART3 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

11.4.3.1 Input Mapping

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral; that is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-7 through Register 11-26).

Each register contains two sets of 6-bit fields, with each set associated with one of the pin-selectable peripherals. Programming a given peripheral's bit field, with an appropriate 6-bit value, maps the RPn/RPIn pin with that value to that peripheral. For any given device, the valid range of values for any of the bit fields corresponds to the maximum number of Peripheral Pin Selections supported by the device.

TABLE 11-3: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)(1)

Input Name	Function Name	Register	Function Mapping Bits
DSM Modulation Input	MDMIN	RPINR30	MDMIR<5:0>
DSM Carrier 1 Input	MDCIN1	RPINR31	MDC1R<5:0>
DSM Carrier 2 Input	MDCIN2	RPINR31	MDC2R<5:0>
External Interrupt 1	INT1	RPINR0	INT1R<5:0>
External Interrupt 2	INT2	RPINR1	INT2R<5:0>
External Interrupt 3	INT3	RPINR1	INT3R<5:0>
External Interrupt 4	INT4	RPINR2	INT4R<5:0>
Input Capture 1	IC1	RPINR7	IC1R<5:0>
Input Capture 2	IC2	RPINR7	IC2R<5:0>
Input Capture 3	IC3	RPINR8	IC3R<5:0>
Input Capture 4	IC4	RPINR8	IC4R<5:0>
Input Capture 5	IC5	RPINR9	IC5R<5:0>
Input Capture 6	IC6	RPINR9	IC6R<5:0>
Input Capture 7	IC7	RPINR10	IC7R<5:0>
Output Compare Fault A	OCFA	RPINR11	OCFAR<5:0>
Output Compare Fault B	OCFB	RPINR11	OCFBR<5:0>
SPI1 Clock Input	SCK1IN	RPINR20	SCK1R<5:0>
SPI1 Data Input	SDI1	RPINR20	SDI1R<5:0>
SPI1 Slave Select Input	SS1IN	RPINR21	SS1R<5:0>
SPI2 Clock Input	SCK2IN	RPINR22	SCK2R<5:0>
SPI2 Data Input	SDI2	RPINR22	SDI2R<5:0>
SPI2 Slave Select Input	SS2IN	RPINR23	SS2R<5:0>
Timer1 External Clock	T1CK	RPINR23	T1CKR<5:0>
Timer2 External Clock	T2CK	RPINR3	T2CKR<5:0>
Timer3 External Clock	T3CK	RPINR3	T3CKR<5:0>
Timer4 External Clock	T4CK	RPINR4	T4CKR<5:0>
Timer5 External Clock	T5CK	RPINR4	T5CKR<5:0>
UART1 Clear-to-Send	$\overline{\text{U1CTS}}$	RPINR18	U1CTSR<5:0>
UART1 Receive	U1RX	RPINR18	U1RXR<5:0>
UART2 Clear-to-Send	$\overline{\text{U2CTS}}$	RPINR19	U2CTSR<5:0>
UART2 Receive	U2RX	RPINR19	U2RXR<5:0>
UART3 Clear-to-Send	$\overline{\text{U3CTS}}$	RPINR21	U3CTSR<5:0>
UART3 Receive	U3RX	RPINR17	U3RXR<5:0>
UART4 Clear-to-Send	$\overline{\text{U4CTS}}$	RPINR27	U4CTSR<5:0>
UART4 Receive	U4RX	RPINR27	U4RXR<5:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger (ST) input buffers.

REGISTER 11-17: RPINR17: PERIPHERAL PIN SELECT INPUT REGISTER 17

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	U3RXR5	U3RXR4	U3RXR3	U3RXR2	U3RXR1	U3RXR0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **U3RXR<5:0>:** Assign UART3 Receive (U3RX) to Corresponding RPn or RPIn Pin bits

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 11-18: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	U1CTSR5	U1CTSR4	U1CTSR3	U1CTSR2	U1CTSR1	U1CTSR0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	U1RXR5	U1RXR4	U1RXR3	U1RXR2	U1RXR1	U1RXR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **U1CTSR<5:0>:** Assign UART1 Clear-to-Send ($\overline{\text{U1CTS}}$) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **U1RXR<5:0>:** Assign UART1 Receive (U1RX) to Corresponding RPn or RPIn Pin bits

REGISTER 11-37: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP21R5	RP21R4	RP21R3	RP21R2	RP21R1	RP21R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP20R5	RP20R4	RP20R3	RP20R2	RP20R1	RP20R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP21R<5:0>:** RP21 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP21 (see Table 11-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP20R<5:0>:** RP20 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP20 (see Table 11-4 for peripheral function numbers).

REGISTER 11-38: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP23R5	RP23R4	RP23R3	RP23R2	RP23R1	RP23R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP22R5	RP22R4	RP22R3	RP22R2	RP22R1	RP22R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

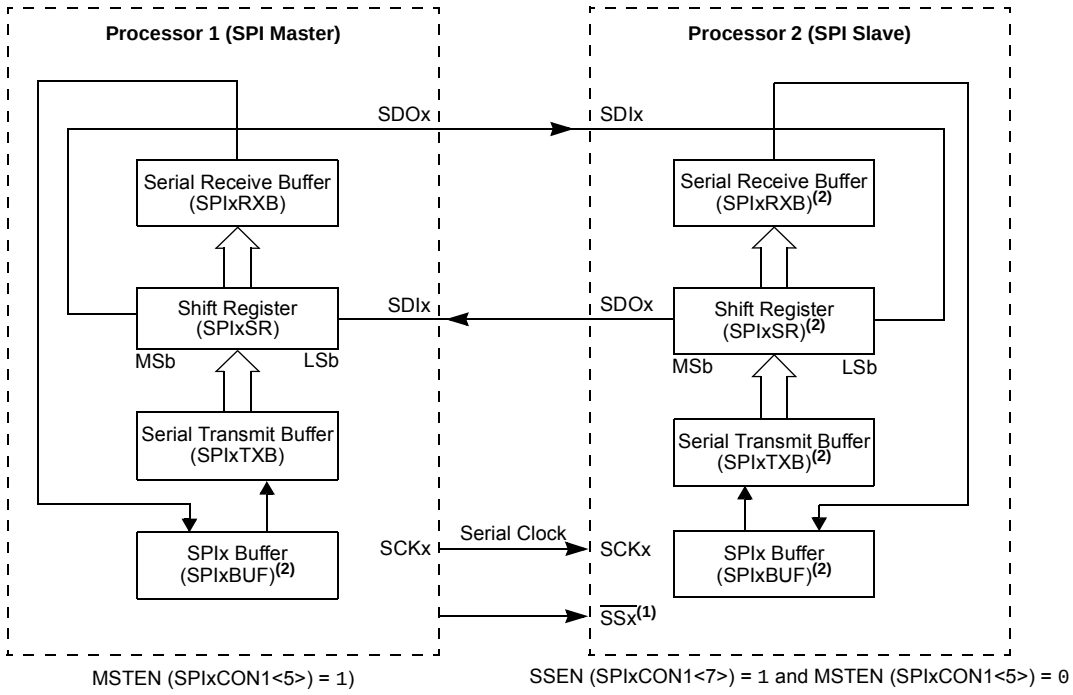
bit 13-8 **RP23R<5:0>:** RP23 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP23 (see Table 11-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP22R<5:0>:** RP22 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP22 (see Table 11-4 for peripheral function numbers).

NOTES:

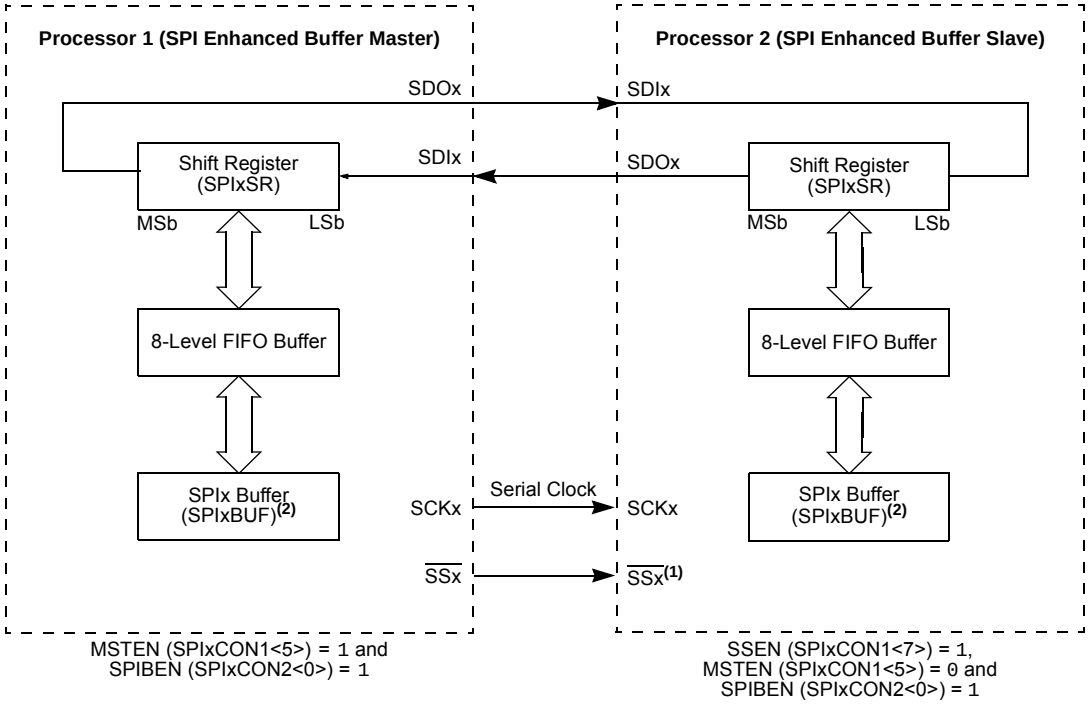
FIGURE 16-3: SPIx MASTER/SLAVE CONNECTION (STANDARD MODE)



Note 1: Using the $\overline{SSx}$ pin in Slave mode of operation is optional.

2: User must write transmit data to read the received data from SPIxBUF. The SPIxTXB and SPIxRXB registers are memory-mapped to SPIxBUF.

FIGURE 16-4: SPIx MASTER/SLAVE CONNECTION (ENHANCED BUFFER MODES)



Note 1: Using the $\overline{SSx}$ pin in Slave mode of operation is optional.

2: User must write transmit data to read the received data from SPIxBUF. The SPIxTXB and SPIxRXB registers are memory-mapped to SPIxBUF.

REGISTER 24-6: AD1CHS: ADC1 SAMPLE SELECT REGISTER (CONTINUED)

bit 7-5 **CH0NA<2:0>:** Sample A Channel 0 Negative Input Select bits
Same definitions as for CHONB<2:0>.

bit 4-0 **CH0SA<4:0>:** Sample A Channel 0 Positive Input Select bits
Same definitions as for CHOSB<4:0>.

Note 1: These input channels do not have corresponding memory-mapped result buffers.
2: These channels are implemented in 100-pin devices only.

REGISTER 24-7: ANCFG: ADC BAND GAP REFERENCE CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	VBG6EN	VBG2EN	VBGEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2 **VBG6EN:** ADC Input V_{BG}/6 Enable bit
1 = Band gap voltage, divided by six reference (V_{BG}/6), is enabled
0 = Band gap, divided by six reference (V_{BG}/6), is disabled

bit 1 **VBG2EN:** ADC Input V_{BG}/2 Enable bit
1 = Band gap voltage, divided by two reference (V_{BG}/2), is enabled
0 = Band gap, divided by two reference (V_{BG}/2), is disabled

bit 0 **VBGEN:** ADC Input V_{BG} Enable bit
1 = Band gap voltage reference (V_{BG}) is enabled
0 = Band gap reference (V_{BG}) is disabled

NOTES:

REGISTER 29-4: CW4: FLASH CONFIGURATION WORD 4

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

r-1	r-1	r-1	r-1	r-1	r-1	r-1	R/PO-1
r	r	r	r	r	r	r	DSSWEN
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
DSWDTEN	DSBOREN	DSWDTOSC	DSWDPS4	DSWDPS3	DSWDPS2	DSWDPS1	DSWDPS0
bit 7							bit 0

Legend:	r = Reserved bit	PO = Program once bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-16 **Unimplemented:** Read as ‘1’

bit 15-9 **Reserved:** Read as ‘1’

bit 8 **DSSWEN:** Deep Sleep Software Control Select bit
1 = Deep Sleep operation is enabled and controlled by the DSEN bit
0 = Deep Sleep operation is disabled

bit 7 **DSWDTEN:** Deep Sleep Watchdog Timer Enable bit
1 = Deep Sleep WDT is enabled
0 = Deep Sleep WDT is disabled

bit 6 **DSBOREN:** Deep Sleep Brown-out Reset Enable bit
1 = BOR is enabled in Deep Sleep mode
0 = BOR is disabled in Deep Sleep mode (remains active in other Sleep modes)

bit 5 **DSWDTOSC:** Deep Sleep Watchdog Timer Clock Select bit
1 = Clock source is LPRC
0 = Clock source is SOSC

TABLE 32-6: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Operating Temperature**	**VDD**	**Conditions**
Power-Down Current (I_{PD})						
DC60	—	—	µA	-40°C	2.0V	
	3.7	—	µA	+25°C		
	6.2	—	µA	+60°C		
	13.6	27.5	µA	+85°C		
	—	—	µA	-40°	3.3V	Sleep(2)
	3.8	—	µA	+25°C		
	6.3	—	µA	+60°C		
	13.7	28	µA	+85°C		
DC61	—	—	µA	-40°	2.0V	Low-Voltage Sleep(3)
	0.33	—	µA	+25°C		
	2	—	µA	+60°C		
	7.7	14.5	µA	+85°C		
	—	—	µA	-40°	3.3V	
	0.34	—	µA	+25°C		
	2	—	µA	+60°C		
	7.9	15	µA	+85°C		
DC70	—	—	µA	-40°	2.0V	Deep Sleep
	0.01	—	µA	+25°C		
	—	—	µA	+60°C		
	—	1.1	µA	+85°C		
	—	—	µA	-40°	3.3V	
	0.04	—	µA	+25°C		
	—	—	µA	+60°C		
	—	1.4	µA	+85°C		
	0.4	2.0	µA	-40°C to +85°C	0V	RTCC with VBAT mode (LPRC/SOSC)(4)

Note 1: Data in the Typical column is at 3.3V, +25°C unless otherwise stated. I_{PD} is measured with all peripherals and clocks (PMD) shutdown; all the ports are made output and driven low.

2: The retention low-voltage regulator is disabled; RETEN (RCON<12>) = 0, $\overline{\text{LPCFG}}$ (CW1<10>) = 1.

3: The retention low-voltage regulator is enabled; RETEN (RCON<12>) = 1, $\overline{\text{LPCFG}}$ (CW1<10>) = 0.

4: The VBAT pin is connected to the battery and RTCC is running with VDD = 0.

TABLE 32-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
	VOL	**Output Low Voltage**					
DO10		I/O Ports	—	—	0.4	V	IOL = 6.6 mA, VDD = 3.6V
			—	—	0.4	V	IOL = 5.0 mA, VDD = 2V
DO16		OSCO/CLKO	—	—	0.4	V	IOL = 6.6 mA, VDD = 3.6V
			—	—	0.4	V	IOL = 5.0 mA, VDD = 2V
	VOH	**Output High Voltage**					
DO20		I/O Ports	3.0	—	—	V	IOH = -3.0 mA, VDD = 3.6V
			2.4	—	—	V	IOH = -6.0 mA, VDD = 3.6V
			1.65	—	—	V	IOH = -1.0 mA, VDD = 2V
			1.4	—	—	V	IOH = -3.0 mA, VDD = 2V
DO26		OSCO/CLKO	2.4	—	—	V	IOH = -6.0 mA, VDD = 3.6V
			1.4	—	—	V	IOH = -1.0 mA, VDD = 2V

Note 1: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 32-10: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
		Program Flash Memory					
D130	EP	Cell Endurance	10000	—	—	E/W	-40°C to +85°C
D131	VPR	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D132B		VDD for Self-Timed Write	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D133A	TIW	Self-Timed Word Write Cycle Time	—	20	—	µs	
		Self-Timed Row Write Cycle Time	—	1.5	—	ms	
D133B	TIE	Self-Timed Page Erase Time	20	—	40	ms	
D134	TRETD	Characteristic Retention	20	—	—	Year	If no other specifications are violated
D135	IDDP	Supply Current during Programming	—	16	—	mA	

Note 1: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated.

32.2 AC Characteristics and Timing Parameters

The information contained in this section defines the PIC24FJ128GA310 family AC characteristics and timing parameters.

TABLE 32-17: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 2V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial Operating voltage VDD range as described in **Section 32.1 "DC Characteristics"**.

FIGURE 32-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

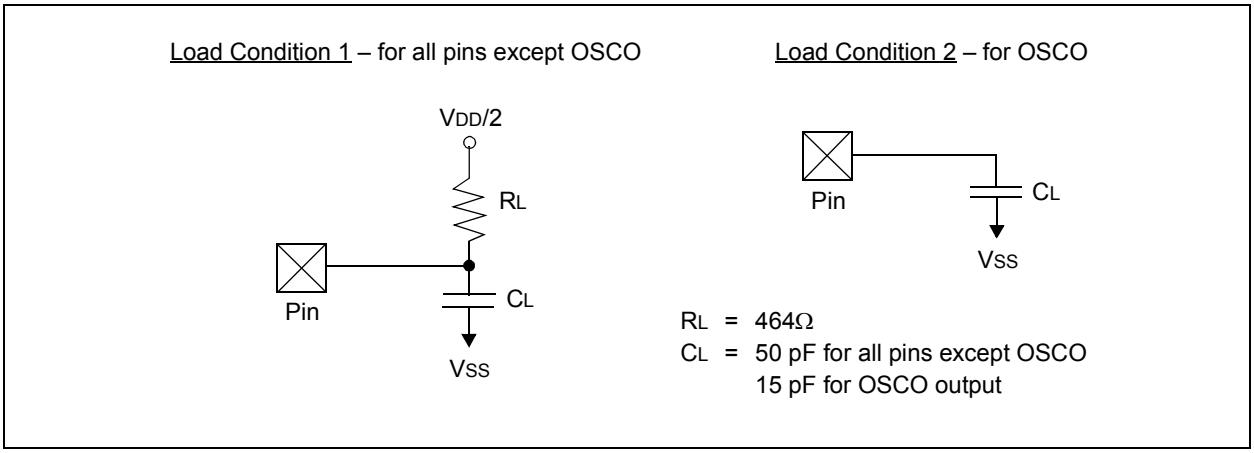


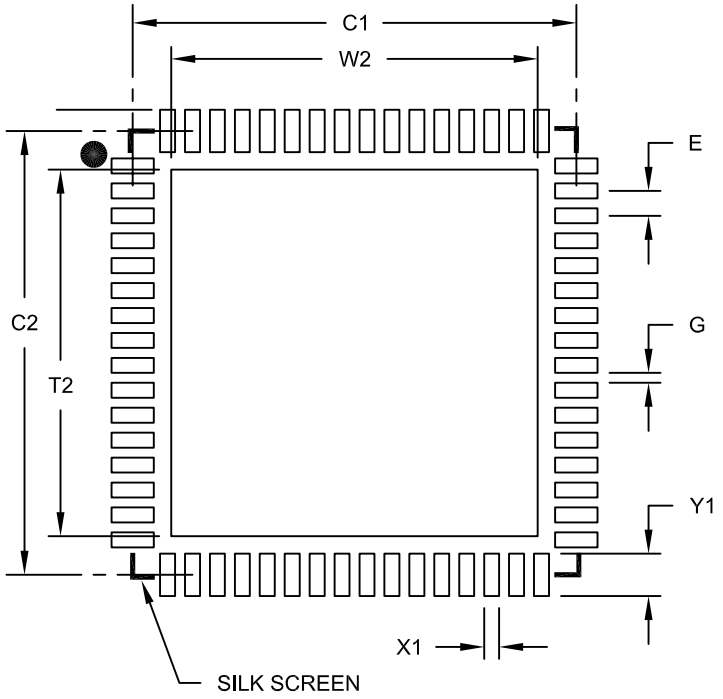
TABLE 32-18: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
DO50	COSCO	OSCO/CLKO Pin	—	—	15	pF	In XT and HS modes when external clock is used to drive OSCI
DO56	CIO	All I/O Pins and OSCO	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^2C™ mode

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			7.35
Optional Center Pad Length	T2			7.35
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2149A