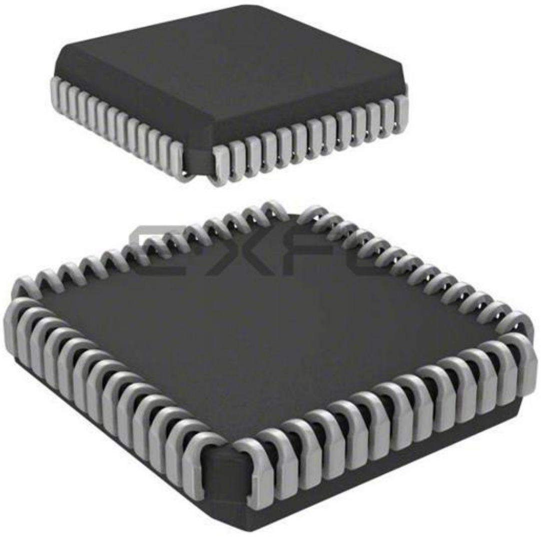
NXP USA Inc. - MC68HC11A1CFNE3 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	3MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	38
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	512 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LCC (J-Lead)
Supplier Device Package	52-PLCC (19.1x19.1)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc11a1cfne3

2.1.4 E Clock Output (E)

This is the output connection for the internally generated E clock which can be used as a timing reference. The frequency of the E clock output is actually one fourth that of the input frequency at the XTAL and EXTAL pins. When the E clock output is low an internal process is taking place and, when high, data is being accessed. The E clock signal is halted when the MCU is in STOP mode.

2.1.5 Interrupt Request ($\overline{\text{IRQ}}$)

The $\overline{\text{IRQ}}$ input provides a means for requesting asynchronous interrupts to the MC68HC11A8. It is program selectable (OPTION register) with a choice of either negative edge-sensitive or level-sensitive triggering, and is always configured to level-sensitive triggering by reset. The $\overline{\text{IRQ}}$ pin requires an external pull-up resistor to V_{DD} (typically 4.7K ohm).

2.1.6 Non-Maskable Interrupt ($\overline{\text{XIRQ}}$)

This input provides a means for requesting a non-maskable interrupt, after reset initialization. During reset, the X bit in the condition code register is set and any interrupt is masked until MCU software enables it. The $\overline{\text{XIRQ}}$ input is level sensitive and requires an external pull-up resistor to V_{DD}.

2.1.7 Mode A/Load Instruction Register and Mode B/Standby Voltage (MODA/$\overline{\text{LIR}}$, MODB/V_{STBY})

During reset, MODA and MODB are used to select one of the four operating modes. Refer to **Table 2-1**. Paragraph **2.2 Operating Modes** provides additional information.

Table 2-1 Operating Modes vs. MODA and MODB

MODB	MODA	Mode Selected
1	0	Single Chip
1	1	Expanded Multiplexed
0	0	Special Bootstrap
0	1	Special Test

After the operating mode has been selected, the $\overline{\text{LIR}}$ pin provides an open-drain output to indicate that an instruction is starting. All instructions are made up of a series of E clock cycles. The $\overline{\text{LIR}}$ signal goes low during the first E clock cycle of each instruction (opcode fetch). This output is provided as an aid in program debugging.

The V_{STBY} signal is used as the input for RAM standby power. When the voltage on this pin is more than one MOS threshold (about 0.7 volts) above the V_{DD} voltage, the internal 256-byte RAM and part of the reset logic are powered from this signal rather than the V_{DD} input. This allows RAM contents to be retained without V_{DD} power applied to the MCU. Reset must be driven low before V_{DD} is removed and must remain low until V_{DD} has been restored to a valid level.

2.1.11.1 Port A

Port A may be configured for: three input capture functions (IC1, IC2, IC3), four output compare functions (OC2, OC3, OC4, OC5), and either a pulse accumulator input (PAI) or a fifth output compare function (OC1). Refer to **8.1 Programmable Timer** for additional information.

Any port A pin that is not used for its alternate timer function may be used as a general-purpose input or output line.

2.1.11.2 Port B

While in single-chip operating modes, all of the port B pins are general-purpose output pins. During MCU reads of this port, the level sensed at the input side of the port B output drivers is read. Port B may also be used in a simple strobed output mode where an output pulse appears at the STRB signal each time data is written to port B.

When in expanded multiplexed operating modes, all of the port B pins act as high order address output signals. During each MCU cycle, bits 8 through 15 of the address are output on the PB0-PB7 lines respectively.

2.1.11.3 Port C

While in single-chip operating modes, all port C pins are general-purpose input/output pins. Port C inputs can be latched by providing an input transition to the STRA signal. Port C may also be used in full handshake modes of parallel I/O where the STRA input and STRB output act as handshake control lines.

When in expanded multiplexed operating modes, all port C pins are configured as multiplexed address/data signals. During the address portion of each MCU cycle, bits 0 through 7 of the address are output on the PC0-PC7 lines. During the data portion of each MCU cycle (E high), pins 0 through 7 are bidirectional data signals (D0-D7). The direction of data at the port C pins is indicated by the R/$\overline{\text{W}}$ signal.

2.1.11.4 Port D

Port D pins 0-5 may be used for general-purpose I/O signals. Port D pins alternately serve as the serial communications interface (SCI) and serial peripheral interface (SPI) signals when those subsystems are enabled.

Pin PD0 is the receive data input (RxD) signal for the serial communication interface (SCI).

Pin PD1 is the transmit data output (TxD) signal for the SCI.

Pins PD2 through PD5 are dedicated to the SPI. PD2 is the master-in-slave-out (MISO) signal. PD3 is the master-out-slave-in (MOSI) signal. PD4 is the serial clock (SCK) signal and PD5 is the slave select ($\overline{\text{SS}}$) input.

3 ON-CHIP MEMORY

This section describes the on-chip ROM, RAM, and EEPROM memories. The memory maps for each mode of operation are shown and the RAM and I/O mapping register (INIT) is described. The INIT register allows the on-chip RAM and the 64 control registers to be moved to suit the needs of a particular application.

3.1 Memory Maps

Composite memory maps for each mode of operation are shown in **Figure 3-1**. Memory locations are shown in the shaded areas and the contents of these shaded areas are shown to the right. These modes include single-chip, expanded multiplexed, special bootstrap, and special test.

Single-chip operating modes do not generate external addresses. Refer to **Table 3-1** for a full list of the registers.

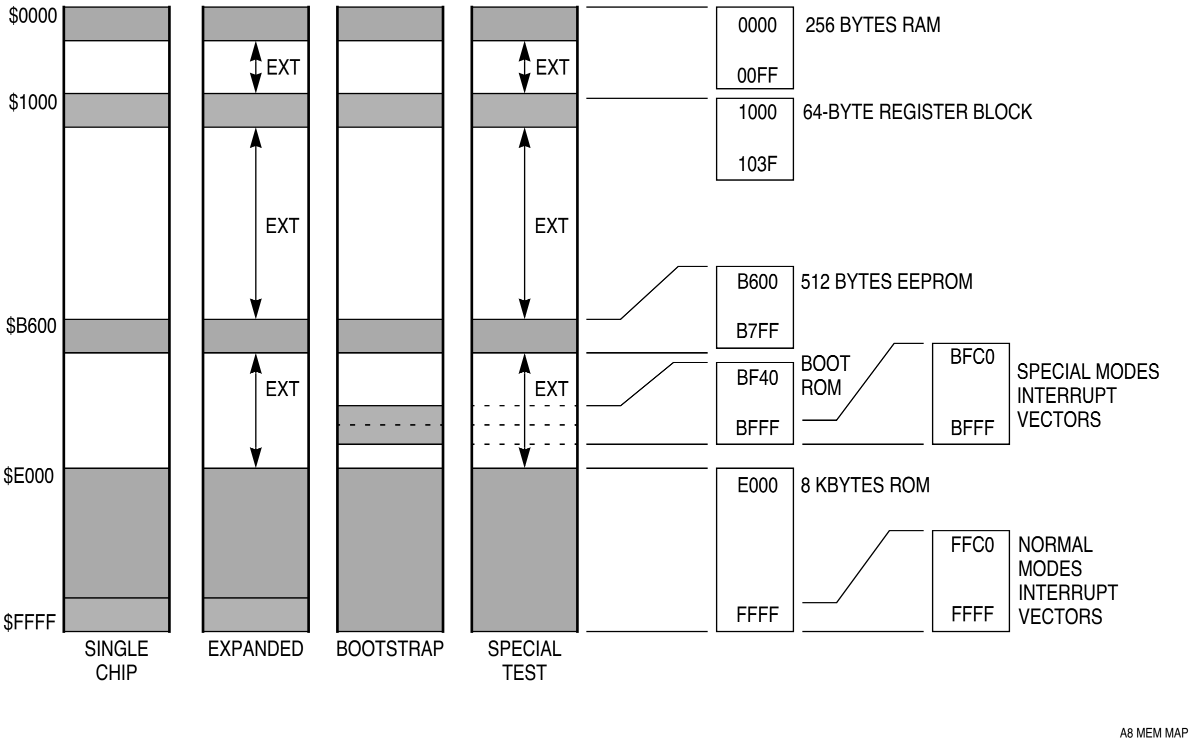


Figure 3-1 Memory Maps

Table 3-1 Register and Control Bit Assignments (Sheet 1 of 2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$1000	Bit 7	—	—	—	—	—	—	Bit 0	PORTA	I/O Port A
$1001									Reserved	
$1002	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC	Parallel I/O Control Register
$1003	Bit 7	—	—	—	—	—	—	Bit 0	PORTC	I/O Port C
$1004	Bit 7	—	—	—	—	—	—	Bit 0	PORTB	Output Port B
$1005	Bit 7	—	—	—	—	—	—	Bit 0	PORTCL	Alternate Latched Port C
$1006									Reserved	
$1007	Bit 7	—	—	—	—	—	—	Bit 0	DDRC	Data Direction for Port C
$1008			Bit 5	—	—	—	—	Bit 0	PORTD	I/O Port D
$1009			Bit 5	—	—	—	—	Bit 0	DDRD	Data Direction for Port D
$100A	Bit 7	—	—	—	—	—	—	Bit 0	PORTE	Input Port E
$100B	FOC1	FOC2	FOC3	FOC4	FOC5				CFORC	Compare Force Register
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3				OC1M	OC1 Action Mask Register
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3				OC1D	OC1 Action Data Register
$100E	Bit 15	—	—	—	—	—	—	Bit 8	TCNT	Timer Counter Register
$100F	Bit 7	—	—	—	—	—	—	Bit 0		
$1010	Bit 15	—	—	—	—	—	—	Bit 8	TIC1	Input Capture 1 Register
$1011	Bit 7	—	—	—	—	—	—	Bit 0		
$1012	Bit 15	—	—	—	—	—	—	Bit 8	TIC2	Input Capture 2 Register
$1013	Bit 7	—	—	—	—	—	—	Bit 0		
$1014	Bit 15	—	—	—	—	—	—	Bit 8	TIC3	Input Capture 3 Register
$1015	Bit 7	—	—	—	—	—	—	Bit 0		
$1016	Bit 15	—	—	—	—	—	—	Bit 8	TOC1	Output Compare 1 Register
$1017	Bit 7	—	—	—	—	—	—	Bit 0		
$1018	Bit 15	—	—	—	—	—	—	Bit 8	TOC2	Output Compare 2 Register
$1019	Bit 7	—	—	—	—	—	—	Bit 0		
$101A	Bit 15	—	—	—	—	—	—	Bit 8	TOC3	Output Compare 3 Register
$101B	Bit 7	—	—	—	—	—	—	Bit 0		
$101C	Bit 15	—	—	—	—	—	—	Bit 8	TOC4	Output Compare 4 Register
$101D	Bit 7	—	—	—	—	—	—	Bit 0		
$101E	Bit 15	—	—	—	—	—	—	Bit 8	TCO5	Output Compare 5 Register
$101F	Bit 7	—	—	—	—	—	—	Bit 0		

Table 3-1 Register and Control Bit Assignments (Sheet 2 of 2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1	Timer Control Register 1
$1021			EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2	Timer Control Register 2
$1022	OC1I	OC2I	OC3I	OC4I	OC5I	IC1I	IC2I	IC3I	TMSK1	Timer Interrupt Mask Register 1
$1023	OC1F	OC2F	OC3F	OC4F	OC5F	IC1F	IC2F	IC3F	TFLG1	Timer Interrupt Flag Register 1
$1024	TOI	RTII	PAOVI	PAII			PR1	PR0	TMSK2	Timer Interrupt Mask Register 2
$1025	TOF	RTIF	PAOVF	PAIF					TFLG2	Timer Interrupt Flag Register 2
$1026	DDRA7	PAEN	PAMOD	PEDGE			RTR1	RTR0	PACTL	Pulse Accumulator Control Register
$1027	Bit 7	—	—	—	—	—	—	Bit 0	PACNT	Pulse Accumulator Count Register
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR	SPI Control Register
$1029	SPIF	WCOL		MODF					SPSR	SPI Status Register
$102A	Bit 7	—	—	—	—	—	—	Bit 0	SPDR	SPI Data Register
$102B	TCLR		SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD	SCI Baud Rate Control
$102C	R8	T8		M	WAKE				SCCR1	SCI Control Register 1
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2	SCI Control Register 2
$102E	TRDE	TC	RDRF	IDLE	OR	NF	FE		SCSR	SCI Status Register
$102F	Bit 7	—	—	—	—	—	—	Bit 0	SCDR	SCI Data (Read RDR, Write TDR)
$1030	CCF		SCAN	MULT	CD	CC	CB	CA	ADCTL	A/D Control Register
$1031	Bit 7	—	—	—	—	—	—	Bit 0	ADR1	A/D Result Register 1
$1032	Bit 7	—	—	—	—	—	—	Bit 0	ADR2	A/D Result Register 2
$1033	Bit 7	—	—	—	—	—	—	Bit 0	ADR3	A/D Result Register 3
$1034	Bit 7	—	—	—	—	—	—	Bit 0	ADR4	A/D Result Register 4
$1035 thru $1038									Reserved	
$1039	ADPU	CSEL	IRQE	DLY	CME		CR1	CR0	OPTION	System Configuration Options
$103A	Bit 7	—	—	—	—	—	—	Bit 0	COPRST	Arm/Reset COP Timer Circuitry
$103B	ODD	EVEN		BYTE	ROW	ERASE	EELAT	EEPGM	PPROG	EEPROM Program Control Register
$103C	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO	Highest Priority I-Bit Int and Misc
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT	RAM and I/O Mapping Register
$103E	TILOP		OCCR	CBYP	DISR	FCM	FCOP	TCON	TEST1	Factory TEST Control Register
$103F	—	—	—	—	NOSEC	NOCOP	ROMON	EEON	CONFIG	COP, ROM, and EEPROM Enables

The erased state of an EEPROM byte is $FF. Programming changes ones to zeros. If any bit in a location needs to be changed from a zero to a one, the byte must be erased in a separate operation before it is reprogrammed. If a new data byte has no ones in bit positions which were already programmed to zero, it is acceptable to program the new data without erasing the EEPROM byte first. For example, programming $50 to a location which was already $55 would change the location to $50.

Programming and erasure of the EEPROM relies on an internal high-voltage charge pump. At E clock frequencies below 2 MHz the efficiency of this charge pump decreases which increases the time required to program or erase a location. The recommended program and erase time is 10 milliseconds when the E clock is 2 MHz and should be increased to as much as 20 milliseconds when E is between 1 MHz and 2 MHz. When the E clock is below 1 MHz, the clock source for the charge pump should be switched from the system clock to an on-chip R-C oscillator clock. This is done by setting the CSEL bit in the OPTION register. A 10 millisecond period should be allowed after setting the CSEL bit to allow the charge pump to stabilize. Note that the CSEL bit also controls a clock to the analog-to-digital converter subsystem.

3.5.1 EEPROM Programming Control Register (PPROG)

This 8-bit register is used to control programming and erasure of the 512-byte EEPROM. Reset clears this register so the EEPROM is configured for normal reads.

	7	6	5	4	3	2	1	0	
$103B	ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM	PPROG
RESET	0	0	0	0	0	0	0	0	

ODD — Program Odd Rows (TEST)

EVEN — Program Even Rows (TEST)

Bit 5 — Not implemented.
This bit always reads zero.

BYTE — Byte Erase Select
This bit overrides the ROW bit.
0 = Row or Bulk Erase
1 = Erase Only One Byte

ROW — Row Erase Select
If the BYTE bit is 1, ROW has no meaning.
0 = Bulk Erase
1 = Row Erase

ERASE — Erase Mode Select
0 = Normal Read or Program
1 = Erase Mode

EELAT — EEPROM Latch Control
0 = EEPROM Address and Data Configured for Read Mode
1 = EEPROM Address and Data Configured for Programming/Erasing

EEPGM — EEPROM Programming Voltage Enable
0 = Programming Voltage Switched Off
1 = Programming Voltage Turned On

If an attempt is made to set both the EELAT and EEPGM bits in the same write cycle, neither will be set. If a write to an EEPROM address is performed while the EEPGM bit is set, the write is ignored and the programming operation currently in progress is not disturbed. These two safeguards were included to prevent accidental EEPROM changes in cases of program runaway. Mask sets A38P, A49N, and date codes before 86xx did not have these safeguards.

3.5.2 Programming/Erasing Internal EEPROM

The EEPROM programming and erasure process is controlled by the PPROG register. The following paragraphs describe the various operations performed on the EEPROM and include example program segments to demonstrate programming and erase operations.

These program segments are intended to be simple straightforward examples of the sequences needed for basic program and erase operations. There are no special restrictions on the address modes used and bit manipulation instructions may be used. Other MCU operations can continue to be performed during EEPROM programming and erasure provided these operations do not include reads of data from EEPROM (the EEPROM is disconnected from the read data bus during EEPROM program and erase operations). The subroutine DLY10 used in these program segments is not shown but can be any set of instructions which takes ten milliseconds.

3.5.2.1 Read

For the read operation the EELAT bit in the PPROG register must be clear. When this bit is cleared, the remaining bits in the PPROG register have no meaning or effect, and the EEPROM may be read as if it were a normal ROM.

3.5.2.2 Programming

During EEPROM programming, the ROW and BYTE bits are not used. If the E clock frequency is 1 MHz or less, the CSEL bit in the OPTION register must be set. Recall that in this EEPROM, zeros must be erased by a separate erase operation before programming. The following program segment demonstrates how to program an EEPROM byte.

On mask set B96D and newer, the CONFIG register may only be programmed or erased while the MCU is operating in the test mode or the bootstrap mode. This interlock was added to help prevent accidental changes to the CONFIG register.

The following program segment demonstrates how to program the CONFIG register. This program assumes that the CONFIG register was previously erased.

```
*On entry, A = data to be programmed onto CONFIG
         •
         •
         •
PROGC  LDAB  #$02
       STAB  $103B  Set EELAT Bit (EEPGM = 0)
       STAA  $103F  Store Data to CONFIG Address
       LDAB  #$03
       STAB  $103B  Turn on Programming Voltage
       JSR   DLY10  Delay 10 ms
       CLR   $103B  Turn Off High Voltage and Set to READ
                    Mode
         •
         •
         •
```

The following program segment demonstrates the erase procedure for the CONFIG register.

```
         •
         •
         •
BULKC  LDAB  #$06
       STAB  $103B  Set Bulk Erase Mode
       STAB  $103F  Write any Data to CONFIG
       LDAB  #$07
       STAB  $103B  Turn on Programming Voltage
       JSR   DLY10  Delay 10 ms
       CLR   $103B  Turn Off High Voltage and Set to READ
                    Mode
         •
         •
         •
```

3.5.3.2 Operation of the Configuration Mechanism

The CONFIG register consists of an EEPROM byte and static working latches. This register controls the start-up configuration of the MCU. The contents of the EEPROM CONFIG byte are transferred into static working latches during any reset sequence. The operation of the MCU is controlled directly by these latches and not the actual EEPROM byte. Changes to the EEPROM byte do not affect operation of the MCU until after the next reset sequence. When programming the CONFIG register, the EEPROM byte is being accessed. When the CONFIG register is being read, the static latches are being accessed.

To change the value in the CONFIG register proceed as follows:

1. Erase the CONFIG register.

CAUTION

Do not issue a reset at this time.

2. Program the new value to the CONFIG register.
3. Issue a reset so the new configuration will take effect.

4.4.1 Input Handshake Protocol

In the input handshake protocol, port C is a latching input port, STRA is an edge-sensitive latch command from the external system that is driving port C, and STRB is a "ready" output line controlled by logic in the MCU.

When a "ready" condition is recognized, the external device places data on the port C lines, then pulses the STRA line. The active edge on the STRA line latches the port C data into the PORTCL register, sets the STAF flag (optionally causing an interrupt), and deasserts the STRB line. Deassertion of the STRB line automatically inhibits the external device from strobing new data into port C. Reading the PORTCL latch register (independent of clearing the STAF flag) asserts the STRB line, indicating that new data may now be applied to port C.

The STRB line can be configured (with the PLS control bit) to be a pulse output (pulse mode) or a static output (interlocked mode).

The port C data direction register bits should be cleared for each line that is to be used as a latched input line. However, some port C lines can be used as latched inputs with the input handshake protocol while, at the same time, using some port C lines as static inputs, and some port C lines as static outputs. The input handshake protocol has no effect on the use of port C lines as static inputs or as static outputs. Reads of the PORTC data register always return the static logic level at the port C lines (for lines configured as inputs). Writes to either the PORTC data register or the alternate latched port C register (PORTCL) send information to the same port C output register without affecting the input handshake strobes.

4.4.2 Output Handshake Protocol

In the output handshake protocol, port C is an output port, STRB is a "ready" output, and STRA is an edge-sensitive acknowledge input signal, used to indicate to the MCU that the output data has been accepted by the external device. In a variation of this output handshake protocol, STRA is also used as an output-enable input, as well as an edge-sensitive acknowledge input.

The MCU places data on the port C output lines and then indicates stable data is available by asserting the STRB line. The external device then processes the available data and pulses the STRA line to indicate that new data may be placed on the port C output lines. The active edge on the STRA line causes the STRB line to be deasserted and the STAF status flag to be set. In response to the STAF bit being set, the program transfers new data out of port C as required. Writing data to the PORTCL register causes the data to appear on port C lines and asserts the STRB line.

There is a variation to the output handshake protocol that allows three-state operation on port C. It is possible to directly connect this 8-bit parallel port to other three-state devices with no additional parts.

While the STRA input line is inactive, all port C lines obey the data direction specified by the data direction register so that lines which are configured as inputs are high impedance. When the STRA line is activated, all port C lines are forced to outputs regardless of the data in the data direction register. Note that in output handshake

WCOL — Write Collision

The write collision bit is set when an attempt is made to write to the serial peripheral data register while data transfer is taking place. If CPHA is zero a transfer is said to begin when $\overline{SS}$ goes low and the transfer ends when $\overline{SS}$ goes high after eight clock cycles on SCK. When CPHA is one a transfer is said to begin the first time SCK becomes active while $\overline{SS}$ is low and the transfer ends when the SPIF flag gets set. Clearing the WCOL bit is accomplished by reading the SPSR (with WCOL set) followed by an access to SPDR.

Bit 5 — Not Implemented

This bit always reads zero.

MODF — Mode Fault

The mode fault flag indicates that there may have been a multi-master conflict for system control and allows a proper exit from system operation to a reset or default system state. The MODF bit is normally clear, and is set only when the master device has its $\overline{SS}$ pin pulled low. Setting the MODF bit affects the internal serial peripheral interface system in the following ways:

1. An SPI interrupt is generated if SPIE = 1.
2. The SPE bit is cleared. This disables the SPI.
3. The MSTR bit is cleared, thus forcing the device into the slave mode.
4. DDRD bits for the four SPI pins are forced to zeros.

Clearing the MODF bit is accomplished by reading the SPSR (with MODF set), followed by a write to the SPCR. Control bits SPE and MSTR may be restored by user software to their original state after the MODF bit has been cleared. It is also necessary to restore DDRD after a mode fault.

Bits 3-0 — Not Implemented

These bits always read zero.

6.4.3 Serial Peripheral Data I/O Register (SPDR)

The serial peripheral data I/O register is used to transmit and receive data on the serial bus. Only a write to this register will initiate transmission/reception of another byte, and this will only occur in the master device. At the completion of transmitting a byte of data, the SPIF status bit is set in both the master and slave devices.

When the user reads the serial peripheral data I/O register, a buffer is actually being read. The first SPIF must be cleared by the time a second transfer of data from the shift register to the read buffer is initiated or an overrun condition will exist. In cases of overrun the byte which causes the overrun is lost.

A write to the serial peripheral data I/O register is not buffered and places data directly into the shift register for transmission.

8 PROGRAMMABLE TIMER, RTI, AND PULSE ACCUMULATOR

This section describes the 16-bit programmable timer, the real time interrupt, and the pulse accumulator system.

8.1 Programmable Timer

The timer has a single 16-bit free-running counter which is clocked by the output of a four-stage prescaler (divide by 1, 4, 8, or 16), which is in turn driven by the MCU E clock. Input functions are called input captures. These input captures record the count from the free-running counter in response to a detected edge on an input line. Output functions, called output compares, cause an output action when there is a match between a 16-bit output-compare register and the free-running counter. This timer system has three input capture registers and five output compare registers.

8.1.1 Counter

The key element in the timer system is a 16-bit free-running counter, or timer counter register. After reset, the MCU is configured to use the E clock as the input to the free-running counter. Initialization software may optionally reconfigure the system to use one of the three prescaler values. The prescaler control bits can only be written once during the first 64 cycles after a reset. Software can read the counter at any time without affecting its value because it is clocked and read during opposite phases of the E clock.

A counter read should first address the most significant byte. An MPU read of this address causes the least significant byte to be transferred to a buffer. This buffer is not affected by reset and is accessed when reading the least significant byte of the counter. For double byte read instructions, the two accesses occur on consecutive bus cycles.

The counter is cleared to $0000 during reset and is a read-only register with one exception. In test modes only, any MPU write to the most significant byte presets the counter to $FFF8 regardless of the value involved in the write.

When the count changes from $FFFF to $0000, the timer overflow flag (TOF) bit is set in timer interrupt flag register 2 (TFLG2). An interrupt can be enabled by setting the interrupt enable bit (TOI) in timer interrupt mask register 2 (TMSK2).

8.1.2 Input Capture

The input capture registers are 16-bit read-only registers which are not affected by reset and are used to latch the value of the counter when a defined transition is sensed by the corresponding input capture edge detector. The level transition which triggers counter transfer is defined by the corresponding input edge bits (EDGxB, EDGxA) in TCTL2.

Register OC1M is used to specify the bits of port A (I/O and timer port) which are to be affected as a result of a successful OC1 compare. Register OC1D is used to specify the data which is to be stored to the affected bits of port A as the result of a successful OC1 compare. If an OC1 compare and another output compare occur during the same E cycle and both attempt to alter the same port A line, the OC1 compare prevails.

This function allows control of multiple l/O pins automatically with a single output compare.

Another intended use for the special l/O pin control on output compare 1 is to allow more than one output compare to control a single l/O pin. This allows pulses as short as one E clock cycle to be generated.

8.1.5 Timer Compare Force Register (CFORC)

The timer compare force register is used to force early output compare actions. The CFORC register is an 8-bit write-only register. Reads of this location have no meaning and always return logic zeros. Note that the compare force function is not generally recommended for use with the output toggle function because a normal compare occurring immediately before or after the force may result in undesirable operation.

	7	6	5	4	3	2	1	0	
$**1**00B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0	CFORC
RESET	0	0	0	0	0	0	0	0	

FOC1-FOC5 — Force Output Compare x Action

0 = Has no meaning

1 = Causes action programmed for output compare x, except the OCxF flag bit is not set.

Bits 2-0 — Not Implemented

These bits always read zero.

8.1.6 Output Compare 1 Mask Register (OC1M)

This register is used in conjunction with output compare 1 to specify the bits of port A which are affected as a result of a successful OC1 compare.

	7	6	5	4	3	2	1	0	
$**1**00C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0	OC1M
RESET	0	0	0	0	0	0	0	0	

The bits of the OC1M register correspond bit-for-bit with the lines of port A (lines 7 through 3 only). For each bit that is affected by the successful compare, the corresponding bit in OC1M should be set to one.

PAMOD — Pulse Accumulator Mode
0 = External event counting
1 = Gated time accumulation

PEDGE — Pulse Accumulator Edge Control

This bit has different meanings depending on the state of the PAMOD bit.

PAMOD	PEDGE	Action on Clock
0	0	PAI Falling Edge Increments the Counter
0	1	PAI Rising Edge Increments the Counter
1	0	A zero on PAI Inhibits Counting
1	1	A one on PAI Inhibits Counting

Bits 3-2 — Not Implemented

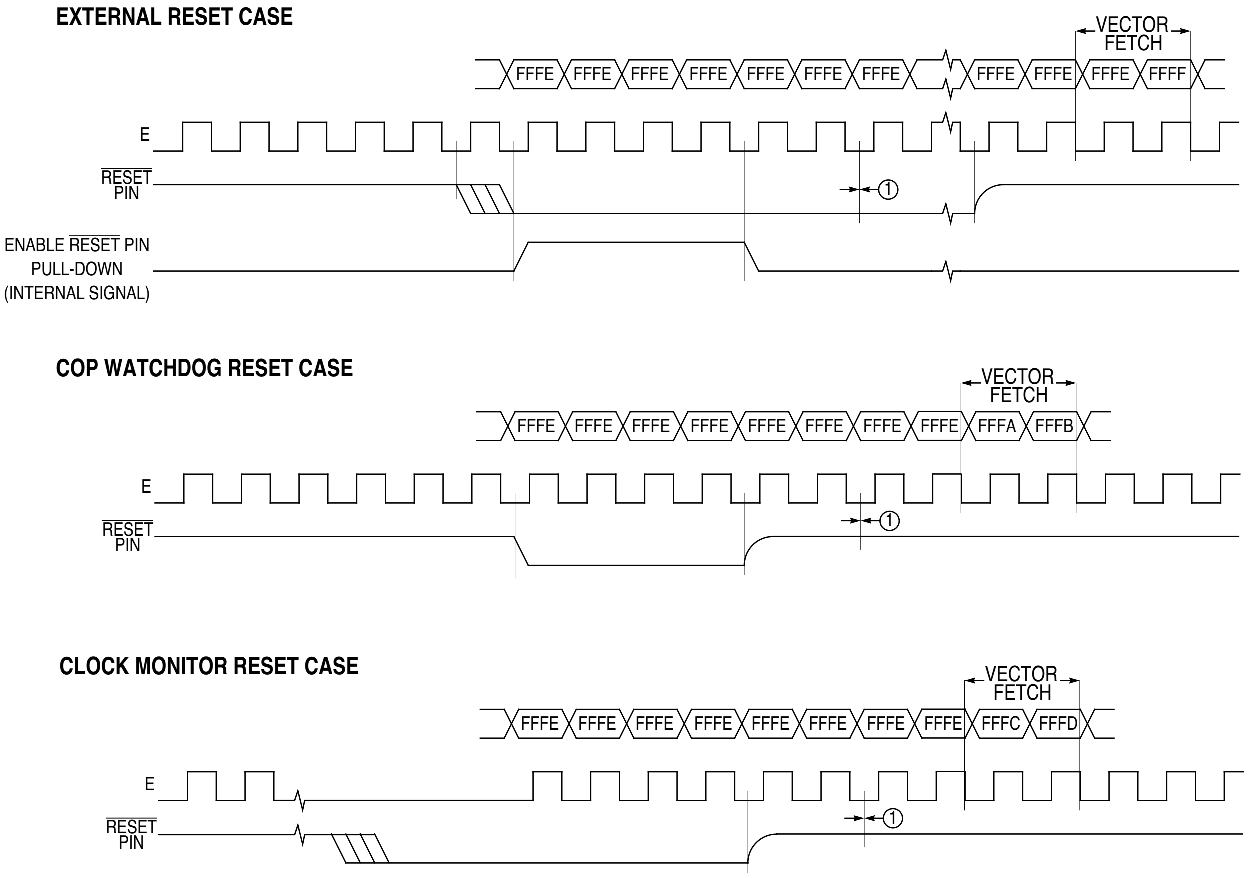
These bits always read zero.

RTR1 and RTR0 — RTI Interrupt Rate Selects

These two bits select one of four rates for the real time periodic interrupt circuit (see **Table 8-1**). Reset clears these two bits and after reset, a full RTI period elapses before the first RTI interrupt.

Table 8-1 Real Time Interrupt Rate versus RTR1 and RTR0

RTR1	RTR0	Rate	XTAL = 12.0 MHz	XTAL = 2^{23}	XTAL = 8.0 MHz	XTAL = 4.9152 MHz	XTAL = 4.0 MHz	XTAL = 3.6864 MHz
0	0	$2^{13} \div E$	8.192 ms	3.91 ms	4.10 ms	6.67 ms	8.19 ms	8.89 ms
0	1	$2^{14} \div E$	16.384 ms	7.81 ms	8.19 ms	13.33 ms	16.38 ms	17.78 ms
1	0	$2^{15} \div E$	32.768 ms	15.62 ms	16.38 ms	26.67 ms	32.77 ms	35.56 ms
1	1	$2^{16} \div E$	65.536 ms	31.25 ms	32.77 ms	53.33 ms	65.54 ms	71.11 ms
		E =	**3.0 MHz**	**2.1 MHz**	**2.0 MHz**	**1.2288 MHz**	**1.0 MHz**	**921.6 kHz**



① RESET PIN SAMPLED AT THIS TIME. LOW LEVEL INDICATES EXTERNAL RESET. HIGH LEVEL INDICATES CLOCK MONITOR OR COP SYSTEM RESET.

Figure 9-1 Reset Timing

supply voltage. The power-on circuitry provides a 4064 cycle time delay from the time of the first oscillator operation. In a system where E = 2 MHz, power on reset lasts about 2 milliseconds. If the external $\overline{\text{RESET}}$ pin is low at the end of the power-on delay time, the MCU remains in the reset condition until the $\overline{\text{RESET}}$ pin goes high.

9.1.2.1 CPU

After reset the CPU fetches the restart vector from locations $FFFE and $FFFF ($BFFE and $BFFF if in special bootstrap or special test operating mode) during the first three cycles, and begins executing instructions. The stack pointer and other CPU registers are indeterminate immediately after reset; however, the X and I interrupt mask bits in the condition code register are set to mask any interrupt requests. Also, the S bit in the condition code register is set to disable the STOP mode.

10.2.7 Prebyte

In order to expand the number of instructions used in the MC68HC11A8, a prebyte instruction has been added to certain instructions. The instructions affected are usually associated with index register Y. The instruction opcodes which do not require a prebyte could be considered as page 1 of the overall opcode map. The remaining opcodes could be considered as pages 2, 3, and 4 of the opcode map and would require a prebyte; $18 for page 2, $1A for page 3, and $CD for page 4.

10.3 Instruction Set

The central processing unit (CPU) in the MC68HC11A8 is basically a proper extension of the MC6801 CPU. In addition to its ability to execute all M6800 and M6801 instructions, the MC68HC11A8 CPU has a paged operation code (opcode) map with a total of 91 new opcodes. Major functional additions include a second 16-bit index register (Y register), two types of 16-by-16 divide instructions, STOP and WAIT instructions, and bit manipulation instructions.

Table 10-1 shows all MC68HC11A8 instructions in all possible addressing modes. For each instruction, the operand construction is shown as well as the total number of machine code bytes and execution time in CPU E-clock cycles. Notes are provided at the end of **Table 10-1** which explain the letters in the Operand and Execution Time columns for some instructions. Definitions of “Special Ops” found in the Boolean Expression column are found in **Figure 10-2**.

Table 10-2 through **Table 10-8** provide a detailed description of the information present on the address bus, data bus, and the read/write (R/$\overline{\text{W}}$) line during each cycle of each instruction. The information is useful in comparing actual with expected results during debug of both software and hardware as the program is executed. The information is categorized in groups according to addressing mode and number of cycles per instruction. In general, instructions with the same address mode and number of cycles execute in the same manner. Exceptions are indicated in the table.

Table 10-5 Cycle-by-Cycle Operation — Extended Mode (Sheet 1 of 2)

Reference Number*	Address Mode and Instructions	Cycles	Cycle #	Address Bus	R/$\overline{W}$ Line	Data Bus
5-1	JMP	3	1 2 3	Opcode Address Opcode Address + 1 Opcode Address + 2	1 1 1	Opcode ($7E) Jump Address (High Byte) Jump Address (Low Byte)
5-2	ADCA, ADCB, ADDA, ADDB, ANDA, ANDB, BITA, BITB, CMPA, CMPB, EORA, EORB, LDAA, LDAB, ORAA ORAB, SBCA, SBCB, SUBA, SUBB	4	1 2 3 4	Opcode Address Opcode Address + 1 Opcode Address + 2 Operand Address	1 1 1 1	Opcode Operand Address (High Byte) Operand Address (Low Byte) Operand Data
5-3	STAA, STAB	4	1 2 3 4	Opcode Address Opcode Address + 1 Opcode Address + 2 Operand Address	1 1 1 0	Opcode Operand Address (High Byte) Operand Address (Low Byte) Accumulator Data
5-4	LDD, LDS, LDX	5	1 2 3 4 5	Opcode Address Opcode Address + 1 Opcode Address + 2 Operand Address Operand Address + 1	1 1 1 1 1	Opcode Operand Address (High Byte) Operand Address (Low Byte) Operand Data (High Byte) Operand Data (Low Byte)
5-5	STD, STS, STX	5	1 2 3 4 5	Opcode Address Opcode Address + 1 Opcode Address + 2 Operand Address Operand Address + 1	1 1 1 0 0	Opcode Operand Address (High Byte) Operand Address (Low Byte) Register Data (High Byte) Register Data (Low Byte)
5-6	LDY	6	1 2 3 4 5 6	Opcode Address Opcode Address + 1 Opcode Address + 2 Opcode Address + 3 Operand Address Operand Address + 1	1 1 1 1 1 1	Opcode (Page Select Byte) ($18) Opcode (Second Byte) ($FE) Operand Address (High Byte) Operand Address (Low Byte) Operand Data (High Byte) Operand Data (Low Byte)
5-7	STY	6	1 2 3 4 5 6	Opcode Address Opcode Address + 1 Opcode Address + 2 Opcode Address + 3 Operand Address Operand Address + 1	1 1 1 1 0 0	Opcode (Page Select Byte) ($18) Opcode (Second Byte) ($FF) Operand Address (High Byte) Operand Address (Low Byte) Register Data (High Byte) Register Data (Low Byte)
5-8	ASL, ASR, CLR, COM, DEC, INC, LSL, LSR, NEG, ROL, ROR	6	1 2 3 4 5 6	Opcode Address Opcode Address + 1 Opcode Address + 2 Operand Address $FFFF Operand Address	1 1 1 1 1 0	Opcode Operand Address (High Byte) Operand Address (Low Byte) Original Operand Data Irrelevant Data Result Operand Data
5-9	TST	6	1 2 3 4 5 6	Opcode Address Opcode Address + 1 Opcode Address + 2 Operand Address $FFFF $FFFF	1 1 1 1 1 1	Opcode ($7D) Operand Address (High Byte) Operand Address (Low Byte) Original Operand Data Irrelevant Data Irrelevant Data
5-10	ADDD, CPX, SUBD	6	1 2 3 4 5 6	Opcode Address Opcode Address + 1 Opcode Address + 2 Operand Address Operand Address + 1 $FFFF	1 1 1 1 1 1	Opcode Operand Address (High Byte) Operand Address (Low Byte) Operand Data (High Byte) Operand Data (Low Byte) Irrelevant Data

*The reference number is given to provide a cross-reference to Table 10-1.

Table A-8 Serial Peripheral Interface (SPI) Timing

V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H

Num	Characteristic	Symbol	2.0 MHz		3.0 MHz		Unit
			Min	Max	Min	Max	
	Operating Frequency Master Slave	$f_{op(m)}$ $f_{op(s)}$	dc dc	0.5 2.0	dc dc	0.5 3.0	f_{op} MHz
1	Cycle Time Master Slave	$t_{cyc(m)}$ $t_{cyc(s)}$	2.0 500	— —	2.0 333	— —	t_{cyc} ns
2	Enable Lead Time Master (Note 2) Slave	$t_{lead(m)}$ $t_{lead(s)}$	— 250	— —	— 240	— —	ns ns
3	Enable Lag Time Master (Note 2) Slave	$t_{lag(m)}$ $t_{lag(s)}$	— 250	— —	— 240	— —	ns ns
4	Clock (SCK) High Time Master Slave	$t_{w(SCKH)m}$ $t_{w(SCKH)s}$	340 190	— —	227 127	— —	ns ns
5	Clock (SCK) Low Time Master Slave	$t_{w(SCKL)m}$ $t_{w(SCKL)s}$	340 190	— —	227 127	— —	ns ns
6	Data Setup Time (Inputs) Master Slave	$t_{su(m)}$ $t_{su(s)}$	100 100	— —	100 100	— —	ns ns
7	Data Hold Time (Inputs) Master Slave	$t_{h(m)}$ $t_{h(s)}$	100 100	— —	100 100	— —	ns ns
8	Access Time (Time to Data Active from High-Impedance State) Slave	t_a	0	120	0	120	ns
9	Disable Time (Hold Time to High-Impedance State) Slave	t_{dis}	—	240	—	167	ns
10	Data Valid (After Enable Edge)(Note 3)	$t_{v(s)}$	—	240	—	167	ns
11	Data Hold Time (Outputs) (After Enable Edge)	t_{ho}	0	—	0	—	ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, CL = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	t_{rm} t_{rs}	— —	100 2.0	— —	100 2.0	ns µs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	t_{fm} t_{fs}	— —	100 2.0	— —	100 2.0	ns µs

NOTES:

1. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Signal production depends on software.
3. Assumes 200 pF load on all SPI pins.