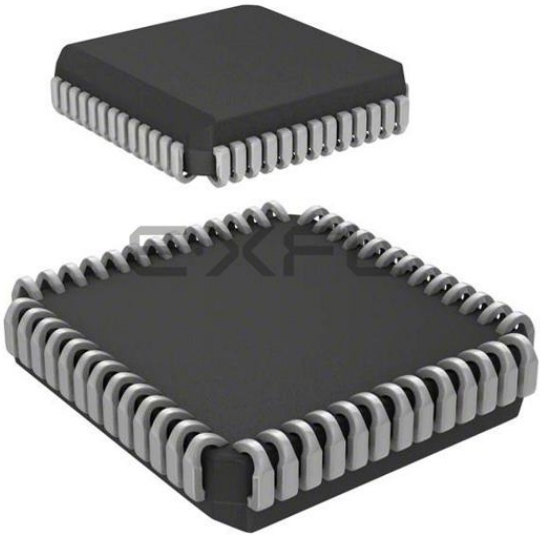

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Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	3MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	38
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	512 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LCC (J-Lead)
Supplier Device Package	52-PLCC (19.1x19.1)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc11a1mfne

10 CPU, ADDRESSING MODES, AND INSTRUCTION SET

A ELECTRICAL CHARACTERISTICS

2 SIGNAL DESCRIPTIONS AND OPERATING MODES

The signal descriptions and operating modes are presented in this section. When the microcontroller is in an expanded multiplexed operating mode, 18 pins change function to support a multiplexed address/data bus.

2.1 Signal Pin Descriptions

The following paragraphs provide a description of the input/output signals. Reference is made, where applicable, to other sections that contain more detail about the function being performed.

2.1.1 Input Power (V_{DD}) and Ground (V_{SS})

Power is supplied to the microcontroller using these pins. V_{DD} is the positive power input and V_{SS} is ground. Although the MC68HC11A8 is a CMOS device, very fast signal transitions are present on many of its pins. Short rise and fall times are present even when the microcontroller is operating at slow clock rates. Special care must be taken to provide good power supply bypassing at the MCU. Recommended bypassing would include a 0.1 µF ceramic capacitor between the V_{DD} and V_{SS} pins and physically adjacent to one of the two pins. A bulk capacitance, whose size depends on the other circuitry in the system, should also be present on the circuit board.

2.1.2 Reset ($\overline{\text{RESET}}$)

This active low bidirectional control signal is used as an input to initialize the MC68HC11A8 to a known start-up state, and as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or computer operating properly (COP) watchdog circuit. This reset signal is significantly different from the reset signal used on other Motorola MCUs. Please refer to **9 RESETS, INTERRUPTS, AND LOW POWER MODES** before designing circuitry to generate or monitor this signal.

2.1.3 Crystal Driver and External Clock Input (XTAL, EXTAL)

These two pins provide the interface for either a crystal or a CMOS compatible clock to control the internal clock generator circuitry. The frequency applied to these pins shall be four times higher than the desired E clock rate. The XTAL pin is normally left unterminated when using an external CMOS compatible clock input to the EXTAL pin. However, a 10K to 100K load resistor to ground may be used to reduce RFI noise emission. The XTAL output is normally intended to drive only a crystal.

The XTAL output may be buffered with a high-input-impedance buffer such as the 74HC04, or it may be used to drive the EXTAL input of another M68HC11.

In all cases take extra care in the circuit board layout around the oscillator pins. Load capacitances shown in the oscillator circuits include all stray layout capacitances. Refer to **Figure 2-1**, **Figure 2-2**, and **Figure 2-3** for diagrams of oscillator circuits.

If the part is not in security mode (or has completed the above erase sequence), a break character is output by the SCI transmitter. For normal use of the boot loader program, the user sends $FF to the SCI receiver at either E clock/16 (7812 baud for E clock = 2 MHz) or E clock/104 (1200 baud for E clock = 2 MHz).

NOTE

This $FF is not echoed through the SCI transmitter.

Now the user must download 256 bytes of program data to be put into RAM starting at location $0000. These characters are echoed through the transmitter. When loading is complete, the program jumps to location $0000 and begins executing that code.

If the SCI transmitter pin is to be used, an external pull-up resistor is required because port D pins are configured for wire-OR operation.

In special bootstrap operating mode the interrupt vectors are directed to RAM as shown in **Table 2-3**. This allows the user to use interrupts by way of a jump table. For example: to use the SWI interrupt, a jump instruction would be placed in RAM at locations $00F4, $00F5, and $00F6. When an SWI is encountered, the vector (which is in the boot loader ROM program) will direct program control to location $00F4 in RAM which in turn contains a JUMP instruction to the interrupt service routine.

Table 2-3 Bootstrap Mode Interrupt Vectors

Address	Vector
00C4	SCI
00C7	SPI
00CA	Pulse Accumulator Input Edge
00CD	Pulse Accumulator Overflow
00D0	Timer Overflow
00D3	Timer Output Compare 5
00D6	Timer Output Compare 4
00D9	Timer Output Compare 3
00DC	Timer Output Compare 2
00DF	Timer Output Compare 1
00E2	Timer Input Capture 3
00E5	Timer Input Capture 2
00E8	Timer Input Capture 1
00EB	Real Time Interrupt
00EE	IRQ
00F1	XIRQ
00F4	SWI
00F7	Illegal Opcode
00FA	COP Fail
00FD	Clock Monitor
BF40 (Boot)	Reset

EELAT — EEPROM Latch Control
0 = EEPROM Address and Data Configured for Read Mode
1 = EEPROM Address and Data Configured for Programming/Erasing

EEPGM — EEPROM Programming Voltage Enable
0 = Programming Voltage Switched Off
1 = Programming Voltage Turned On

If an attempt is made to set both the EELAT and EEPGM bits in the same write cycle, neither will be set. If a write to an EEPROM address is performed while the EEPGM bit is set, the write is ignored and the programming operation currently in progress is not disturbed. These two safeguards were included to prevent accidental EEPROM changes in cases of program runaway. Mask sets A38P, A49N, and date codes before 86xx did not have these safeguards.

3.5.2 Programming/Erasing Internal EEPROM

The EEPROM programming and erasure process is controlled by the PPROG register. The following paragraphs describe the various operations performed on the EEPROM and include example program segments to demonstrate programming and erase operations.

These program segments are intended to be simple straightforward examples of the sequences needed for basic program and erase operations. There are no special restrictions on the address modes used and bit manipulation instructions may be used. Other MCU operations can continue to be performed during EEPROM programming and erasure provided these operations do not include reads of data from EEPROM (the EEPROM is disconnected from the read data bus during EEPROM program and erase operations). The subroutine DLY10 used in these program segments is not shown but can be any set of instructions which takes ten milliseconds.

3.5.2.1 Read

For the read operation the EELAT bit in the PPROG register must be clear. When this bit is cleared, the remaining bits in the PPROG register have no meaning or effect, and the EEPROM may be read as if it were a normal ROM.

3.5.2.2 Programming

During EEPROM programming, the ROW and BYTE bits are not used. If the E clock frequency is 1 MHz or less, the CSEL bit in the OPTION register must be set. Recall that in this EEPROM, zeros must be erased by a separate erase operation before programming. The following program segment demonstrates how to program an EEPROM byte.

5 SERIAL COMMUNICATIONS INTERFACE

This section contains a description of the serial communication interface (SCI).

5.1 Overview and Features

A full-duplex asynchronous Serial Communications Interface (SCI) is provided with a standard NRZ format (one start bit, eight or nine data bits, and one stop bit) and a variety of baud rates. The SCI transmitter and receiver are functionally independent, but use the same data format and bit rate. “Baud” and “bit rate” are used synonymously in the following description.

5.1.1 SCI Two-Wire System Features

- Standard NRZ (mark/space) format.
- Advanced error detection method includes noise detection for noise duration of up to 1/16 bit time.
- Full-duplex operation.
- Software programmable for one of 32 different baud rates.
- Software selectable word length (eight or nine bit words).
- Separate transmitter and receiver enable bits.
- Capable of being interrupt driven.
- Four separate enable bits available for interrupt control.

5.1.2 SCI Receiver Features

- Receiver wake-up function (idle or address bit).
- Idle line detect.
- Framing error detect.
- Noise detect.
- Overrun detect.
- Receiver data register full flag.

5.1.3 SCI Transmitter Features

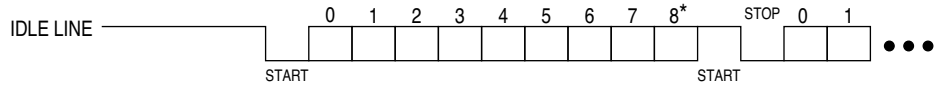
- Transmit data register empty flag.
- Transmit complete flag.
- Send break.

5.2 Data Format

Receive data or transmit data is the serial data which is transferred to the internal data bus from the receive data input pin (RxD), or from the internal bus to the transmit data output pin (TxD).

The non-return-to-zero (NRZ) data format shown in **Figure 5-1** is used and must meet the following criteria:

1. The idle line is brought to a logic one state prior to transmission/reception of a character.
2. A start bit (logic zero) is used to indicate the start of a frame.
3. The data is transmitted and received least-significant-bit first.
4. A stop bit (logic one) is used to indicate the end of a frame. A frame consists of a start bit, a character of eight or nine data bits, and a stop bit.
5. A break is defined as the transmission or reception of a low (logic zero) for at least one complete frame time.



* CONTROL BIT M IN SCCR1 SELECTS EITHER 8-BIT OR 9-BIT DATA.

SCI DATA FORMAT

Figure 5-1 Data Format

5.3 Wake-Up Feature

The receiver wake-up feature reduces SCI service overhead in multiple receiver systems. Software in each receiver evaluates the first character(s) of each message. If the message is intended for a different receiver, the SCI can be placed in a sleep mode so that the rest of the message will not generate requests for service. Whenever a new message is started, logic in the sleeping receivers causes them to wake up so they can evaluate the initial character(s) of the new message.

A sleeping SCI receiver can be configured (using the WAKE control bit in serial communications control register 1 (SCCR1)) to wake up using either of two methods: idle line wake up or address mark wake up.

In idle line wake up, a sleeping receiver wakes up as soon as the RxD line becomes idle. Idle is defined as a continuous logic high on the RxD line for ten (or eleven) full bit times. Systems using this type of wake up must provide at least one character time of idle between messages to wake up sleeping receivers but must not allow any idle time between characters within a message.

In address mark wake up, the most significant bit (MSB) in a character is used to indicate that the character is an address (1) or a data (0) character. Sleeping receivers will wake up whenever an address character is received. Systems using this method for wake up would set the MSB of the first character in each message and leave it clear for all other characters in the message. Idle periods may be present within messages and no idle time is required between messages for this wake up method.

5.4 Receive Data (RxD)

Receive data is the serial data which is applied through the input line and the serial communications interface to the internal bus. The receiver circuitry clocks the input at a rate equal to 16 times the baud rate and this time is referred to as the RT clock.

5.8.1 Serial Communications Data Register (SCDR)

The serial communications data register performs two functions; i.e., it acts as the receive data register when it is read and as the transmit data register when it is written. **Figure 5-6** shows this register as two separate registers, namely: the receive data register and the transmit data register.

NOTE

The divided frequencies shown in **Table 5-3** represent baud rates which are the highest transmit baud rate (Tx) that can be obtained by a specific crystal frequency and only using the prescaler division. Lower baud rates may be obtained by providing a further division using the SCI rate select bits as shown below for some representative prescaler outputs.

Table 5-4 Transmit Baud Rate Output for a Given Prescaler Output

SCR Bit			Divided By	Representative Highest Prescaler Baud Rate Output					
2	1	0		131.072 K Baud	32.768 K Baud	76.80 K Baud	19.20 K Baud	9600 Baud	4800 Baud
0	0	0	1	131.072 K Baud	32.768 K Baud	76.80 K Baud	19.20 K Baud	9600 Baud	4800 Baud
0	0	1	2	65.536 K Baud	16.384 K Baud	38.40 K Baud	9600 Baud	4800 Baud	2400 Baud
0	1	0	4	32.768 K Baud	8.192 K Baud	19.20 K Baud	4800 Baud	2400 Baud	1200 Baud
0	1	1	8	16.384 K Baud	4.096 K Baud	9600 Baud	2400 Baud	1200 Baud	600 Baud
1	0	0	16	8.192 K Baud	2.048 K Baud	4800 Baud	1200 Baud	600 Baud	300 Baud
1	0	1	32	4.096 K Baud	1.024 K Baud	2400 Baud	600 Baud	300 Baud	150 Baud
1	1	0	64	2.048 K Baud	512 Baud	1200 Baud	300 Baud	150 Baud	75 Baud
1	1	1	128	1.024 K Baud	256 Baud	600 Baud	150 Baud	75 Baud	—

NOTE

Table 5-4 illustrates how the SCI select bits can be used to provide lower transmitter baud rates by further dividing the prescaler output frequency. The five examples are only representative samples. In all cases, the baud rates shown are transmit baud rates (transmit clock) and the receiver clock is 16 times higher in frequency than the actual baud rate.

7.7 A/D Result Registers 1, 2, 3, and 4 (ADR1, ADR2, ADR3, and ADR4)

The A/D result registers are read-only registers used to hold an 8-bit conversion result. Writes to these registers have no effect. Data in the A/D result registers is valid when the CCF flag bit in the ADCTL register is set, indicating a conversion sequence is complete. If conversion results are needed sooner refer to **Figure 7-1**. For example the ADR1 result is valid 33 cycles after an ADCTL write. Refer to the A/D channel assignments in **Table 7-1** for the relationship between the channels and the result registers.

7.8 A/D Power-Up and Clock Select

A/D power-up is controlled by bit 7 (ADPU) of the OPTION register. When ADPU is cleared, power to the A/D system is disabled. When ADPU is set, the A/D system is enabled. A delay of as much as 100 microseconds is required after turning on the A/D converter to allow the analog bias voltages to stabilize.

Clock select is controlled by bit 6 (CSEL) of the OPTION register. When CSEL is cleared, the A/D system uses the system E clock. When CSEL is set, the A/D system uses an internal R-C clock source, which runs at about 1.5 MHz. The MCU E clock is not suitable to drive the A/D system if it is operating below 750 kHz, in which case the R-C internal clock should be selected. A delay of 10 ms is required after changing CSEL from zero to one to allow the R-C oscillator to start and internal bias voltages to settle. Refer to **9.1.5 Configuration Options Register (OPTION)** for additional information. Note that the CSEL control bit also enables a separate R-C oscillator to drive the EEPROM charge pump.

When the A/D system is operating with the MCU E clock, all switching and comparator operations are synchronized to the MCU clocks. This allows the comparator results to be sampled at quiet clock times to minimize noise errors. The internal R-C oscillator is asynchronous to the MCU clock so noise will affect A/D results more while CSEL = 1.

8 PROGRAMMABLE TIMER, RTI, AND PULSE ACCUMULATOR

This section describes the 16-bit programmable timer, the real time interrupt, and the pulse accumulator system.

8.1 Programmable Timer

The timer has a single 16-bit free-running counter which is clocked by the output of a four-stage prescaler (divide by 1, 4, 8, or 16), which is in turn driven by the MCU E clock. Input functions are called input captures. These input captures record the count from the free-running counter in response to a detected edge on an input line. Output functions, called output compares, cause an output action when there is a match between a 16-bit output-compare register and the free-running counter. This timer system has three input capture registers and five output compare registers.

8.1.1 Counter

The key element in the timer system is a 16-bit free-running counter, or timer counter register. After reset, the MCU is configured to use the E clock as the input to the free-running counter. Initialization software may optionally reconfigure the system to use one of the three prescaler values. The prescaler control bits can only be written once during the first 64 cycles after a reset. Software can read the counter at any time without affecting its value because it is clocked and read during opposite phases of the E clock.

A counter read should first address the most significant byte. An MPU read of this address causes the least significant byte to be transferred to a buffer. This buffer is not affected by reset and is accessed when reading the least significant byte of the counter. For double byte read instructions, the two accesses occur on consecutive bus cycles.

The counter is cleared to $0000 during reset and is a read-only register with one exception. In test modes only, any MPU write to the most significant byte presets the counter to $FFF8 regardless of the value involved in the write.

When the count changes from $FFFF to $0000, the timer overflow flag (TOF) bit is set in timer interrupt flag register 2 (TFLG2). An interrupt can be enabled by setting the interrupt enable bit (TOI) in timer interrupt mask register 2 (TMSK2).

8.1.2 Input Capture

The input capture registers are 16-bit read-only registers which are not affected by reset and are used to latch the value of the counter when a defined transition is sensed by the corresponding input capture edge detector. The level transition which triggers counter transfer is defined by the corresponding input edge bits (EDGxB, EDGxA) in TCTL2.

8.1.9 Timer Control Register 2 (TCTL2)

	7	6	5	4	3	2	1	0	
$1021	0	0	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
RESET	0	0	0	0	0	0	0	0	

Bits 7-6 — Not Implemented

These bits always read zero.

EDGxB and EDGxA — Input Capture x Edge Control.

These two bits (EDGxB and EDGxA) are cleared to zero by reset and are encoded to configure the input sensing logic for input capture x as follows:

EDGxB	EDBxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any (rising or falling) edge

8.1.10 Timer Interrupt Mask Register 1 (TMSK1)

	7	6	5	4	3	2	1	0	
$1022	OC1I	OC2I	OC3I	OC4I	OC5I	IC1I	IC2I	IC3I	TMSK1
RESET	0	0	0	0	0	0	0	0	

OCxl — Output Compare x Interrupt

If the OCxl enable bit is set when the OCxF flag bit is set, a hardware interrupt sequence is requested.

ICxl — Input Capture x Interrupt

If the ICxl enable bit is set when the ICxF flag bit is set, a hardware interrupt sequence is requested.

8.1.11 Timer Interrupt Flag Register 1 (TFLG1)

Timer interrupt flag register 1 is used to indicate the occurrence of timer system events, and together with the TMSK1 register allows the timer subsystem to operate in a polled or interrupt driven system. For each bit in TFLG1, there is a corresponding bit in TMSK1 in the same bit position. If the mask bit is set, each time the conditions for the corresponding flag are met, a hardware interrupt sequence is requested as well as the flag bit being set.

These timer system status flags are cleared by writing a one to the bit positions corresponding to the flag(s) which are to be cleared. Bit manipulation instructions would be inappropriate for flag clearing because they are read-modify-write instructions. Even though the instruction mask implies that the programmer is only interested in some of the bits in the manipulated location, the entire location is actually read and rewritten which may clear other bits in the register.

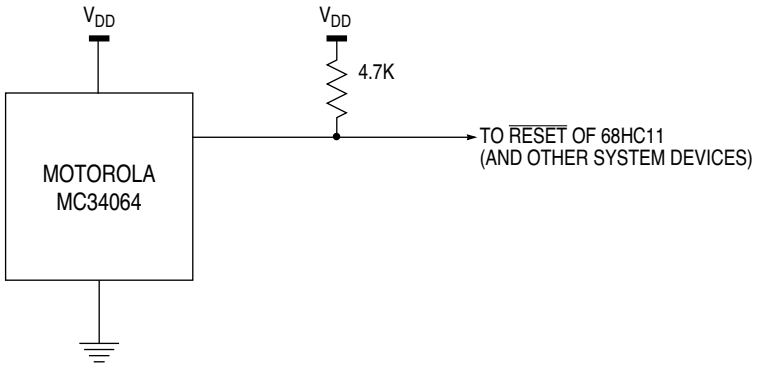


Figure 9-2 Simple LVI Reset Circuit

9.1.2.2 Memory Map

After reset, the INIT register is initialized to $01, putting the 256 bytes of RAM at locations $0000 through $00FF and the control registers at locations $1000 through $103F. The 8K-byte ROM and/or the 512-byte EEPROM may or may not be present in the memory map because the two bits that enable them in the CONFIG register are EEPROM cells and are not affected by reset or power down.

9.1.2.3 Parallel I/O

When a reset occurs in expanded multiplexed operating mode, the 18 pins used for parallel I/O are dedicated to the expansion bus. If a reset occurs in the single-chip operating mode, the STAF, STAI, and HNDS bits in the parallel input/output control register (PIOC) are cleared so that no interrupt is pending or enabled, and the simple strobed mode (rather than full handshake mode) of parallel I/O is selected. The CWOM bit in PIOC is cleared so port C is not in wired-OR mode. Port C is initialized as an input port (DDRC = $00), port B is a general purpose output port with all bits cleared. STRA is the edge-sensitive strobe A input and the active edge is initially configured to detect rising edges (EGA bit in the PIOC set), and STRB is the strobe B output and is initially a logic zero (the INVB bit in the PIOC is set). Port C, port D bits 0 through 5, port A bits 0, 1, 2, and 7, and port E are configured as general purpose high-impedance inputs. Port B and bits 3 through 6 of port A have their directions fixed as outputs and their reset state is a logic zero.

9.1.2.4 Timer

During reset, the timer system is initialized to a count of $0000. The prescaler bits are cleared, and all output compare registers are initialized to $FFFF. All input capture registers are indeterminate after reset. The output compare 1 mask (OC1M) register is cleared so that successful OC1 compares do not affect any I/O pins. The other four output compares are configured to not affect any I/O pins on successful compares. All three input capture edge-detector circuits are configured for “capture disabled” operation. The timer overflow interrupt flag and all eight timer function interrupt flags are cleared. All nine timer interrupts are disabled since their mask bits are cleared.

9.1.4 Clock Monitor Reset

The clock monitor function is enabled by the CME control bit in the OPTION register. When CME is clear, the monitor function is disabled. When the CME bit is set, the clock monitor function detects the absence of an E clock for more than a certain period of time. The timeout period is dependent on processing parameters and will be between 5 and 100 microseconds. This means that an E-clock rate of 200 kHz or more will never cause a clock monitor failure and an E-clock rate of 10 kHz or less will definitely cause a clock monitor failure. This implies that systems operating near or below an E-clock rate of 200 kHz should not use the clock monitor function.

Upon detection of a slow or absent clock, the clock monitor circuit will cause a system reset. This reset is issued to the external system via the bidirectional $\overline{\text{RESET}}$ pin. The clock monitor system has a separate reset vector.

Special considerations are needed when using a STOP function and clock monitor in the same system. Since the STOP function causes the clocks to be halted, the clock monitor function will generate a reset sequence if it is enabled at the time the STOP mode is entered.

The clock monitor is useful as a backup for the COP watchdog timer. Since the watchdog timer requires a clock to function, it will not indicate any failure if the system clocks fail. The clock monitor would detect such a failure and force the MCU to its reset state. Note that clocks are not required for the MCU to reach its reset configuration, although clocks are required to sequence through reset back to the run condition.

9.1.5 Configuration Options Register (OPTION)

This is a special purpose 8-bit register that is used (optionally) during initialization to configure internal system configuration options. With the exception of bits 7, 6, and 3 (ADPU, CSEL, and CME) which may be read or written at any time, this register may be written to only once after a reset and thereafter is a read-only register. If no write is performed to this location within 64 E-clock cycles after reset, then bits 5, 4, 1, and 0 (IRQE, DLY, CR1, and CR0) will become read-only to minimize the possibility of any accidental changes to the system configuration (writes will be ignored). While in special test modes, the protection mechanism on this register is preempted and all bits in the OPTION register may be written repeatedly.

	7	6	5	4	3	2	1	0	
$**1**039	ADPU	CSEL	IRQE	DLY	CME	0	CR1	CR0	OPTION
RESET	0	0	0	1	0	0	0	0	

ADPU — A/D Power-up

This bit controls operations of the on-chip analog-to-digital converter. When ADPU is clear, the A/D system is powered down and conversion requests will not return meaningful information. To use the A/D system, this bit should be set. A 100 microsecond delay is required after ADPU is turned on to allow the A/D system to stabilize.

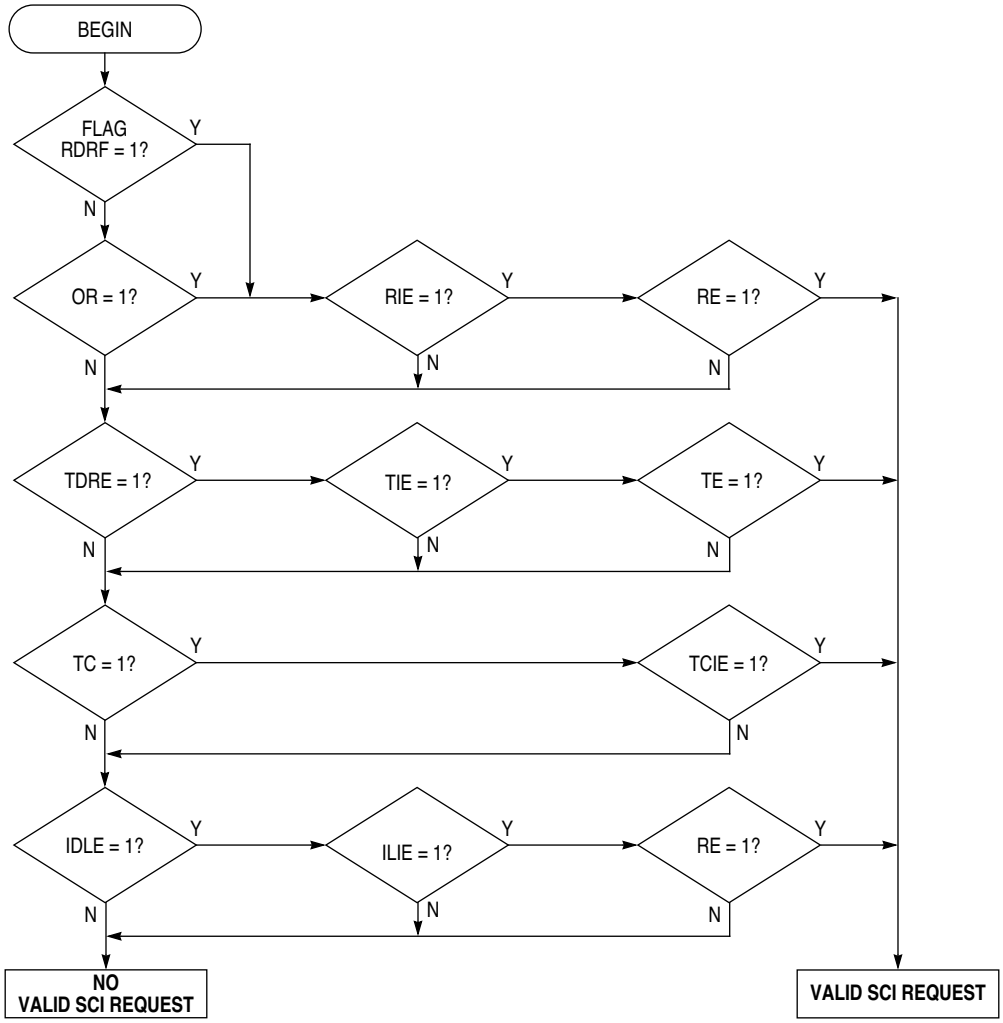
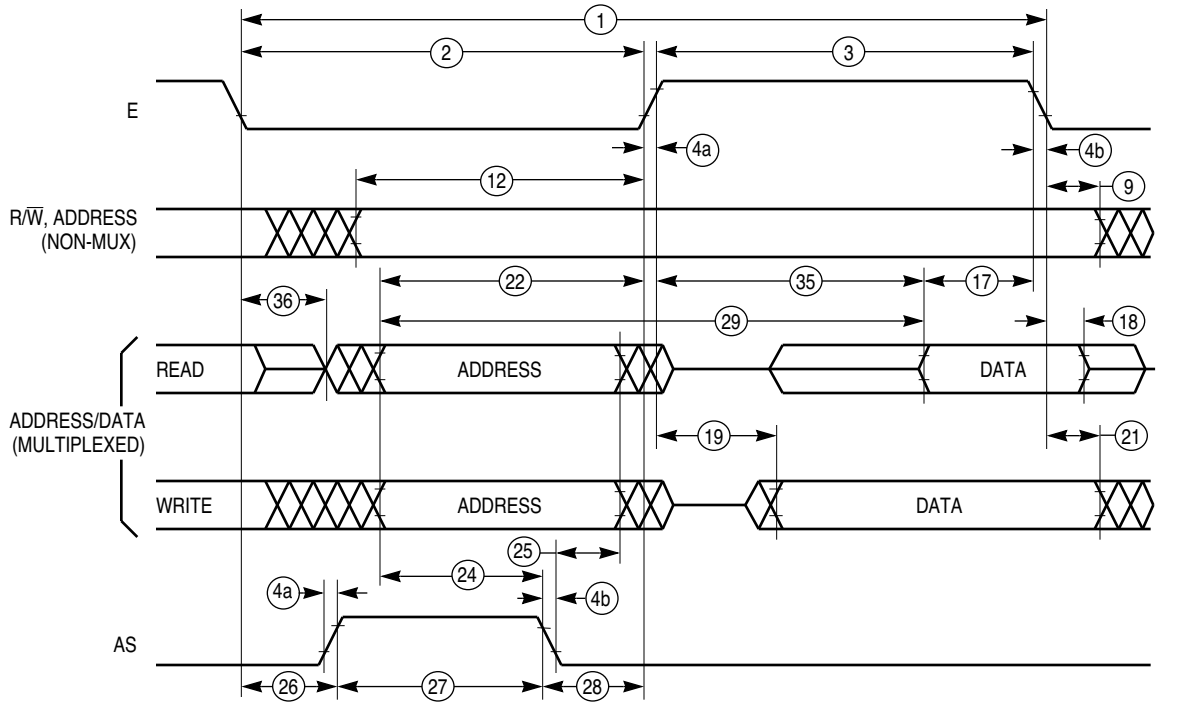


Figure 9-6 Interrupt Source Resolution Within SCI

Table 10-7 Cycle-by-Cycle Operation — Indexed Y Mode (Sheet 1 of 2)

Reference Number*	Address Mode and Instructions	Cycles	Cycle #	Address Bus	R/$\overline{W}$ Line	Data Bus
7-1	JMP	4	1	Opcode Address	1	Opcode (Page Select Byte) ($18)
			2	Opcode Address + 1	1	Opcode (Second Byte) ($6E)
			3	Opcode Address + 2	1	Index Offset
			4	$FFFF	1	Irrelevant Data
7-2	ADCA, ADCB, ADDA, ADDB, ANDA ANDB, BITA, BITB, CMPA, CMPB, EORA, EORB, LDAA, LDAB, ORAA, ORAB, SBCA, SBCB, SUBA, SUBB,	5	1	Opcode Address	1	Opcode (Page Select Byte) ($18)
			2	Opcode Address + 1	1	Opcode (Second Byte)
			3	Opcode Address + 2	1	Index Offset
			4	$FFFF	1	Irrelevant Data
			5	(IY) + Offset	1	Operand Data
7-3	ASL, ASR, CLR, COM, DEC, INC, LSL, LSR, NEG, ROL, ROR	7	1	Opcode Address	1	Opcode (Page Select Byte)
			2	Opcode Address + 1	1	Opcode (Second Byte)
			3	Opcode Address + 2	1	Index Offset
			4	$FFFF	1	Irrelevant Data
			5	(IY) + Offset	1	Original Operand Data
			6	$FFFF	1	Irrelevant Data
			7	(IY) + Offset	0	Result Operand Data
7-4	TST	7	1	Opcode Address	1	Opcode (Page Select Byte) ($18)
			2	Opcode Address + 1	1	Opcode (Second Byte) ($6D)
			3	Opcode Address + 2	1	Index Offset
			4	$FFFF	1	Irrelevant Data
			5	(IY) + Offset	1	Original Operand Data
			6	$FFFF	1	Irrelevant Data
			7	$FFFF	1	Irrelevant Data
7-5	STAA, STAB	5	1	Opcode Address	1	Opcode (Page Select Byte) ($18)
			2	Opcode Address + 1	1	Opcode (Second Byte)
			3	Opcode Address + 2	1	Index Offset
			4	$FFFF	1	Irrelevant Data
			5	(IY) + Offset	0	Accumulator Data
7-6	LDD, LDS, LDX, LDY	6	1	Opcode Address	1	Opcode (Page Select Byte)
			2	Opcode Address + 1	1	Opcode (Second Byte)
			3	Opcode Address + 2	1	Index Offset
			4	$FFFF	1	Irrelevant Data
			5	(IY) + Offset	1	Operand Data (High Byte)
			6	(IY) + Offset + 1	1	Operand Data (Low Byte)
7-7	STD, STS, STX, STY	6	1	Opcode Address	1	Opcode (Page Select Byte)
			2	Opcode Address + 1	1	Opcode (Second Byte)
			3	Opcode Address + 2	1	Index Offset
			4	$FFFF	1	Irrelevant Data
			5	(IY) + Offset	0	Register Data (High Byte)
			6	(IY) + Offset + 1	0	Register Data (Low Byte)
7-8	ADDD, CPD, CPX, CPY, SUBD	7	1	Opcode Address	1	Opcode (Page Select Byte)
			2	Opcode Address + 1	1	Opcode (Second Byte)
			3	Opcode Address + 2	1	Index Offset
			4	$FFFF	1	Irrelevant Data
			5	(IY) + Offset	1	Operand Data (High Byte)
			6	(IY) + Offset + 1	1	Operand Data (Low Byte)
			7	$FFFF	1	Irrelevant Data

* The reference number is given to provide a cross-reference to Table 10-1.



NOTE: Measurement points shown are 20% and 70% of V_{DD}.

MUX BUS TIM

Figure A-14 Multiplexed Expansion Bus Timing Diagram

A

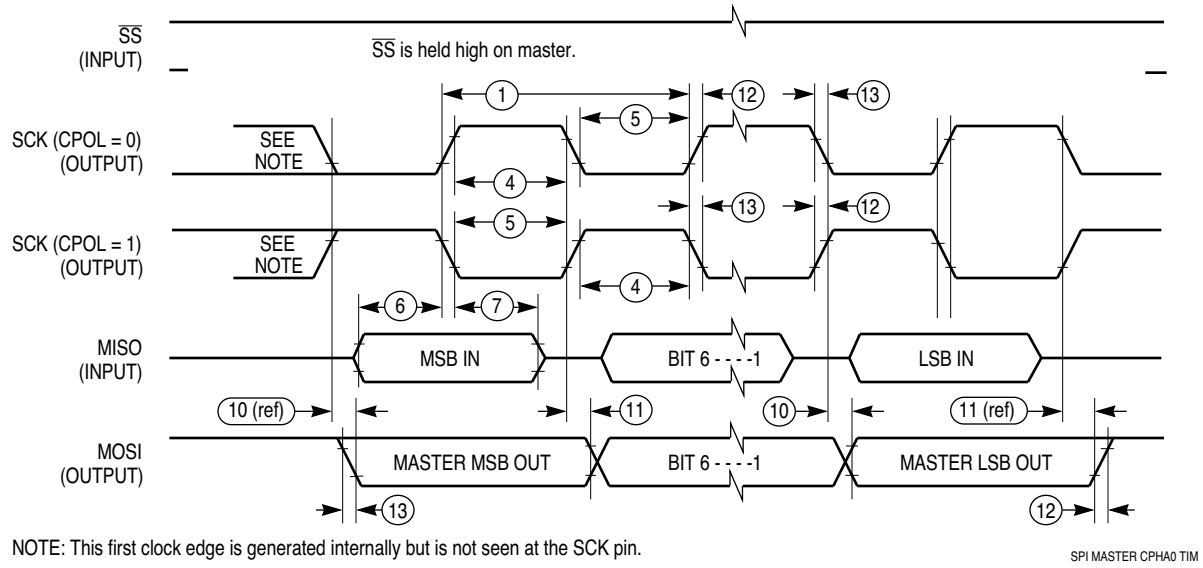
Table A-8 Serial Peripheral Interface (SPI) Timing

V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Num	Characteristic	Symbol	2.0 MHz		3.0 MHz		Unit
			Min	Max	Min	Max	
	Operating Frequency Master Slave	 $f_{op(m)}$ $f_{op(s)}$	 dc dc	 0.5 2.0	 dc dc	 0.5 3.0	 f_{op} MHz
1	Cycle Time Master Slave	 $t_{cyc(m)}$ $t_{cyc(s)}$	 2.0 500	 — —	 2.0 333	 — —	 t_{cyc} ns
2	Enable Lead Time Master (Note 2) Slave	 $t_{lead(m)}$ $t_{lead(s)}$	 — 250	 — —	 — 240	 — —	 ns ns
3	Enable Lag Time Master (Note 2) Slave	 $t_{lag(m)}$ $t_{lag(s)}$	 — 250	 — —	 — 240	 — —	 ns ns
4	Clock (SCK) High Time Master Slave	 $t_{w(SCKH)m}$ $t_{w(SCKH)s}$	 340 190	 — —	 227 127	 — —	 ns ns
5	Clock (SCK) Low Time Master Slave	 $t_{w(SCKL)m}$ $t_{w(SCKL)s}$	 340 190	 — —	 227 127	 — —	 ns ns
6	Data Setup Time (Inputs) Master Slave	 $t_{su(m)}$ $t_{su(s)}$	 100 100	 — —	 100 100	 — —	 ns ns
7	Data Hold Time (Inputs) Master Slave	 $t_{h(m)}$ $t_{h(s)}$	 100 100	 — —	 100 100	 — —	 ns ns
8	Access Time (Time to Data Active from High-Impedance State) Slave	 t_a	 0	 120	 0	 120	 ns
9	Disable Time (Hold Time to High-Impedance State) Slave	 t_{dis}	 —	 240	 —	 167	 ns
10	Data Valid (After Enable Edge)(Note 3)	$t_{v(s)}$	—	240	—	167	ns
11	Data Hold Time (Outputs) (After Enable Edge)	t_{ho}	0	—	0	—	ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, CL = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{rm} t_{rs}	 — —	 100 2.0	 — —	 100 2.0	 ns µs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{fm} t_{fs}	 — —	 100 2.0	 — —	 100 2.0	 ns µs

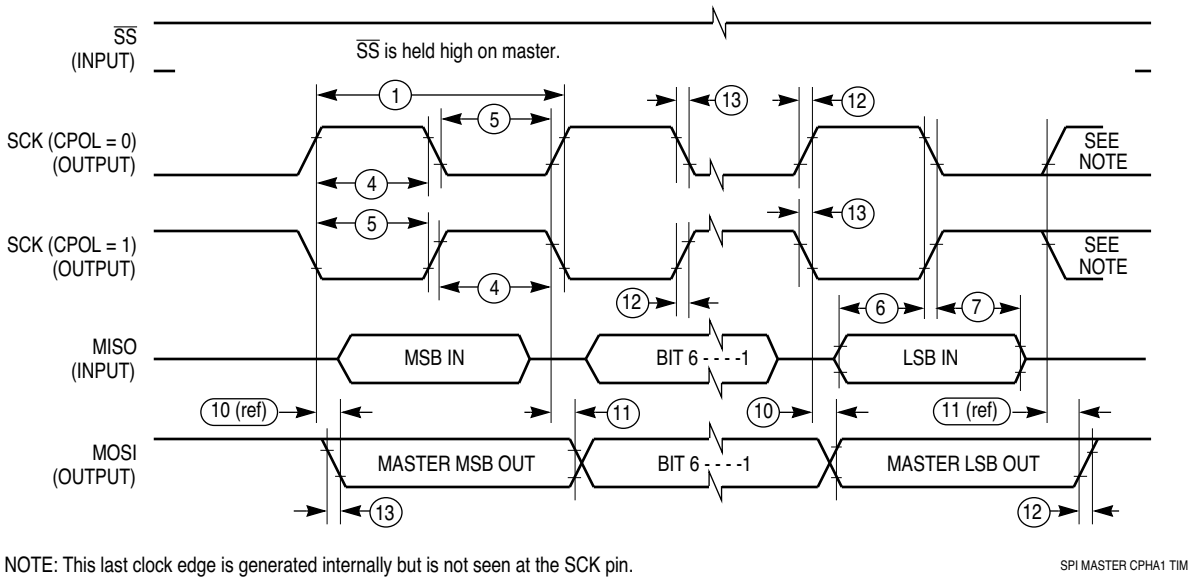
NOTES:

1. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Signal production depends on software.
3. Assumes 200 pF load on all SPI pins.



NOTE: This first clock edge is generated internally but is not seen at the SCK pin.

a) SPI Master Timing (CPHA = 0)



NOTE: This last clock edge is generated internally but is not seen at the SCK pin.

b) SPI Master Timing (CPHA = 1)

Figure A-15 SPI Timing Diagram (1 of 2)

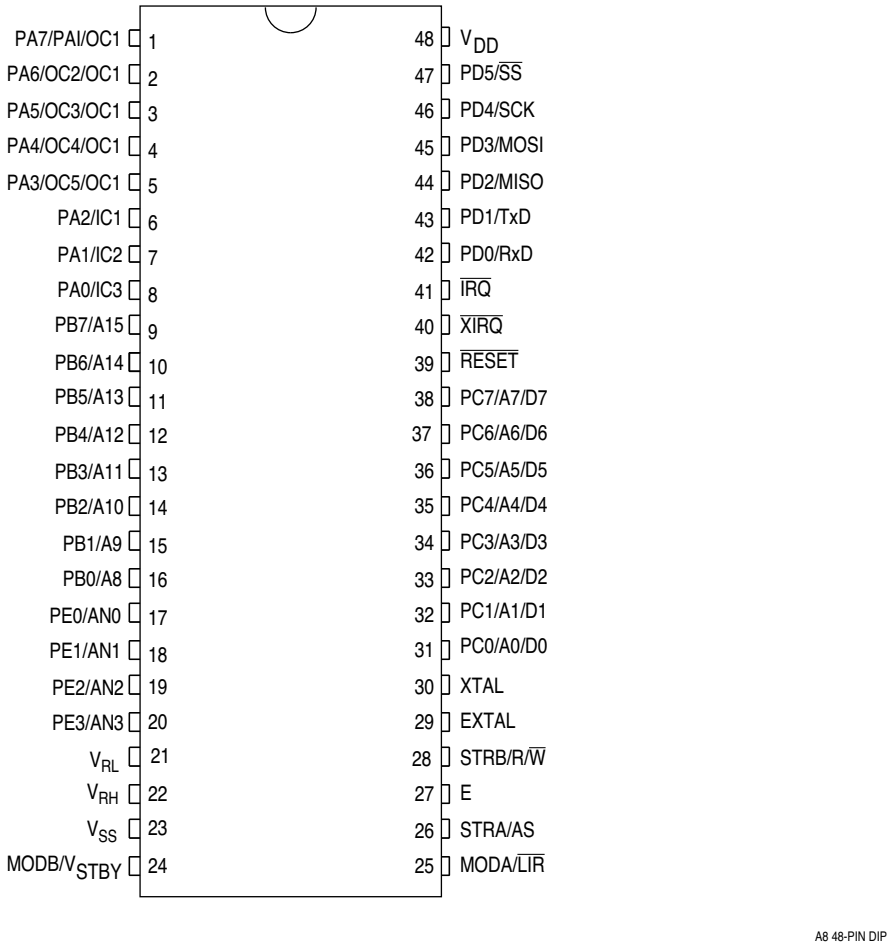


Figure B-2 48-Pin DIP

B