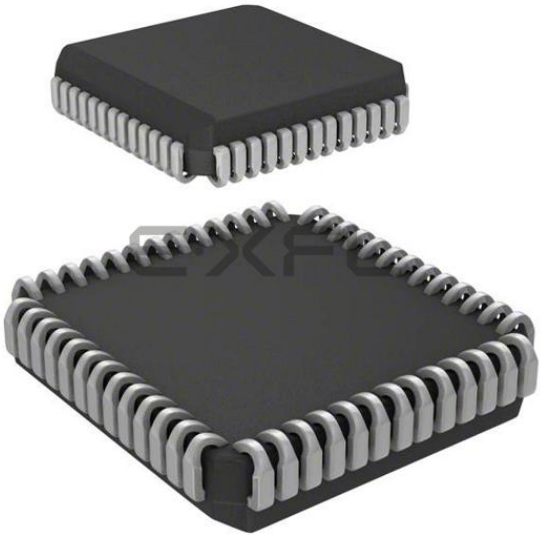

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Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	3MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	38
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	512 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LCC (J-Lead)
Supplier Device Package	52-PLCC (19.1x19.1)
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(SCI) and a separate synchronous serial peripheral interface (SPI) are included. The main 16-bit free-running timer system has three input capture lines, five output compare lines, and a real-time interrupt function. An 8-bit pulse accumulator subsystem can count external events or measure external periods.

Self monitoring circuitry is included on-chip to protect against system errors. A computer operating properly (COP) watchdog system protects against software failures. A clock monitor system generates a system reset in case the clock is lost or runs too slow. An illegal opcode detection circuit provides a non-maskable interrupt if an illegal opcode is detected.

Two software controlled operating modes, WAIT and STOP, are available to conserve additional power.

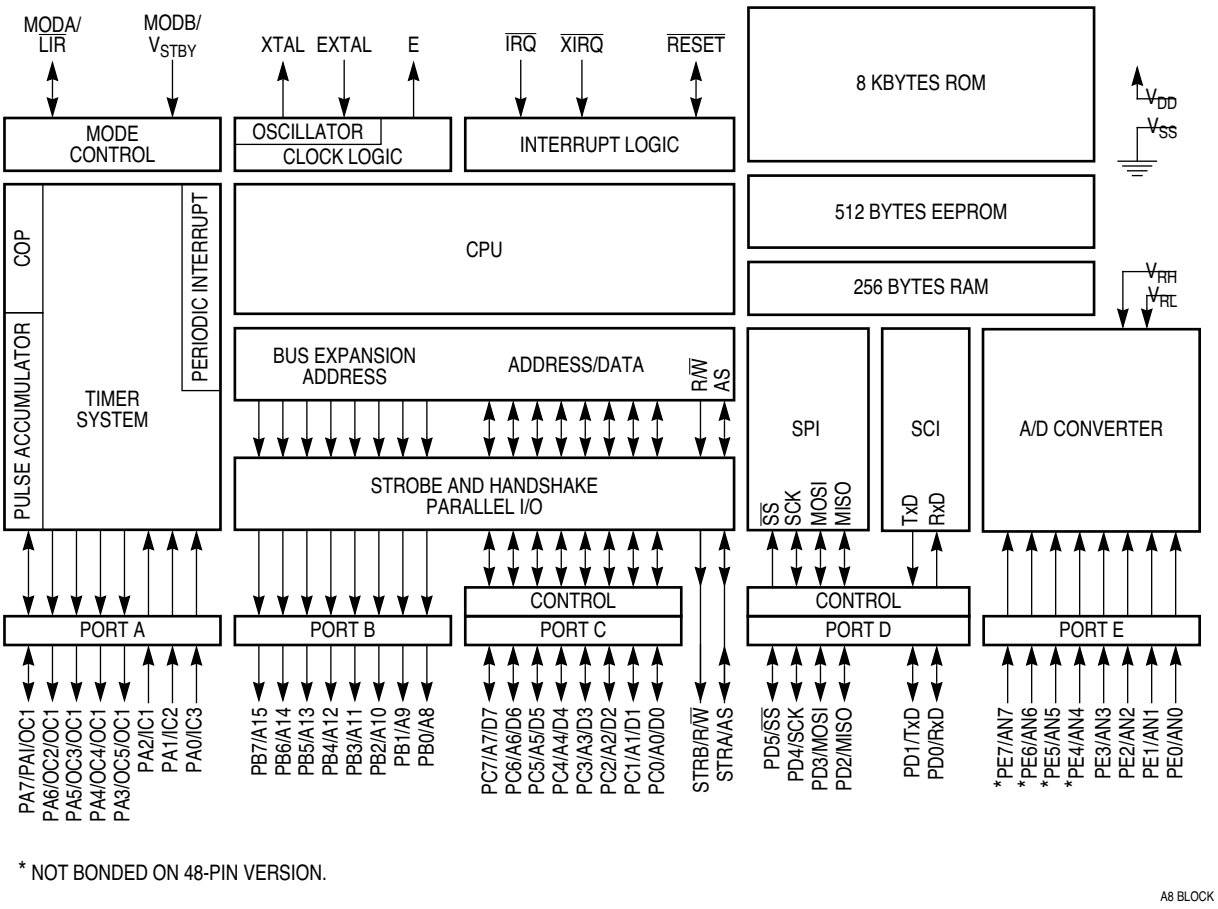
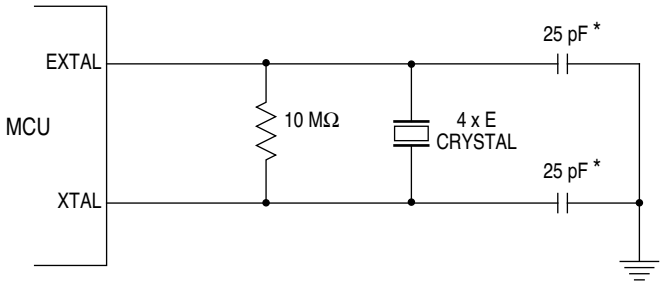


Figure 1-1 Block Diagram

1.3 Programmer's Model

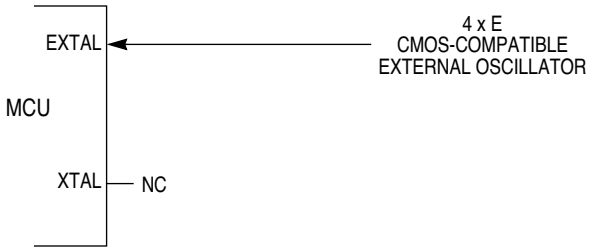
In addition to being able to execute all M6800 and M6801 instructions, the MC68HC11A8 allows execution of 91 new opcodes. **Figure 1-2** shows the seven CPU registers which are available to the programmer.



* THIS VALUE INCLUDES ALL STRAY CAPACITANCES.

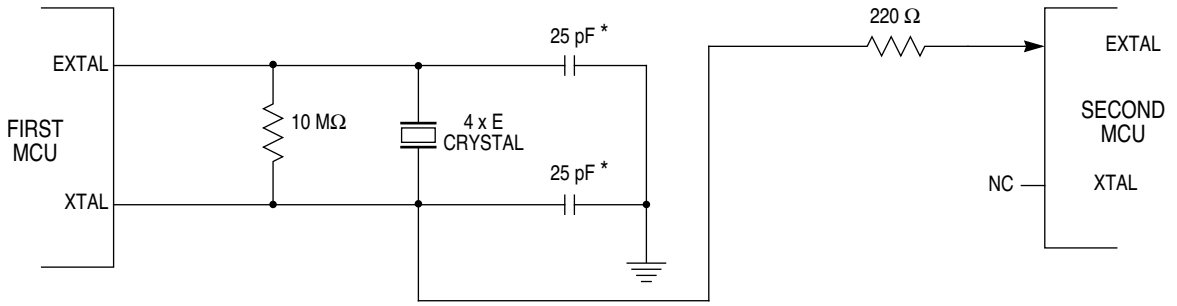
COMMON XTAL CONN

Figure 2-1 Common Crystal Connections



EXT EXTAL CONN

Figure 2-2 External Oscillator Connections



* THIS VALUE INCLUDES ALL STRAY CAPACITANCES.

DUAL-MCU XTAL CONN

Figure 2-3 One Crystal Driving Two MCUs

Table 2-2 Port Signal Summary

Port-Bit	Single Chip and Bootstrap Mode	Expanded Multiplexed and Special Test Mode
A-0	PA0/IC3	PA0/IC3
A-1	PA1/IC2	PA1/IC2
A-2	PA2/IC1	PA2/IC1
A-3	PA3/OC5/OC1	PA3/OC5/OC1
A-4	PA4/OC4/OC1	PA4/OC4/OC1
A-5	PA5/OC3/OC1	PA5/OC3/OC1
A-6	PA6/OC2/OC1	PA6/OC2/OC1
A-7	PA7/PAI/OC1	PA7/PAI/OC1
B-0	PB0	A8
B-1	PB1	A9
B-2	PB2	A10
B-3	PB3	A11
B-4	PB4	A12
B-5	PB5	A13
B-6	PB6	A14
B-7	PB7	A15
C-0	PC0	A0/D0
C-1	PC1	A1/D1
C-2	PC2	A2/D2
C-3	PC3	A3/D3
C-4	PC4	A4/D4
C-5	PC5	A5/D5
C-6	PC6	A6/D6
C-7	PC7	A7/D7
D-0	PD0/RXD	PD0/RXD
D-1	PD1/TXD	PD1/TXD
D-2	PD2/MISO	PD2/MISO
D-3	PD3/MOSI	PD3/MOSI
D-4	PD4/SCK	PD4/SCK
D-5	PD5/SS	PD5/SS
	STRA	AS
	STRB	R/W
E-0	PE0/AN0	PE0/AN0
E-1	PE1/AN1	PE1/AN1
E-2	PE2/AN2	PE2/AN2
E-3	PE3/AN3	PE3/AN3
E-4	PE4/AN4##	PE4/AN4##
E-5	PE5/AN5##	PE5/AN5##
E-6	PE6/AN6##	PE6/AN6##
E-7	PE7/AN7##	PE7/AN7##

Not bonded in 48-pin versions

The erased state of an EEPROM byte is $FF. Programming changes ones to zeros. If any bit in a location needs to be changed from a zero to a one, the byte must be erased in a separate operation before it is reprogrammed. If a new data byte has no ones in bit positions which were already programmed to zero, it is acceptable to program the new data without erasing the EEPROM byte first. For example, programming $50 to a location which was already $55 would change the location to $50.

Programming and erasure of the EEPROM relies on an internal high-voltage charge pump. At E clock frequencies below 2 MHz the efficiency of this charge pump decreases which increases the time required to program or erase a location. The recommended program and erase time is 10 milliseconds when the E clock is 2 MHz and should be increased to as much as 20 milliseconds when E is between 1 MHz and 2 MHz. When the E clock is below 1 MHz, the clock source for the charge pump should be switched from the system clock to an on-chip R-C oscillator clock. This is done by setting the CSEL bit in the OPTION register. A 10 millisecond period should be allowed after setting the CSEL bit to allow the charge pump to stabilize. Note that the CSEL bit also controls a clock to the analog-to-digital converter subsystem.

3.5.1 EEPROM Programming Control Register (PPROG)

This 8-bit register is used to control programming and erasure of the 512-byte EEPROM. Reset clears this register so the EEPROM is configured for normal reads.

	7	6	5	4	3	2	1	0	
$103B	ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM	PPROG
RESET	0	0	0	0	0	0	0	0	

ODD — Program Odd Rows (TEST)

EVEN — Program Even Rows (TEST)

Bit 5 — Not implemented.
This bit always reads zero.

BYTE — Byte Erase Select
This bit overrides the ROW bit.
0 = Row or Bulk Erase
1 = Erase Only One Byte

ROW — Row Erase Select
If the BYTE bit is 1, ROW has no meaning.
0 = Bulk Erase
1 = Row Erase

ERASE — Erase Mode Select
0 = Normal Read or Program
1 = Erase Mode

Once a valid start bit is detected, the start bit, each data bit, and the stop bit are sampled three times at RT intervals 8 RT, 9 RT, and 10 RT (1 RT is the position where the bit is expected to start), as shown in **Figure 5-2**. The value of the bit is determined by voting logic which takes the value of the majority of samples.

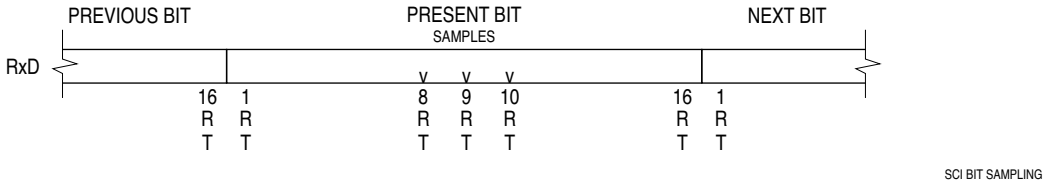


Figure 5-2 Sampling Technique Used on All Bits

5.5 Start Bit Detection

When the RxD input is detected low, it is tested for three more sample times (referred to as the start edge verification samples in **Figure 5-3**). If at least two of these three verification samples detect a logic zero, a valid start bit has been detected, otherwise the line is assumed to be idle. A noise flag is set if all three verification samples do not detect a logic zero. A valid start bit could be assumed with a set noise flag present.

If there has been a framing error without detection of a break (10 zeros for 8-bit format or 11 zeros for 9-bit format), the circuit continues to operate as if there actually was a stop bit and the start edge will be placed artificially. The last bit received in the data shift register is inverted to a logic one, and the three logic one start qualifiers (shown in **Figure 5-3**) are forced into the sample shift register during the interval when detection of a start bit is anticipated (see **Figure 5-4**); therefore, the start bit will be accepted no sooner than it is anticipated.

If the receiver detects that a break produced the framing error, the start bit will not be artificially induced and the receiver must actually detect a logic one before the start bit can be recognized. See **Figure 5-5**.

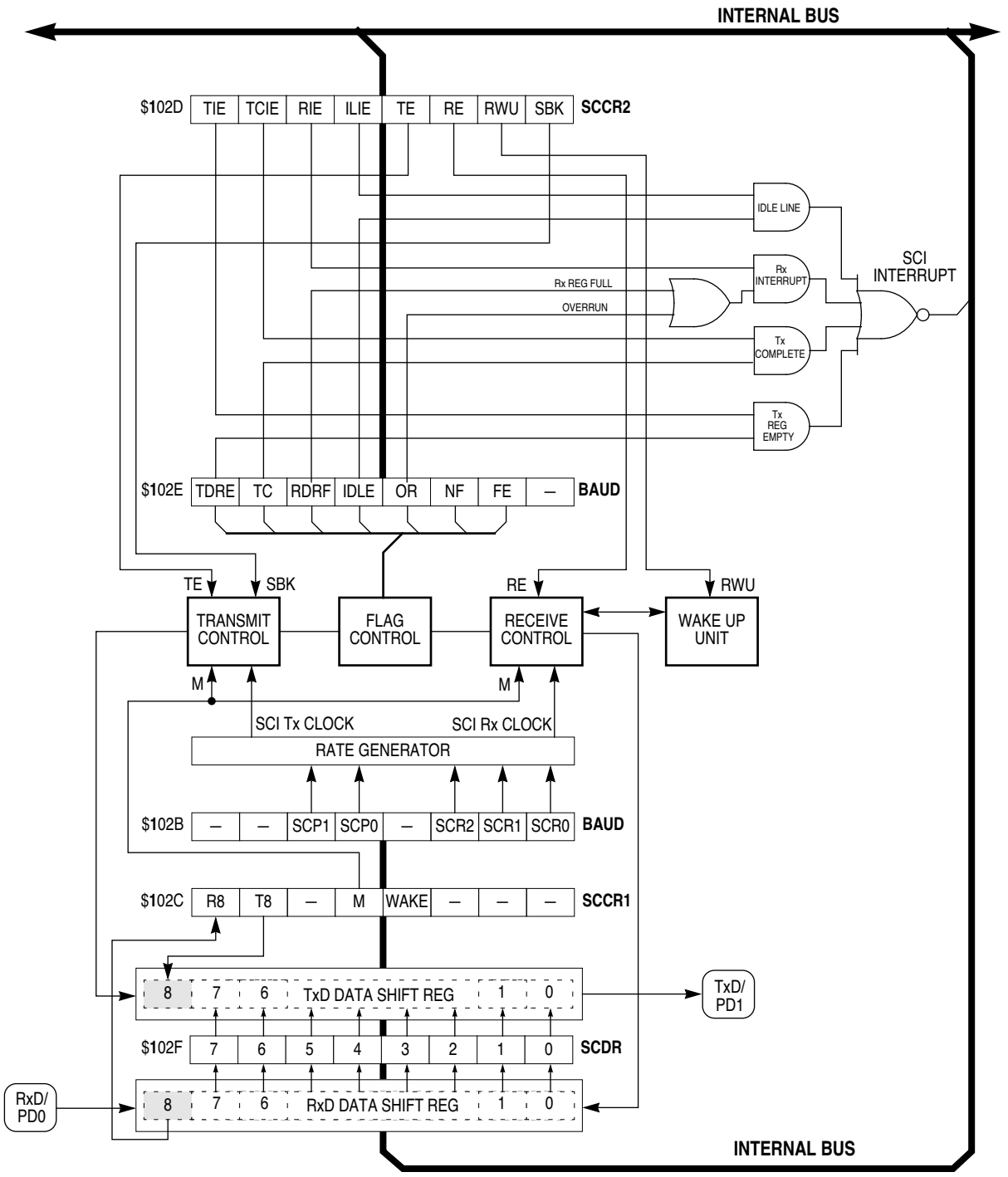


Figure 5-6 Serial Communications Interface Block Diagram

6.3 Functional Description

Figure 6-2 shows a block diagram of the serial peripheral interface circuitry. When a master device transmits data to a slave device via the MOSI line, the slave device responds by sending data to the master device via the master's MISO line. This implies full duplex transmission with both data out and data in synchronized with the same clock signal. Thus, the byte transmitted is replaced by the byte received and eliminates the need for separate transmit-empty and receiver-full status bits. A single status bit (SPIF) is used to signify that the I/O operation has been completed.

The SPI is double buffered on read, but not on write. If a write is performed during data transfer, the transfer occurs uninterrupted, and the write will be unsuccessful. This condition will cause the write collision (WCOL) status bit in the SPSR to be set. After a data byte is shifted, the SPIF flag of the SPSR is set.

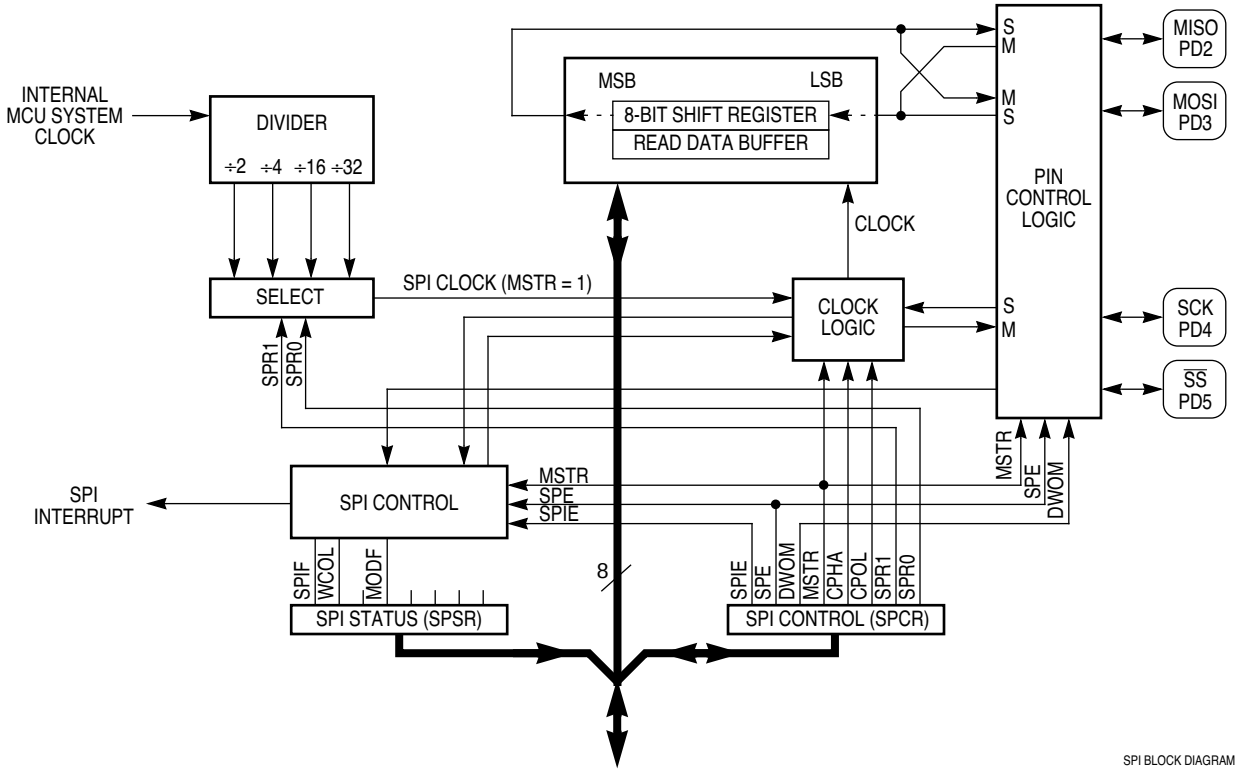


Figure 6-2 Serial Peripheral Interface Block Diagram

In the master mode, the SCK pin is an output. It idles high or low, depending on the CPOL bit in the SPCR, until data is written to the shift register, at which point eight clocks are generated to shift the eight bits of data and then SCK goes idle again.

In a slave mode, the slave start logic receives a logic low at the $\overline{SS}$ pin and a clock input at the SCK pin. Thus, the slave is synchronized with the master. Data from the master is received serially at the slave MOSI line and loads the 8-bit shift register. After the 8-bit shift register is loaded, its data is parallel transferred to the read buffer. During a write cycle, data is written into the shift register, then the slave waits for a clock train from the master to shift the data out on the slave's MISO line.

The result obtained by an input capture corresponds to the value of the counter one E clock cycle after the transition which triggered the edge-detection logic. The selected edge transition sets the ICxF bit in timer interrupt flag register 1 (TFLG1) and can cause an interrupt if the corresponding ICxl bit(s) is (are) set in the timer interrupt mask register 1 (TMSK1). A read of the input capture register's most significant byte inhibits captures for one E cycle to allow a double-byte read of the full 16-bit register.

8.1.3 Output Compare

All output compare registers are 16-bit read/write registers which are initialized to $FFFF by reset. They can be used as output waveform controls or as elapsed time indicators. If an output compare register is not used, it may be used as a storage location.

All output compare registers have a separate dedicated comparator for comparing against the free-running counter. If a match is found, the corresponding output compare flag (OCxF) bit in TFLG1 is set and a specified action is automatically taken. For output compare functions two through five the automatic action is controlled by pairs of bits (OMx and OLx) in the timer control register 1 (TCTL1). Each pair of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. The output action is taken on each successful compare regardless of whether or not the OCxF flag was previously clear.

An interrupt can also accompany a successful output compare, provided that the corresponding interrupt enable bit (OCxl) is set in TMSK1.

After a write cycle to the most significant byte, output compares are inhibited for one E cycle in order to allow writing two consecutive bytes before making the next comparison. If both bytes of the register are to be changed, a double-byte write instruction should be used in order to take advantage of the compare inhibit feature.

Writes can be made to either byte of the output compare register without affecting the other byte.

A write-only register, timer compare force (CFORC), allows forced compares. Five of the bit positions in the CFORC register correspond to the five output compares. To force a compare, or compares, a write is done to CFORC register with the associated bits set for each output compare that is to be forced. The action taken as a result of a forced compare is the same as if there was a match between the OCx register and the free-running counter, except that the corresponding interrupt status flag bits are not set. Output actions are synchronized to the prescaled timer clock so there could be as much as 16 E clock cycles of delay between the write to CFORC and the output action.

8.1.4 Output Compare 1 I/O Pin Control

Unlike the other four output compares, output compare 1 can automatically affect any or all of the five output pins (bits 3-7) in port A as a result of a successful compare between the OC1 register and the 16-bit free-running counter. The two 5-bit registers used in conjunction with this function are the output compare 1 mask register (OC1M) and the output compare 1 data register (OC1D).

Note that the pulse accumulator function shares line 7 of port A. If the DDRA7 bit in the pulse accumulator control register (PACTL) is set, then port A line 7 is configured as an output and OC1 can obtain access by setting OC1M bit 7. In this condition if the PAEN bit in the PACTL register is set, enabling the pulse accumulator input, then OC1 compares cause a write of OC1D bit 7 to an internal latch, and the output of that latch drives the pin and the pulse accumulator input. This action can then cause the pulse accumulator to take the appropriate action (pulse count or gate modes).

8.1.7 Output Compare 1 Data Register (OC1D)

This register is used in conjunction with output compare 1 to specify the data which is to be stored to the affected bits of port A as the result of a successful OC1 compare.

	7	6	5	4	3	2	1	0	
$1**0**0D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0	OC1D
RESET	0	0	0	0	0	0	0	0	

The bits of the OC1D register correspond bit-for-bit with the lines of port A (lines 7 thru 3 only). When a successful OC1 compare occurs, for each bit that is set in OC1M, the corresponding data bit in OC1D is stored in the corresponding bit of port A. If there is a conflicting situation where an OC1 compare and another output compare function occur during the same E cycle with both attempting to alter the same port A line, the OC1 action prevails.

8.1.8 Timer Control Register 1 (TCTL1)

	7	6	5	4	3	2	1	0	
$1**0**20	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
RESET	0	0	0	0	0	0	0	0	

OM2, OM3, OM4, and OM5 — Output Mode
OL2, OL3, OL4, and OL5 — Output Level

These two control bits (OMx and OLx) are encoded to specify the output action taken as a result of a successful OCx compare.

OMx	OLx	Action Taken Upon Successful Compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

	7	6	5	4	3	2	1	0	
$1023	OC1F	OC2F	OC3F	OC4F	OC5F	IC1F	IC2F	IC3F	TFLG1
RESET	0	0	0	0	0	0	0	0	

OCxF — Output Compare x Flag

This flag bit is set each time the timer counter matches the output compare register x value. A write of a zero does not affect this bit. A write of a one causes this bit to be cleared.

ICxF — Input Capture x Flag

This flag is set each time a selected active edge is detected on the ICx input line. A write of a zero does not affect this bit. A write of a one causes this bit to be cleared.

8.1.12 Timer Interrupt Mask Register 2 (TMSK2)

Timer interrupt mask register 2 is used to control whether or not a hardware interrupt sequence is requested as a result of a status bit being set in timer interrupt flag register 2. In addition, two timer prescaler bits are included in this register. For each of the four most significant bits in timer flag register 2, (TFLG2), there is a corresponding bit in the timer mask register 2 (TMSK2) in the same bit position.

	7	6	5	4	3	2	1	0	
$1024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	TMSK2
RESET	0	0	0	0	0	0	0	0	

TOI — Timer Overflow Interrupt Enable

0 = TOF interrupts disabled
1 = Interrupt requested when TOF = 1

RTII — RTI Interrupt Enable

0 = RTIF interrupts disabled
1 = Interrupt requested when RTIF = 1

PAOVI — Pulse Accumulator Overflow Interrupt Enable

0 = PAOVF interrupts disabled
1 = Interrupt requested when PAOVF = 1

PAII — Pulse Accumulator Input Interrupt Enable

0 = PAIF interrupts disabled
1 = Interrupt requested when PAIF = 1

Bits 3 and 2 — Not Implemented

These bits always read zero.

of reset. The DLY control bit is set to specify that an oscillator start-up delay is imposed upon recovery from STOP mode. The clock monitor system is disabled by CME equal zero.

9.1.3 Computer Operating Properly (COP) Reset

The MCU includes a computer operating properly watchdog system to help protect against software failures. To use a COP watchdog timer, a watchdog timer reset sequence must be executed on a regular periodic basis so that the watchdog timer is never allowed to time out.

The internal COP function includes special control bits which permit specification of one of four time out periods and even allows the function to be disabled completely. The COP system has a separate reset vector.

The NOCOP control bit, which determines whether or not a watchdog timeout causes a system reset, is implemented in an EEPROM cell in the CONFIG register. Once programmed, this bit remains set (or cleared) even when no power is applied, and the COP function is enabled or disabled independent of resident software. The NOCOP control bit may be preempted while in special modes to prevent the COP system from causing a hardware reset.

Two other control bits in the OPTION register select one of four timeout durations for the COP timer. The actual timeout period is dependent on the system E clock frequency, but for reference purposes, **Table 9-1** shows the relationship between the CR1 and CR0 control bits and the COP timeout period for various system clock frequencies.

Table 9-1 COP Timeout Period versus CR1 and CR0

CR1	CR0	Rate	XTAL = 12.0 MHz Timeout –0/+10.9 ms	XTAL = 2^{23} Timeout – 0/+15.6 ms	XTAL = 8.0 MHz Timeout – 0/+16.4 ms	XTAL = 4.9152 MHz Timeout – 0/+26.7 ms	XTAL = 4.0 MHz Timeout – 0/+32.8 ms	XTAL = 3.6864 MHz Timeout – 0/+35.6 ms
0	0	$2^{15} \div E$	10.923 ms	15.625 ms	16.384 ms	26.667 ms	32.768 ms	35.556 ms
0	1	$2^{17} \div E$	43.691 ms	62.5 ms	65.536 ms	106.67 ms	131.07 ms	142.22 ms
1	0	$2^{19} \div E$	174.76 ms	250 ms	262.14 ms	426.67 ms	524.29 ms	568.89 ms
1	1	$2^{21} \div E$	699.05 ms	1 s	1.049 s	1.707 s	2.1 s	2.276 s
		E =	**3.0 MHz**	**2.1 MHz**	**2.0 MHz**	**1.2288 MHz**	**1.0 MHz**	**921.6 kHz**

The default reset condition of the CR1 and CR0 bits is cleared which corresponds to the shortest timeout period.

The sequence required to reset the watchdog timer is:

1. Write $55 to the COP reset register (COPRST) at $103A, followed by
2. Write $AA to the same address.

Both writes must occur in correct order prior to timeout but, any number of instructions may be executed between the writes. The elapsed time between adjacent software reset sequences must never be greater than the COP time out period. Reading the COPRST register does not return meaningful data and does not affect the watchdog timer.

Table 9-4 SCI Serial System Interrupts

Interrupt Cause	Local Mask
Receive Data Register Full	RIE
Receiver Overrun	RIE
Idle Line Detect	ILIE
Transmit Data Register Empty	TIE
Transmit Complete	TCIE

9.2.1 Software Interrupt (SWI)

The software interrupt is executed in the same manner as any other instruction and will take precedence over interrupts only if the other interrupts are masked (I and X bits in the condition code register set). The SWI instruction is executed in a manner similar to other maskable interrupts in that it sets the I bit, CPU registers are stacked, etc.

NOTE

The SWI instruction will not be fetched if an interrupt is pending. However, once an SWI instruction has begun, no interrupt can be honored until the SWI vector has been fetched.

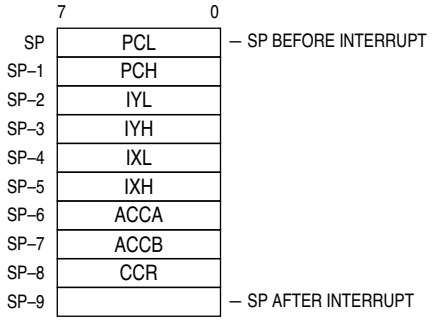


Figure 9-3 Interrupt Stacking Order

9.2.2 Illegal Opcode Trap

Since not all possible opcodes or opcode sequences are defined, an illegal opcode detection circuit has been included. When an illegal opcode is detected, an interrupt is requested to the illegal opcode vector. The illegal opcode vector should never be left uninitialized. It is a good idea to reinitialize the stack pointer as a result of an illegal opcode interrupt so repeated execution of illegal opcodes does not cause stack overruns.

9.2.3 Interrupt Mask Bits in Condition Code Register

Upon reset, both the X bit and the I bit are set to inhibit all maskable interrupts and $\overline{\text{XIRQ}}$. After minimum system initialization, software may clear the X bit by a TAP instruction, thus enabling $\overline{\text{XIRQ}}$ interrupts. Thereafter software cannot set the X bit so an $\overline{\text{XIRQ}}$ interrupt is effectively a nonmaskable interrupt. Since the operation of the I

10 CPU, ADDRESSING MODES, AND INSTRUCTION SET

This section provides a description of the CPU registers, addressing modes, and a summary of the M68HC11 instruction set. Special operations such as subroutine calls and interrupts are described and cycle-by-cycle operations for all instructions are presented.

10.1 CPU Registers

In addition to being able to execute all M6800 and M6801 instructions, the MC68HC11A8 uses a 4-page opcode map to allow execution of 91 new opcodes (see **10.2.7 Prebyte**). Seven registers, discussed in the following paragraphs, are available to programmers as shown in **Figure 10-1**.

10.1.1 Accumulators A and B

Accumulator A and accumulator B are general-purpose 8-bit registers used to hold operands and results of arithmetic calculations or data manipulations. These two accumulators can be concatenated into a single 16-bit accumulator called the D accumulator.

10.1.2 Index Register X (IX)

The 16-bit IX register is used for indexed mode addressing. It provides a 16-bit indexing value which is added to an 8-bit offset provided in an instruction to create an effective address. The IX register can also be used as a counter or as a temporary storage register.

Table 10-1 MC68HC11A8 Instructions, Addressing Modes, and Execution Times (Sheet 3 of 6)

Source Form(s)	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal)		Bytes	Cycle	Cycle by Cycle*	Condition Codes
				Opcode	Operand(s)				S X H I N Z V C
CPX (opr)	Compare X to Memory 16-Bit	IX – M:M + 1	IMM	8C	jj kk	3	4	3-3	- - - - ↕ ↕ ↕ ↕
			DIR	9C	dd	2	5	4-7	
			EXT	BC	hh ll	3	6	5-10	
			IND,X	AC	ff	2	6	6-10	
			IND,Y	CD AC	ff	3	7	7-8	
CPY (opr)	Compare Y to Memory 16-Bit	IY – M:M + 1	IMM	18 8C	jj kk	4	5	3-5	- - - - ↕ ↕ ↕ ↕
			DIR	18 9C	dd	3	6	4-9	
			EXT	18 BC	hh ll	4	7	5-11	
			IND,X	1A AC	ff	3	7	6-11	
			IND,Y	18 AC	ff	3	7	7-8	
DAA	Decimal Adjust A	Adjust Sum to BCD	INH	19		1	2	2-1	- - - - ↕ ↕ ↕ ↕
DEC (opr)	Decrement Memory Byte	M – 1 → M	EXT	7A	hh ll	3	6	5-8	- - - - ↕ ↕ ↕ -
			IND,X	6A	ff	2	6	6-3	
			IND,Y	18 6A	ff	3	7	7-3	
DECA	Decrement Accumulator A	A – 1 → A	A INH	4A		1	2	2-1	- - - - ↕ ↕ ↕ -
DECB	Decrement Accumulator B	B – 1 → B	B INH	5A		1	2	2-1	- - - - ↕ ↕ ↕ -
DES	Decrement Stack Pointer	SP – 1 → SP	INH	34		1	3	2-3	- - - - - - - -
DEX	Decrement Index Register X	IX – 1 → IX	INH	09		1	3	2-2	- - - - - ↕ - -
DEY	Decrement Index Register Y	IY – 1 → IY	INH	18 09		2	4	2-4	- - - - - ↕ - -
EORA (opr)	Exclusive OR A with Memory	A ⊕ M → A	A IMM	88	ii	2	2	3-1	- - - - ↕ ↕ 0 -
			A DIR	98	dd	2	3	4-1	
			A EXT	B8	hh ll	3	4	5-2	
			A IND,X	A8	ff	2	4	6-2	
			A IND,Y	18 A8	ff	3	5	7-2	
EORB (opr)	Exclusive OR B with Memory	B ⊕ M → B	B IMM	C8	ii	2	2	3-1	- - - - ↕ ↕ 0 -
			B DIR	D8	dd	2	3	4-1	
			B EXT	F8	hh ll	3	4	5-2	
			B IND,X	E8	ff	2	4	6-2	
			B IND,Y	18 E8	ff	3	5	7-2	
FDIV	Fractional Divide 16 by 16	D/IX → IX; r → D	INH	03		1	41	2-17	- - - - - ↕ ↕ ↕
IDIV	Integer Divide 16 by 16	D/IX → IX; r → D	INH	02		1	41	2-17	- - - - - ↕ 0 ↕
INC (opr)	Increment Memory Byte	M + 1 → M	EXT	7C	hh ll	3	6	5-8	- - - - ↕ ↕ ↕ -
			IND,X	6C	ff	2	6	6-3	
			IND,Y	18 6C	ff	3	7	7-3	
INCA	Increment Accumulator A	A + 1 → A	A INH	4C		1	2	2-1	- - - - ↕ ↕ ↕ -
INCB	Increment Accumulator B	B + 1 → B	B INH	5C		1	2	2-1	- - - - ↕ ↕ ↕ -
INS	Increment Stack Pointer	SP + 1 → SP	INH	31		1	3	2-3	- - - - - - - -
INX	Increment Index Register X	IX + 1 → IX	INH	08		1	3	2-2	- - - - - ↕ - -
INY	Increment Index Register Y	IY + 1 → IY	INH	18 08		2	4	2-4	- - - - - ↕ - -
JMP (opr)	Jump	See Special Ops	EXT	7E	hh ll	3	3	5-1	- - - - - - - -
			IND,X	6E	ff	2	3	6-1	
			IND,Y	18 6E	ff	3	4	7-1	
JSR (opr)	Jump to Subroutine	See Special Ops	DIR	9D	dd	2	5	4-8	- - - - - - - -
			EXT	BD	hh ll	3	6	5-12	
			IND,X	AD	ff	2	6	6-12	
			IND,Y	18 AD	ff	3	7	7-9	
LDAA (opr)	Load Accumulator A	M → A	A IMM	86	ii	2	2	3-1	- - - - ↕ ↕ 0 -
			A DIR	96	dd	2	3	4-1	
			A EXT	B6	hh ll	3	4	5-2	
			A IND,X	A6	ff	2	4	6-2	
			A IND,Y	18 A6	ff	3	5	7-2	
LDAB (opr)	Load Accumulator B	M → B	B IMM	C6	ii	2	2	3-1	- - - - ↕ ↕ 0 -
			B DIR	D6	dd	2	3	4-1	
			B EXT	F6	hh ll	3	4	5-2	
			B IND,X	E6	ff	2	4	6-2	
			B IND,Y	18 E6	ff	3	5	7-2	
LDD (opr)	Load Double Accumulator D	M → A,M + 1 → B	IMM	CC	jj kk	3	3	3-2	- - - - ↕ ↕ 0 -
			DIR	DC	dd	2	4	4-3	
			EXT	FC	hh ll	3	5	5-4	
			IND,X	EC	ff	2	5	6-6	
			IND,Y	18 EC	ff	3	6	7-6	

*Cycle-by-cycle number provides a reference to Tables 10-2 through 10-8 which detail cycle-by-cycle operation.
Example: Table 10-1 Cycle-by-Cycle column reference number 2-4 equals Table 10-2 line item 2-4.

NOTES:
1. Edge sensitive IRQ pin (IRQE bit = 1)
2. Level sensitive IRQ pin (IRQE bit = 0)

Figure A-6 Interrupt Timing Diagram

Table A-7a Expansion Bus Timing (MC68L11A8)

V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H							
Num	**Characteristic**	**Symbol**	**1.0 MHz**		**2.0 MHz**		**Unit**
			Min	**Max**	**Min**	**Max**	
	Frequency of Operation (E-Clock Frequency)	f_o	dc	1.0	dc	2.0	MHz
1	Cycle Time	t_{cyc}	1000	—	500	—	ns
2	Pulse Width, E Low $PW_{EL} = 1/2\ t_{cyc} - 23$ ns (Note 1)	PW_{EL}	475	—	225	—	ns
3	Pulse Width, E High $PW_{EH} = 1/2\ t_{cyc} - 28$ ns (Note 1)	PW_{EH}	470	—	220	—	ns
4a, b	E and AS Rise and Fall Time	t_r t_f	—	25 25	—	25 25	ns
9	Address Hold Time $t_{AH} = 1/8\ t_{cyc} - 29.5$ ns (Note 1, 2a)	t_{AH}	95	—	33	—	ns
12	Non-Muxed Address Valid Time to E Rise $t_{AV} = PW_{EL} - (t_{ASD} + 80$ ns) (Note 1, 2a)	t_{AV}	275	—	88	—	ns
17	Read Data Setup Time	t_{DSR}	30	—	30	—	ns
18	Read Data Hold Time (Max = t_{MAD})	t_{DHR}	0	150	0	88	ns
19	Write Data Delay Time $t_{DDW} = 1/8\ t_{cyc} + 65.5$ ns (Note 1, 2a)	t_{DDW}	—	195	—	133	ns
21	Write Data Hold Time $t_{DHW} = 1/8\ t_{cyc} - 29.5$ ns (Note 1, 2a)	t_{DHW}	95	—	33	—	ns
22	Muxed Address Valid Time to E Rise $t_{AVM} = PW_{EL} - (t_{ASD} + 90$ ns) (Note 1, 2a)	t_{AVM}	265	—	78	—	ns
24	Muxed Address Valid Time to AS Fall $t_{ASL} = PW_{ASH} - 70$ ns (Note 1)	t_{ASL}	150	—	25	—	ns
25	Muxed Address Hold Time $t_{AHL} = 1/8\ t_{cyc} - 29.5$ ns (Note 1, 2b)	t_{AHL}	95	—	33	—	ns
26	Delay Time, E to AS Rise $t_{ASD} = 1/8\ t_{cyc} - 9.5$ ns (Note 1, 2a)	t_{ASD}	120	—	58	—	ns
27	Pulse Width, AS High $PW_{ASH} = 1/4\ t_{cyc} - 29$ ns (Note 1)	PW_{ASH}	220	—	95	—	ns
28	Delay Time, AS to E Rise $t_{ASED} = 1/8\ t_{cyc} - 9.5$ ns (Note 1, 2b)	t_{ASED}	120	—	58	—	ns
29	MPU Address Access Time (Note 2a) $t_{ACCA} = t_{cyc} - (PW_{EL} - t_{AVM}) - t_{DSR} - t_f$	t_{ACCA}	735	—	298	—	ns
35	MPU Access Time $t_{ACCE} = PW_{EH} - t_{DSR}$	t_{ACCE}	—	440	—	190	ns
36	Muxed Address Delay (Previous Cycle MPU Read) $t_{MAD} = t_{ASD} + 30$ ns (Note 1, 2a)	t_{MAD}	150	—	88	—	ns

NOTES:

1. Formula only for dc to 2 MHz.
2. Input clocks with duty cycles other than 50% affect bus performance. Timing parameters affected by input clock duty cycle are identified by (a) and (b). To recalculate the approximate bus timing values, substitute the following expressions in place of 1/8 t_{cyc} in the above formulas, where applicable:
   (a) (1-DC) x 1/4 t_{cyc}
   (b) DC x 1/4 t_{cyc}

   Where:
   DC is the decimal value of duty cycle percentage (high time).
3. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.

Table A-8 Serial Peripheral Interface (SPI) Timing

V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Num	Characteristic	Symbol	2.0 MHz		3.0 MHz		Unit
			Min	Max	Min	Max	
	Operating Frequency Master Slave	 $f_{op(m)}$ $f_{op(s)}$	 dc dc	 0.5 2.0	 dc dc	 0.5 3.0	 f_{op} MHz
1	Cycle Time Master Slave	 $t_{cyc(m)}$ $t_{cyc(s)}$	 2.0 500	 — —	 2.0 333	 — —	 t_{cyc} ns
2	Enable Lead Time Master (Note 2) Slave	 $t_{lead(m)}$ $t_{lead(s)}$	 — 250	 — —	 — 240	 — —	 ns ns
3	Enable Lag Time Master (Note 2) Slave	 $t_{lag(m)}$ $t_{lag(s)}$	 — 250	 — —	 — 240	 — —	 ns ns
4	Clock (SCK) High Time Master Slave	 $t_{w(SCKH)m}$ $t_{w(SCKH)s}$	 340 190	 — —	 227 127	 — —	 ns ns
5	Clock (SCK) Low Time Master Slave	 $t_{w(SCKL)m}$ $t_{w(SCKL)s}$	 340 190	 — —	 227 127	 — —	 ns ns
6	Data Setup Time (Inputs) Master Slave	 $t_{su(m)}$ $t_{su(s)}$	 100 100	 — —	 100 100	 — —	 ns ns
7	Data Hold Time (Inputs) Master Slave	 $t_{h(m)}$ $t_{h(s)}$	 100 100	 — —	 100 100	 — —	 ns ns
8	Access Time (Time to Data Active from High-Impedance State) Slave	 t_a	 0	 120	 0	 120	 ns
9	Disable Time (Hold Time to High-Impedance State) Slave	 t_{dis}	 —	 240	 —	 167	 ns
10	Data Valid (After Enable Edge)(Note 3)	$t_{v(s)}$	—	240	—	167	ns
11	Data Hold Time (Outputs) (After Enable Edge)	t_{ho}	0	—	0	—	ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, CL = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{rm} t_{rs}	 — —	 100 2.0	 — —	 100 2.0	 ns µs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{fm} t_{fs}	 — —	 100 2.0	 — —	 100 2.0	 ns µs

NOTES:

1. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Signal production depends on software.
3. Assumes 200 pF load on all SPI pins.

B MECHANICAL DATA AND ORDERING INFORMATION

B.1 Pin Assignments

The MC68HC11A8 is available in the 52-pin plastic leaded chip carrier (PLCC), the 48-pin dual in-line package (DIP), or the 64-pin quad flat pack (QFP).

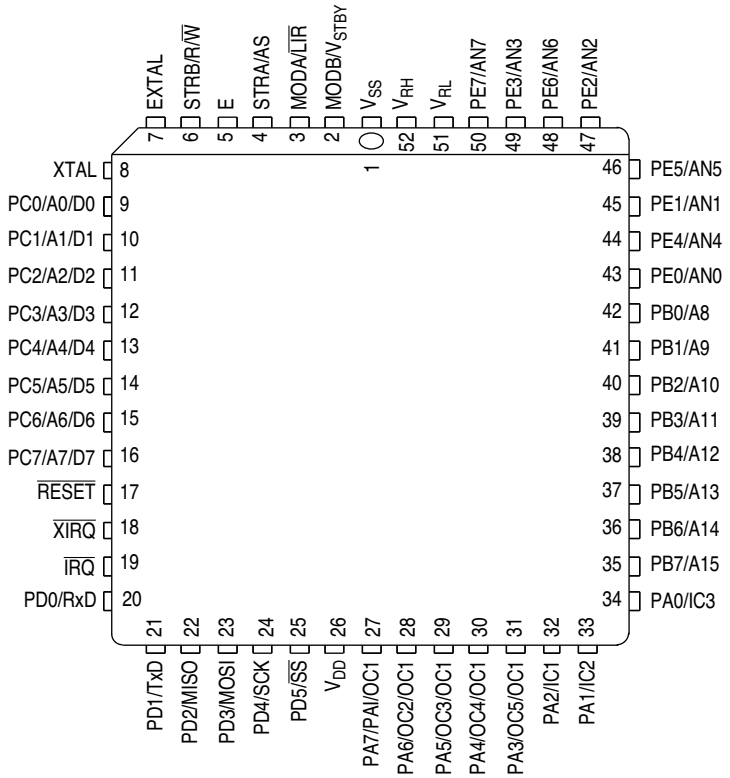


Figure B-1 52-Pin PLCC

Table B-1 Ordering Information

Package	Temperature	CONFIG	Description	MC Order Number
52-Pin PLCC	– 40° to + 85°C	$0C	No ROM, No EEPROM	MC68HC11A0CFN2
	– 40° to + 85°C	$0C	No ROM, No EEPROM, 3 MHz	MC68HC11A0CFN3
	– 40° to + 85°C	$0D	No ROM	MC68HC11A1CFN2
	– 40° to + 85°C	$0D	No ROM, 3 MHz	MC68HC11A1CFN3
	– 40° to + 105°C	$0D	No ROM	MC68HC11A1VFN2
	– 40° to + 125°C	$0D	No ROM	MC68HC11A1MFN2
	– 40° to + 85°C	$09	No ROM, COP On	MC68HCP11A1CFN2
	– 40° to + 85°C	$09	No ROM, COP On, 3 MHz	MC68HCP11A1CFN3
	– 40° to + 105°C	$09	No ROM, COP On	MC68HCP11A1VFN2
	– 40° to + 125°C	$09	No ROM, COP On	MC68HCP11A1MFN2
	– 40° to + 85°C	$0F	BUFFALO ROM	MC68HC11A8BCFN2
	– 40° to + 105°C	$0F	BUFFALO ROM	MC68HC11A8VCFN2
	– 40° to + 125°C	$0F	BUFFALO ROM	MC68HC11A8MCFN2
48-Pin DIP	– 40° to + 85°C	$0C	No ROM, No EEPROM	MC68HC11A0CP2
	– 40° to + 85°C	$0C	No ROM, No EEPROM, 3 MHz	MC68HC11A0CP3
	– 40° to + 85°C	$0D	No ROM	MC68HC11A1CP2
	– 40° to + 85°C	$0D	No ROM, 3 MHz	MC68HC11A1CP3
	– 40° to + 105°C	$0D	No ROM	MC68HC11A1VP2
	– 40° to + 125°C	$0D	No ROM	MC68HC11A1MP2
	– 40° to + 85°C	$09	No ROM, COP On	MC68HCP11A1CP2
	– 40° to + 85°C	$09	No ROM, COP On, 3 MHz	MC68HCP11A1CP3
	– 40° to + 105°C	$09	No ROM, COP On	MC68HCP11A1VP2
	– 40° to + 125°C	$09	No ROM, COP On	MC68HCP11A1MP2
	– 40° to + 85°C	$0F	BUFFALO ROM	MC68HC11A8BCP2
	– 40° to + 105°C	$0F	BUFFALO ROM	MC68HC11A8BVP2
	– 40° to + 125°C	$0F	BUFFALO ROM	MC68HC11A8BMP2
64-Pin QFP	– 40° to + 85°C	$0C	No ROM, No EEPROM	MC68HC11A0CFU2
	– 40° to + 85°C	$0C	No ROM, No EEPROM, 3 MHz	MC68HC11A0CFU3
	– 40° to + 85°C	$0D	No ROM	MC68HC11A1CFU2
	– 40° to + 85°C	$0D	No ROM, 3 MHz	MC68HC11A1CFU3
	– 40° to + 105°C	$0D	No ROM	MC68HC11 A1VFU2
	– 40° to + 125°C	$0D	No ROM	MC68HC11A1MFU2
	– 40° to + 85°C	$0F	BUFFALO ROM	MC68HC11A8BCFU2
	– 40° to + 105°C	$0F	BUFFALO ROM	MC68HC11A8VCFU2