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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8560cvt667jb

6 DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8560.

6.1 DDR SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8560.

Table 13. DDR SDRAM DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	4
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.18$	V	4
Output leakage current	I_{OZ}	–10	10	μA	5
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–15.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	15.2	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	100	μA	—

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. V_{IH} can tolerate an overshoot of 1.2V over GV_{DD} for a pulse width of ≤3 ns, and the pulse width cannot be greater than t_{MCK}. V_{IL} can tolerate an undershoot of 1.2V below GND for a pulse width of ≤3 ns, and the pulse width cannot be greater than t_{MCK}.
5. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

Table 14 provides the DDR capacitance.

Table 14. DDR SDRAM Capacitance

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, MSYNC_IN	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak to peak) = 0.2 V.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 15 provides the input AC timing specifications for the DDR SDRAM interface.

Table 15. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	GV_{DD} + 0.3	V	—
MDQS—MDQ/MECC input skew per byte For DDR = 333 MHz For DDR ≤ 266 MHz	t_{DISKEW}	 -750 -1125	 750 1125	ps	1, 2

Note:

1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 ≤ n ≤ 7) or ECC (MECC[{0...7}] if n=8).
2. For timing budget analysis, the MPC8560 consumes ±550 ps of the total budget.

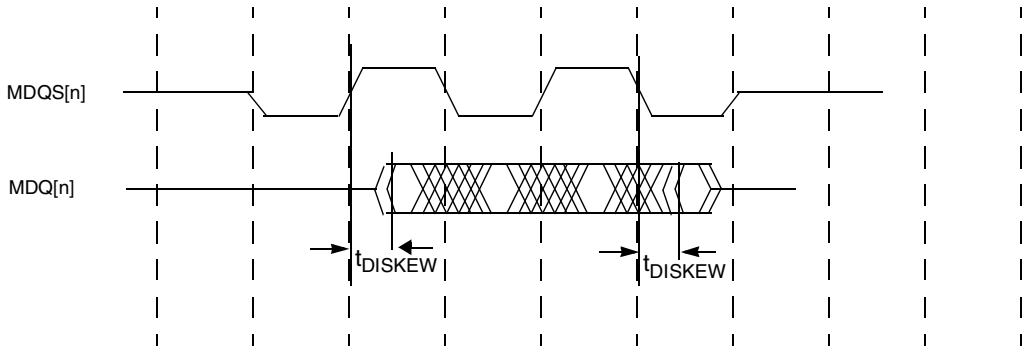


Figure 4. DDR SDRAM Interface Input Timing

Table 16. DDR SDRAM Output AC Timing Specifications–DLL Mode (continued)

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDSHME}	1.5	4.0	ns	7, 8

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (OX or DX). For example, t_{DDKHOV} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (O) are valid (V) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. Maximum possible clock skew between a clock MCK[n] and its relative inverse clock $\overline{\text{MCK}}$[n], or between a clock MCK[n] and a relative clock MCK[m] or MSYNC_OUT. Skew measured between complementary signals at $GV_{DD}/2$.
4. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$ and MDQ/MECC/MDM/MDQS.
5. Note that t_{DDSHMH} follows the symbol conventions described in note 1. For example, t_{DDSHMH} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) until the MDQS signal is valid (MH). t_{DDSHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. These controls allow the relationship between the synchronous clock control timing and the source-synchronous DQS domain to be modified by the user. For best turnaround times, these may need to be set to delay t_{DDSHMH} an additional $0.25t_{MCK}$. This will also affect t_{DDSHMP} and t_{DDSHME} accordingly. See the *MPC8560 PowerQUICC III Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8560.
7. All outputs are referenced to the rising edge of MSYNC_IN (S) at the pins of the MPC8560. Note that t_{DDSHMP} follows the symbol conventions described in note 1. For example, t_{DDSHMP} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) for the duration of the MDQS signal precharge period (MP).
8. Guaranteed by design.
9. Guaranteed by characterization.

Figure 5 provides the AC test load for the DDR bus.

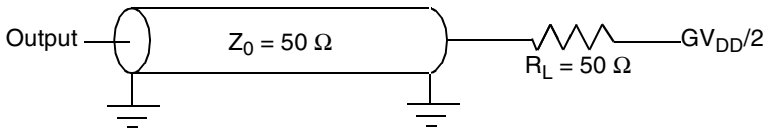


Figure 5. DDR AC Test Load

Table 17. DDR SDRAM Measurement Conditions

Symbol	DDR	Unit	Notes
V_{TH}	MV_{REF} ± 0.31 V	V	1
V_{OUT}	0.5 × GV_{DD}	V	2

Notes:

1. Data input threshold measurement point.
2. Data output measurement point.

Table 20. GMII, MII, RGMII, RTBI, and TBI DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	2.37	2.63	V
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V
Input high voltage	V_{IH}	1.70	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	–0.3	0.70	V
Input high current (V_{IN} [1] = LV_{DD})	I_{IH}	—	10	μA
Input low current (V_{IN} [1] = GND)	I_{IL}	–15	—	μA

Note:
1.Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1and Table 2.

7.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

7.2.1 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

7.2.1.1 GMII Transmit AC Timing Specifications

Table 21 provides the GMII transmit AC timing specifications.

Table 21. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	40	—	60	%
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX} [3]	0.5	—	5.0	ns

7.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

7.2.2.1 MII Transmit AC Timing Specifications

Table 23 provides the MII transmit AC timing specifications.

Table 23. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX} [2]	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise and fall time	t_{MTXR}, t_{MTXF} [2,3]	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 10 shows the MII transmit AC timing diagram.

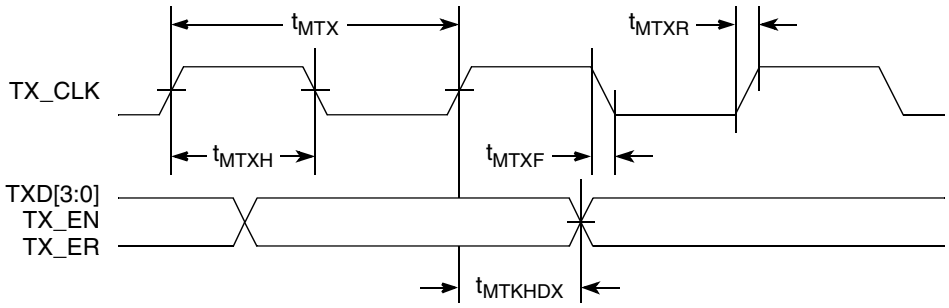


Figure 10. MII Transmit AC Timing Diagram

Table 31. Local Bus General Timing Parameters—DLL Enabled (continued)

Parameter	POR Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKHOZ2}$	—	2.5	ns	7, 9
	TSEC2_TXD[6:5] = 11 (default)			3.8		

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for DLL enabled mode.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $OV_{DD}/2$.
4. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for DLL enabled to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins TSEC2_TXD[6:5].
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.
9. Guaranteed by design.

Table 32 describes the general timing parameters of the local bus interface of the MPC8560 with the DLL bypassed.

Table 32. Local Bus General Timing Parameters—DLL Bypassed

Parameter	POR Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	—	t_{LBK}	6.0	—	ns	2
Internal launch/capture clock to LCLK delay	—	t_{LBKHKT}	2.3	3.9	ns	8
LCLK[n] skew to LCLK[m] or LSYNC_OUT	—	$t_{LBKSKEW}$	—	150	ps	3, 9
Input setup to local bus clock (except LUPWAIT)	—	$t_{LBIVKH1}$	5.7	—	ns	4, 5
LUPWAIT input setup to local bus clock	—	$t_{LBIVKH2}$	5.6	—	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	—	$t_{LBIXKH1}$	-1.8	—	ns	4, 5
LUPWAIT input hold from local bus clock	—	$t_{LBIXKH2}$	-1.3	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	—	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKLOV1}$	—	-0.3	ns	4
	TSEC2_TXD[6:5] = 11 (default)			1.2		

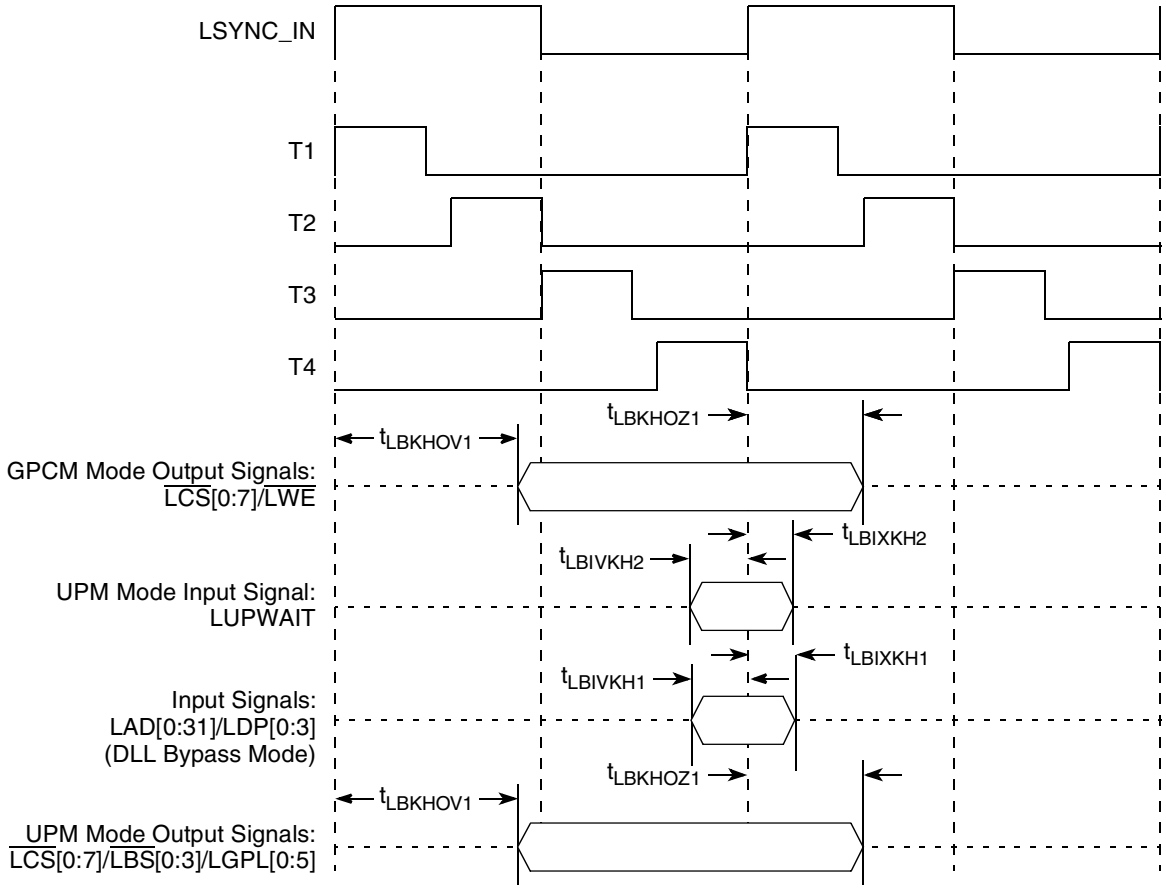


Figure 21. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Enabled)

Figure 24 shows the FCC internal clock.

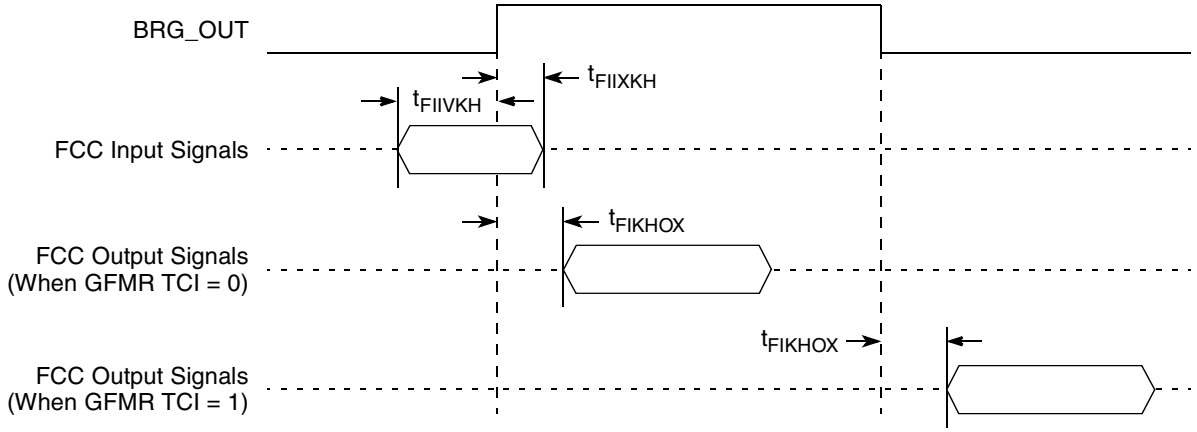


Figure 24. FCC Internal AC Timing Clock Diagram

Figure 25 shows the FCC external clock.

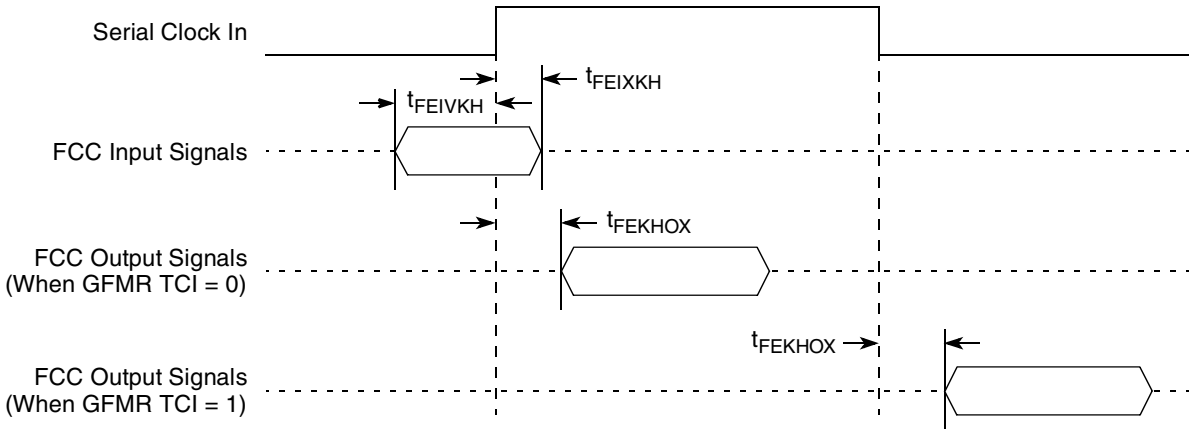


Figure 25. FCC External AC Timing Clock Diagram

Figure 26 shows Ethernet collision timing on FCCs.

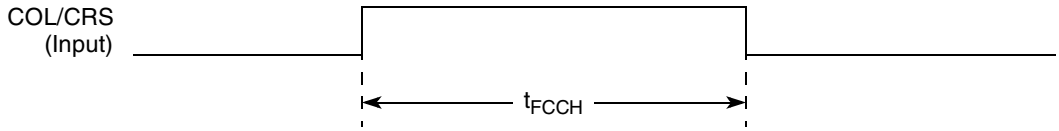
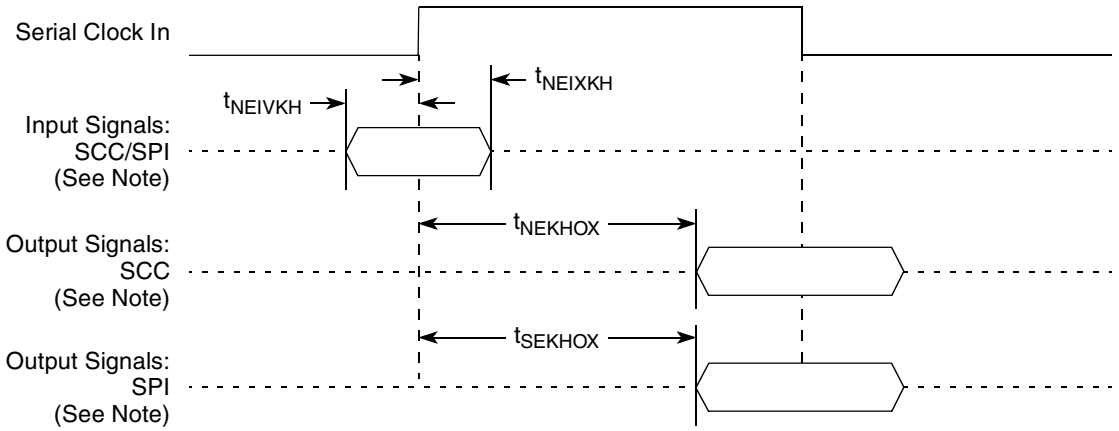


Figure 26. Ethernet Collision AC Timing Diagram (FCC)

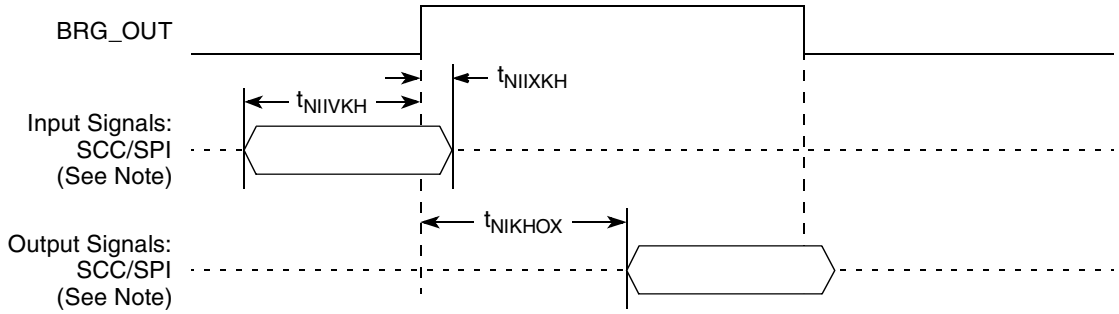
Figure 27 shows the SCC/SPI external clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 27. SCC/SPI AC Timing External Clock Diagram

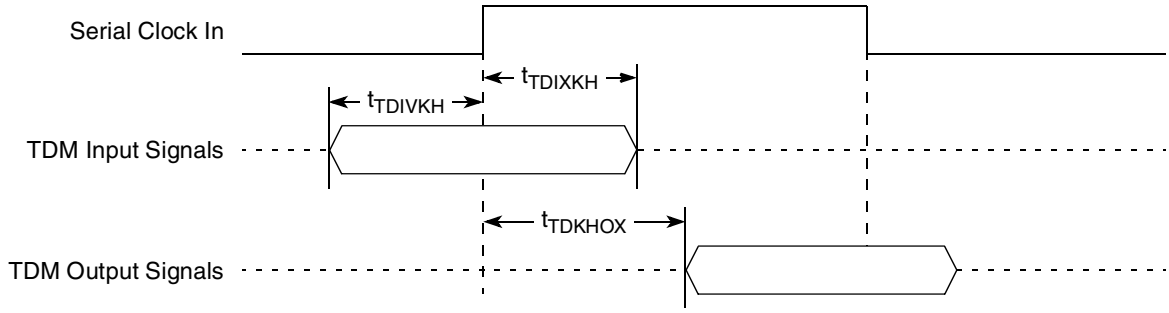
Figure 28 shows the SCC/SPI internal clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 28. SCC/SPI AC Timing Internal Clock Diagram

Figure 29 shows TDM input and output signals.



Note: There are 4 possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 29. TDM Signal AC Timing Diagram

Table 36 shows CPM I^{2}C AC Timing.

Table 36. CPM I^{2}C AC Timing

Characteristic	Symbol	Min	Max	Unit
SCL clock frequency (slave)	f_{SCL}	0	F_{MAX}[1]	Hz
SCL clock frequency (master)	f_{SCL}	BRGCLK/16512	BRGCLK/48	Hz
Bus free time between transmissions	t_{SDHDL}	1/(2.2 * f_{SCL})	—	s
Low period of SCL	t_{SCLCH}	1/(2.2 * f_{SCL})	—	s
High period of SCL	t_{SCHCL}	1/(2.2 * f_{SCL})	—	s
Start condition setup time [2]	t_{SCHDL}	2/(divider * f_{SCL})	—	s
Start condition hold time [2]	t_{SDLCL}	3/(divider * f_{SCL})	—	s
Data hold time [2]	t_{SCLDX}	2/(divider * f_{SCL})	—	s
Data setup time [2]	t_{SDVCH}	3/(divider * f_{SCL})	—	s
SDA/SCL rise time	t_{SRISE}	—	1/(10 * f_{SCL})	s
SDA/SCL fall time	t_{SFALL}	—	1/(33 * f_{SCL})	s
Stop condition setup time	t_{SCHDH}	2/(divider * f_{SCL})	—	s

Notes:

1. F_{MAX} = BRGCLK/(min_divider*prescaler). Where prescaler=25-I2MODE[PDIV]; and min_divider=12 if digital filter disabled and 18 if enabled.
   Example #1: if I2MODE[PDIV]=11 (prescaler=4) and I2MODE[FLT]=0 (digital filter disabled) then FMAX=BRGCLK/48
   Example #2: if I2MODE[PDIV]=00 (prescaler=32) and I2MODE[FLT]=1 (digital filter enabled) then FMAX=BRGCLK/576
2. divider = f_{SCL}/prescaler.
   In master mode: divider = BRGCLK/(f_{SCL}*prescaler) = 2*(I2BRG[DIV]+3)
   In slave mode: divider = BRGCLK/(f_{SCL}*prescaler)

Figure 30 is a a diagram of CPM I^{2}C Bus Timing.

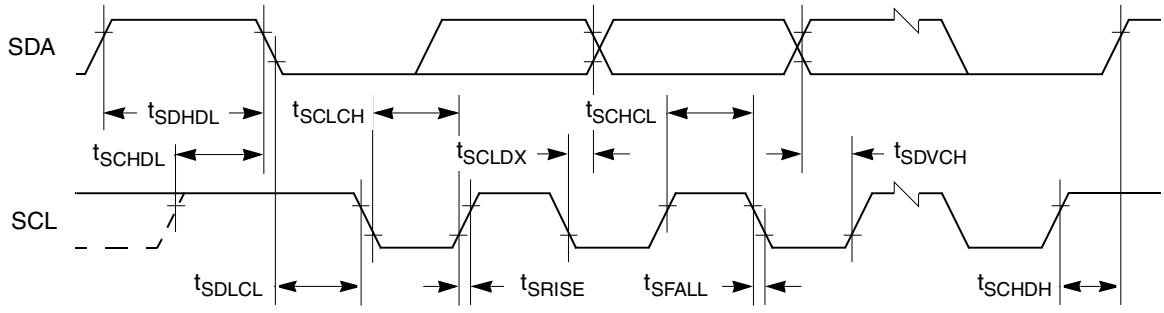


Figure 30. CPM I^{2}C Bus Timing Diagram

12.2 PCI/PCI-X AC Electrical Specifications

This section describes the general AC timing parameters of the PCI/PCI-X bus of the MPC8560. Note that the SYSCLK signal is used as the PCI input clock. Table 43 provides the PCI AC timing specifications at 66 MHz.

Table 43. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol [1]	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from SYSCLK	t_{PCKHOX}	2.0	—	ns	2, 9
SYSCLK to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3, 10
Input setup to SYSCLK	t_{PCIVKH}	3.0	—	ns	2, 4, 9
Input hold from SYSCLK	t_{PCIXKH}	0	—	ns	2, 4, 9
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ [9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	5, 6, 10
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	6, 10
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	7, 10

Notes:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI/PCI-X timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI/PCI-X timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 15, "Clocking."
6. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
7. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
8. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 µs.
9. Guaranteed by characterization.
10. Guaranteed by design.

- The peak differential signal of the transmitter output or receiver input, is A – B volts.
- The peak-to-peak differential signal of the transmitter output or receiver input, is 2 × (A – B) volts.

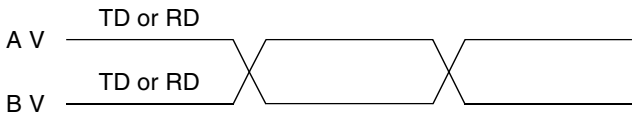


Figure 42. Differential Peak-to-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using numerical values, consider the case where a LVDS transmitter has a common mode voltage of 1.2 V and each signal has a swing that goes between 1.4 and 1.0 V. Using these values, the peak-to-peak voltage swing of the signals TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ is 400 mV. The differential signal ranges between 400 and –400 mV. The peak differential signal is 400 mV, and the peak-to-peak differential signal is 800 mV.

A timing edge is the zero-crossing of a differential signal. Each skew timing parameter on a parallel bus is synchronously measured on two signals relative to each other in the same cycle, such as data to data, data to clock, or clock to clock. A skew timing parameter may be relative to the edge of a signal or to the middle of two sequential edges.

Static skew represents the timing difference between signals that does not vary over time regardless of system activity or data pattern. Path length differences are a primary source of static skew.

Dynamic skew represents the amount of timing difference between signals that is dependent on the activity of other signals and varies over time. Crosstalk between signals is a source of dynamic skew.

Eye diagrams and compliance masks are a useful way to visualize and specify driver and receiver performance. This technique is used in several serial bus specifications. An example compliance mask is shown in Figure 43. The key difference in the application of this technique for a parallel bus is that the data is source synchronous to its bus clock while serial data is referenced to its embedded clock. Eye diagrams reveal the quality (cleanness, openness, goodness) of a driver output or receiver input. An advantage of using an eye diagram and a compliance mask is that it allows specifying the quality of a signal without requiring separate specifications for effects such as rise time, duty cycle distortion, data dependent dynamic skew, random dynamic skew, etc. This allows the individual semiconductor manufacturer maximum flexibility to trade off various performance criteria while keeping the system performance constant.

In using the eye pattern and compliance mask approach, the quality of the signal is specified by the compliance mask. The mask specifies the maximum permissible magnitude of the signal and the minimum permissible eye opening. The eye diagram for the signal under test is generated according to the specification. Compliance is determined by whether the compliance mask can be positioned over the eye diagram such that the eye pattern falls entirely within the unshaded portion of the mask.

Serial specifications have clock encoded with the data, but the LP-LVDS physical layer defined by RapidIO is a source synchronous parallel port so additional specifications to include effects that are not found in serial links are required. Specifications for the effect of bit to bit timing differences caused by static skew have been added and the eye diagrams specified are measured relative to the associated clock in order to include clock to data effects. With the transmit output (or receiver input) eye diagram, the user can determine if the transmitter output (or receiver input) is compliant with an oscilloscope with the appropriate software.

Table 50. RapidIO Driver AC Timing Specifications—1 Gbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential output high voltage	V_{OHD}	200	540	mV	1
Differential output low voltage	V_{OLD}	–540	–200	mV	1
Duty cycle	DC	48	52	%	2, 6
V_{OD} rise time, 20%–80% of peak to peak differential signal swing	t_{FALL}	100	—	ps	3, 6
V_{OD} fall time, 20%–80% of peak to peak differential signal swing	t_{RISE}	100	—	ps	6
Data valid	DV	575	—	ps	6
Skew of any two data outputs	t_{DPAIR}	—	100	ps	4, 6
Skew of single data outputs to associated clock	$t_{SKEW,PAIR}$	–100	100	ps	5, 6

Notes:

1.See Figure 44.

2.Requires ±100 ppm long term frequency stability.

3.Measured at V_{OD} = 0 V.

4.Measured using the RapidIO transmit mask shown in Figure 44.

5.See Figure 49.

6.Guaranteed by design.

The compliance of driver output signals TD[0:15] and TFRAME with their minimum data valid window (DV) specification shall be determined by generating an eye pattern for each of the data signals and comparing the eye pattern of each data signal with the RapidIO transmit mask shown in Figure 44. The value of X2 used to construct the mask shall be $(1 - DV_{min})/2$. A signal is compliant with the data valid window specification if the transmit mask can be positioned on the signal's eye pattern such that the eye pattern falls entirely within the unshaded portion of the mask.

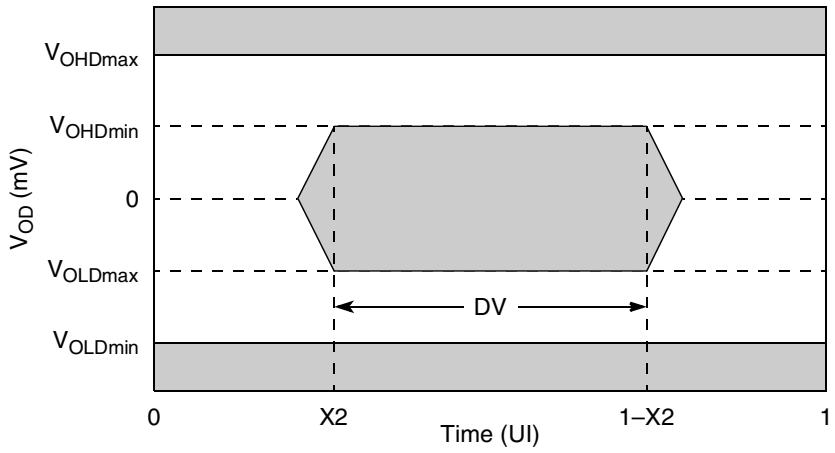


Figure 44. RapidIO Transmit Mask

3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
7. The socket lid must always be oriented to A1.

14.3 Pinout Listings

Table 54 provides the pin-out listing for the MPC8560, 783 FC-PBGA package.

Table 54. MPC8560 Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI/PCI-X				
PCI_AD[63:0]	AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14, V15, W15, Y15, AA15, AB15, AC15, AD15, AG15, AH15, V16, W16, AB16, AC16, AD16, AE16, AF16, V17, W17, Y17, AA17, AB17, AE17, AF17, AF18, AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9, AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11, AG11, AH11, V12, W12, Y12, AB12, AD12, AE12, AG12, AH12, V13, Y13, AB13, AC13	I/O	OV_{DD}	17
PCI_C_$\overline{BE}$[7:0]	AG13, AH13, V14, W14, AH8, AB10, AD11, AC12	I/O	OV_{DD}	17
PCI_PAR	AA11	I/O	OV_{DD}	—
PCI_PAR64	Y14	I/O	OV_{DD}	—
$\overline{\text{PCI\_FRAME}}$	AC10	I/O	OV_{DD}	2
$\overline{\text{PCI\_TRDY}}$	AG10	I/O	OV_{DD}	2
$\overline{\text{PCI\_IRDY}}$	AD10	I/O	OV_{DD}	2
$\overline{\text{PCI\_STOP}}$	V11	I/O	OV_{DD}	2
$\overline{\text{PCI\_DEVSEL}}$	AH10	I/O	OV_{DD}	2
PCI_IDSEL	AA9	I	OV_{DD}	—
$\overline{\text{PCI\_REQ64}}$	AE13	I/O	OV_{DD}	5, 10
$\overline{\text{PCI\_ACK64}}$	AD13	I/O	OV_{DD}	2
$\overline{\text{PCI\_PERR}}$	W11	I/O	OV_{DD}	2
$\overline{\text{PCI\_SERR}}$	Y11	I/O	OV_{DD}	2, 4
$\overline{\text{PCI\_REQ0}}$	AF5	I/O	OV_{DD}	—
$\overline{\text{PCI\_REQ}}$[1:4]	AF3, AE4, AG4, AE5	I	OV_{DD}	—
$\overline{\text{PCI\_GNT}}$[0]	AE6	I/O	OV_{DD}	—
$\overline{\text{PCI\_GNT}}$[1:4]	AG5, AH5, AF6, AG6	O	OV_{DD}	5, 9

Table 54. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface				
MDQ[0:63]	M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12	I/O	GV_{DD}	—
MECC[0:7]	N20, M20, L19, E19, C21, A21, G19, A19	I/O	GV_{DD}	—
MDM[0:8]	L24, H28, F24, L21, E18, E16, G14, B13, M19	O	GV_{DD}	—
MDQS[0:8]	L26, J25, D25, A22, H18, F16, F14, C13, C20	I/O	GV_{DD}	—
MBA[0:1]	B18, B19	O	GV_{DD}	—
MA[0:14]	N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13	O	GV_{DD}	—
$\overline{\text{MWE}}$	D17	O	GV_{DD}	—
$\overline{\text{MRAS}}$	F17	O	GV_{DD}	—
$\overline{\text{MCAS}}$	J16	O	GV_{DD}	—
$\overline{\text{MCS}}$[0:3]	H16, G16, J15, H15	O	GV_{DD}	—
MCKE[0:1]	E26, E28	O	GV_{DD}	11
MCK[0:5]	J20, H25, A15, D20, F28, K14	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	F20, G27, B15, E20, F27, L14	O	GV_{DD}	—
MSYNC_IN	M28	I	GV_{DD}	—
MSYNC_OUT	N28	O	GV_{DD}	—
Local Bus Controller Interface				
LA[27]	U18	O	OV_{DD}	5, 9
LA[28:31]	T18, T19, T20, T21	O	OV_{DD}	7, 9
LAD[0:31]	AD26, AD27, AD28, AC26, AC27, AC28, AA22, AA23, AA26, Y21, Y22, Y26, W20, W22, W26, V19, T22, R24, R23, R22, R21, R18, P26, P25, P20, P19, P18, N22, N23, N24, N25, N26	I/O	OV_{DD}	—
LALE	V21	O	OV_{DD}	8, 9
LBCTL	V20	O	OV_{DD}	9
LCKE	U23	O	OV_{DD}	—
LCLK[0:2]	U27, U28, V18	O	OV_{DD}	—
$\overline{\text{LCS}}$[0:4]	Y27, Y28, W27, W28, R27	O	OV_{DD}	18
$\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$	R28	I/O	OV_{DD}	1

15 Clocking

This section describes the PLL configuration of the MPC8560. Note that the platform clock is identical to the CCB clock.

15.1 Clock Ranges

Table 55 provides the clocking specifications for the processor core and Table 56 provides the clocking specifications for the memory bus.

Table 55. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	667 MHz		833 MHz		1 GHz			
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	400	667	400	833	400	1000	MHz	1, 2, 3

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, "Platform/System PLL Ratio," and Section 15.3, "e500 Core PLL Ratio," for ratio settings.
2.)The minimum e500 core frequency is based on the minimum platform frequency of 200 MHz.
3.)The 1.0 GHz core frequency is based on a 1.3 V VDD supply voltage.

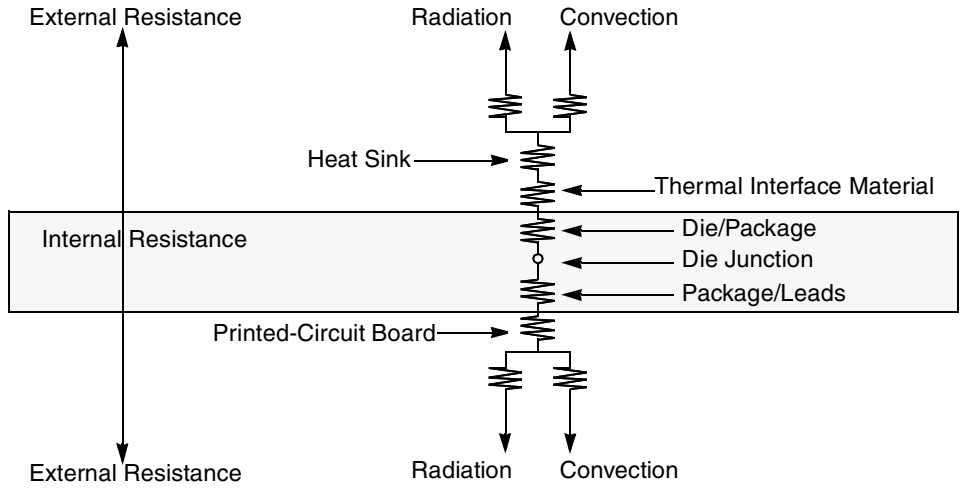
Table 56. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	667 MHz		833 MHz		1 GHz			
	Min	Max	Min	Max	Min	Max		
Memory bus frequency	100	166	100	166	100	166	MHz	1, 2, 3

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, "Platform/System PLL Ratio," and Section 15.3, "e500 Core PLL Ratio," for ratio settings.
2. The memory bus speed is half of the DDR data rate, hence, half of the platform clock frequency.
3.)The 1.0 GHz core frequency is based on a 1.3 V VDD supply voltage.

Figure 53 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 53. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

16.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 54 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 51). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink, the heat sink should be slowly removed. Heating the heat sink to 40-50°C with an air gun can soften the interface material and make the removal easier. The use of an adhesive for heat sink attach is not recommended.

Table 62. Document Revision History (continued)

Rev. No.	Substantive Change(s)
1.2	Section 1.1.1—Updated feature list. Section 1.2.1.1—Updated notes for Table 1. Section 1.2.1.2—Removed 5-V PCI interface overshoot and undershoot figure. Section 1.2.1.3—Added this section to summarize impedance driver settings for various interfaces. Section 1.4—Updated rows in Reset Initialization timing specifications table. Added a table with DLL and PLL timing specifications. Section 1.5.2.2—Updated note 6 of DDR SDRAM Output AC Timing Specifications table. Section 1.7—Changed the minimum input low current from -600 to -15 μA for the RGMII DC electrical characteristics. Section 1.7.2—Changed LCS[3:4] to TSEC1_TXD[6:5]. Updated notes regarding LCS[3:4]. Section 1.13.2—Updated the mechanical dimensions diagram for the package. Section 1.13.3—Updated the notes for LBCTL, TRIG_OUT, and ASLEEP. Corrected pin assignments for IIC_SDA and IIC_SCL. Corrected reserved pin assignment of V11 to U11. V11 is actually $\overline{\text{PCI\_STOP}}$. Section 1.14.1—Updated the table for frequency options with respect to platform/CCB frequencies. Section 1.14.4—Edited Frequency options with respect to memory bus speeds.
1.1	Made updates throughout document. Section 1.6.1—Added symbols and note for the GTX_CLK125 timing parameters. Section 1.11.3—Updated pin list table: LGPL5/LSDAMUX to LGPL5, LA[27:29] and LA[30:31] to LA[27:31], TRST to $\overline{\text{TRST}}$, added GBE Clocking section and EC_GTX_CLK125 signal. Figure 50—Updated pin 2 connection information.
1	Original Customer Version.

19 Device Nomenclature

Ordering information for the parts fully covered by this specification document is provided in Section 19.1, "Part Numbers Fully Addressed by this Document."

19.1 Part Numbers Fully Addressed by this Document

Table 63 provides the Freescale part numbering nomenclature for the MPC8560. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 63. Part Numbering Nomenclature

MPC	nnnn	t	pp	ff(f)	c	r
Product Code	**Part Identifier**	**Temperature Range [1]**	**Package [2]**	**Processor Frequency [3, 4]**	**Platform Frequency**	**Revision Level**
MPC	8560	Blank = 0 to 105°C C= -40 to 105°C	PX = FC-PBGA VT = FC-PBGA (Pb-free)	833 = 833 MHz 667 = 667 MHz	L = 333 MHz J= 266 MHz	B = Rev. 2.0 (SVR = 0x80700020) C = Rev. 2.1 (SVR = 0x80700021)
MPC	8560	Blank = 0 to 105°C C = –40 to 105°C	PX = FC-PBGA VT = FC-PBGA (Pb-free)	AQ = 1.0 GHz	F = 333 MHz	B = Rev. 2.0 (SVR = 0x80700020) C = Rev. 2.1 (SVR = 0x80700021)

Notes:

1. For Temperature Range=C, Processor Frequency is limited to 667 MHz.
2. See Section 14, "Package and Pin Listings" for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. The core must be clocked at a minimum frequency of 400 MHz. A device must not be used beyond the core frequency or platform frequency indicated on the device.
4. Designers should use the maximum power value corresponding to the core and platform frequency grades indicated on the device. A lower maximum power value should not be assumed for design purposes even when running at a lower frequency.

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