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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	833MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8560px833lb

  - Contiguous or discontiguous memory mapping
  - Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
  - Sleep mode support for self refresh SDRAM
  - Supports auto refreshing
  - On-the-fly power management using CKE signal
  - Registered DIMM support
  - Fast memory access via JTAG port
  - 2.5-V SSTL2 compatible I/O
- RapidIO interface unit
  - 8-bit RapidIO I/O and messaging protocols
  - Source-synchronous double data rate (DDR) interfaces
  - Supports small type systems (small domain, 8-bit device ID)
  - Supports four priority levels (ordering within a level)
  - Reordering across priority levels
  - Maximum data payload of 256 bytes per packet
  - Packet pacing support at the physical layer
  - CRC protection for packets
  - Supports atomic operations increment, decrement, set, and clear
  - LVDS signaling
- RapidIO–compliant message unit
  - One inbound data message structure (inbox)
  - One outbound data message structure (outbox)
  - Supports chaining and direct modes in the outbox
  - Support of up to 16 packets per message
  - Support of up to 256 bytes per packet and up to 4 Kbytes of data per message
  - Supports one inbound doorbell message structure
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts with 32-bit messages
  - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
  - Four global high resolution timers/counters that can generate interrupts
  - Supports 22 other internal interrupt sources
  - Supports fully nested interrupt delivery
  - Interrupts can be routed to external pin for external processing

  - Interrupts can be routed to the e500 core's standard or critical interrupt inputs
  - Interrupt summary registers allow fast identification of interrupt source
- I^2C controller
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the I^2C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I^2C addressing mode
  - Data integrity checked with preamble signature and CRC
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 166 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
  - Three protocol engines available on a per chip select basis:
    - General purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-,16-, or 32-bit)
- Two three-speed (10/100/1Gb) Ethernet controllers (TSECs)
  - Dual IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab compliant controllers
  - Support for different Ethernet physical interfaces:
    - 10/100/1Gb Mbps IEEE 802.3 GMII
    - 10/100 Mbps IEEE 802.3 MII
    - 10 Mbps IEEE 802.3 MII
    - 1000 Mbps IEEE 802.3z TBI
    - 10/100/1Gb Mbps RGMII/RTBI
  - Full- and half-duplex support
  - Buffer descriptors are backward compatible with MPC8260 and MPC860T 10/100 programming models
  - 9.6-Kbyte jumbo frame support
  - RMON statistics support
  - 2-Kbyte internal transmit and receive FIFOs

Table 16. DDR SDRAM Output AC Timing Specifications–DLL Mode (continued)

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDSHME}	1.5	4.0	ns	7, 8

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (OX or DX). For example, t_{DDKHOV} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (O) are valid (V) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. Maximum possible clock skew between a clock MCK[n] and its relative inverse clock $\overline{\text{MCK}}$[n], or between a clock MCK[n] and a relative clock MCK[m] or MSYNC_OUT. Skew measured between complementary signals at $GV_{DD}/2$.
4. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$ and MDQ/MECC/MDM/MDQS.
5. Note that t_{DDSHMH} follows the symbol conventions described in note 1. For example, t_{DDSHMH} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) until the MDQS signal is valid (MH). t_{DDSHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. These controls allow the relationship between the synchronous clock control timing and the source-synchronous DQS domain to be modified by the user. For best turnaround times, these may need to be set to delay t_{DDSHMH} an additional $0.25t_{MCK}$. This will also affect t_{DDSHMP} and t_{DDSHME} accordingly. See the *MPC8560 PowerQUICC III Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8560.
7. All outputs are referenced to the rising edge of MSYNC_IN (S) at the pins of the MPC8560. Note that t_{DDSHMP} follows the symbol conventions described in note 1. For example, t_{DDSHMP} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) for the duration of the MDQS signal precharge period (MP).
8. Guaranteed by design.
9. Guaranteed by characterization.

Figure 5 provides the AC test load for the DDR bus.

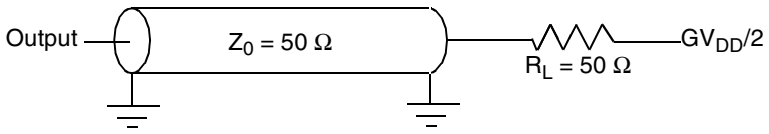


Figure 5. DDR AC Test Load

Table 17. DDR SDRAM Measurement Conditions

Symbol	DDR	Unit	Notes
V_{TH}	MV_{REF} ± 0.31 V	V	1
V_{OUT}	0.5 × GV_{DD}	V	2

Notes:

1. Data input threshold measurement point.
2. Data output measurement point.

Table 20. GMII, MII, RGMII, RTBI, and TBI DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	2.37	2.63	V
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V
Input high voltage	V_{IH}	1.70	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	–0.3	0.70	V
Input high current (V_{IN} [1] = LV_{DD})	I_{IH}	—	10	μA
Input low current (V_{IN} [1] = GND)	I_{IL}	–15	—	μA

Note:
1.Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1and Table 2.

7.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

7.2.1 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

7.2.1.1 GMII Transmit AC Timing Specifications

Table 21 provides the GMII transmit AC timing specifications.

Table 21. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	40	—	60	%
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX} [3]	0.5	—	5.0	ns

Figure 14 shows the RGMII and RTBI AC timing and multiplexing diagrams.

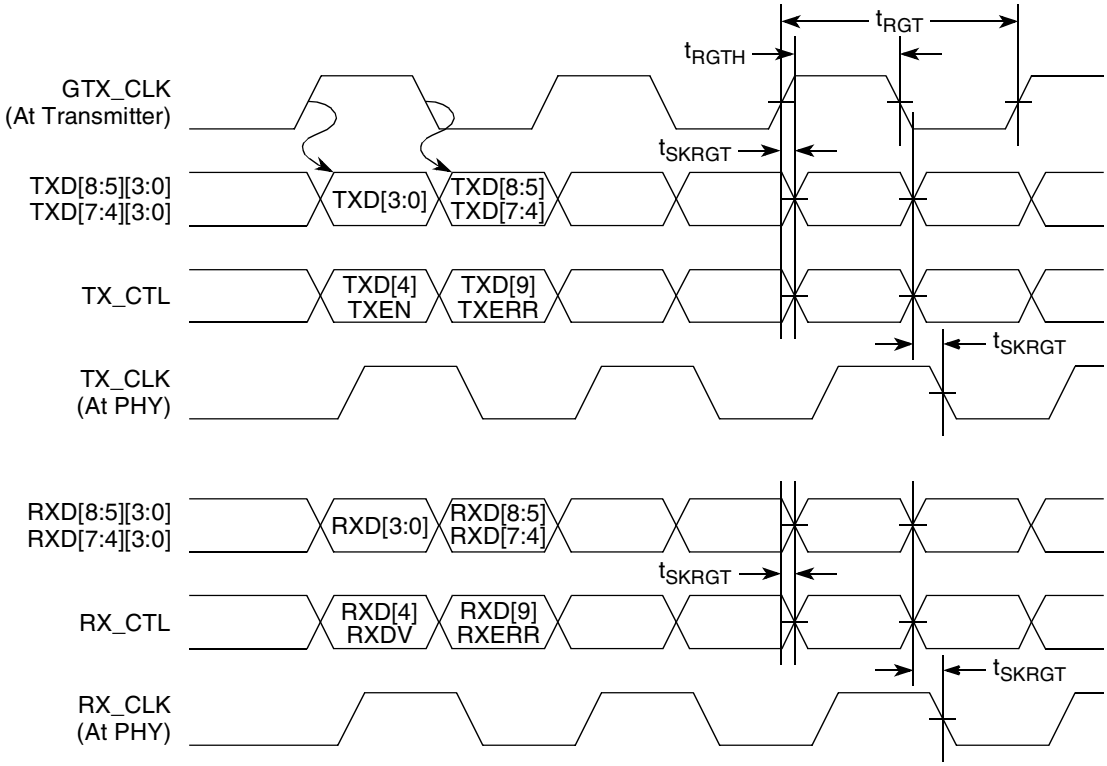


Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

7.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 7.1, "Three-Speed Ethernet Controller (TSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics."

7.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 28.

Table 28. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.13	3.47	V
Output high voltage (OV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	1.70	—	V
Input low voltage	V_{IL}	—	0.90	V

Table 28. MII Management DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit
Input high current (OV_{DD} = Max, V_{IN} [1] = 2.1 V)	I_{IH}	—	40	μA
Input low current (OV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA

Note:

1.Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.3.2 MII Management AC Electrical Specifications

Table 29 provides the MII management AC timing specifications.

Table 29. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	0.893	—	10.4	MHz	2, 4
MDC period	t_{MDC}	96	—	1120	ns	
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	
MDC to MDIO valid	t_{MDKHDV}			$2*[1/(f_{ccb\_clk}/8)]$	ns	3
MDC to MDIO delay	t_{MDKHDX}	10	—	$2*[1/(f_{ccb\_clk}/8)]$	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	
MDC rise time	t_{MDCR}	—	—	10	ns	4
MDC fall time	t_{MDHF}	—	—	10	ns	4

Notes:

1.The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2.This parameter is dependent on the CCB clock speed (that is, for a CCB clock of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a CCB clock of 333 MHz, the maximum frequency is 10.4 MHz and the minimum frequency is 1.5 MHz).

3.This parameter is dependent on the CCB clock speed (that is, for a CCB clock of 267 MHz, the delay is 60 ns and for a CCB clock of 333 MHz, the delay is 48 ns).

4.Guaranteed by design.

Table 31. Local Bus General Timing Parameters—DLL Enabled (continued)

Parameter	POR Configuration	Symbol [1]	Min	Max	Unit	Notes
Input setup to local bus clock (except LUPWAIT)	—	$t_{LBIVKH1}$	1.8	—	ns	4, 5, 8
LUPWAIT input setup to local bus clock	—	$t_{LBIVKH2}$	1.7	—	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	—	$t_{LBIXKH1}$	0.5	—	ns	4, 5, 8
LUPWAIT input hold from local bus clock	—	$t_{LBIXKH2}$	1.0	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	—	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKHOV1}$	—	2.0	ns	4, 8
	TSEC2_TXD[6:5] = 11 (default)			3.5		
Local bus clock to data valid for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKHOV2}$	—	2.2	ns	4, 8
	TSEC2_TXD[6:5] = 11 (default)			3.7		
Local bus clock to address valid for LAD	TSEC2_TXD[6:5] = 00	$t_{LBKHOV3}$	—	2.3	ns	4, 8
	TSEC2_TXD[6:5] = 11 (default)			3.8		
Local bus clock to LALE assertion		$t_{LBKHOV4}$	—	2.3	ns	4, 8
Output hold from local bus clock (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKHOX1}$	0.7	—	ns	4, 8
	TSEC2_TXD[6:5] = 11 (default)		1.6			
Output hold from local bus clock for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKHOX2}$	0.7	—	ns	4, 8
	TSEC2_TXD[6:5] = 11 (default)		1.6			
Local bus clock to output high Impedance (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKHOZ1}$	—	2.5	ns	7, 9
	TSEC2_TXD[6:5] = 11 (default)			3.8		

Table 31. Local Bus General Timing Parameters—DLL Enabled (continued)

Parameter	POR Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKHOZ2}$	—	2.5	ns	7, 9
	TSEC2_TXD[6:5] = 11 (default)			3.8		

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for DLL enabled mode.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $OV_{DD}/2$.
4. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for DLL enabled to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins TSEC2_TXD[6:5].
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.
9. Guaranteed by design.

Table 32 describes the general timing parameters of the local bus interface of the MPC8560 with the DLL bypassed.

Table 32. Local Bus General Timing Parameters—DLL Bypassed

Parameter	POR Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	—	t_{LBK}	6.0	—	ns	2
Internal launch/capture clock to LCLK delay	—	t_{LBKHKT}	2.3	3.9	ns	8
LCLK[n] skew to LCLK[m] or LSYNC_OUT	—	$t_{LBKSKEW}$	—	150	ps	3, 9
Input setup to local bus clock (except LUPWAIT)	—	$t_{LBIVKH1}$	5.7	—	ns	4, 5
LUPWAIT input setup to local bus clock	—	$t_{LBIVKH2}$	5.6	—	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	—	$t_{LBIXKH1}$	-1.8	—	ns	4, 5
LUPWAIT input hold from local bus clock	—	$t_{LBIXKH2}$	-1.3	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	—	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKLOV1}$	—	-0.3	ns	4
	TSEC2_TXD[6:5] = 11 (default)			1.2		

Table 36 shows CPM I^{2}C AC Timing.

Table 36. CPM I^{2}C AC Timing

Characteristic	Symbol	Min	Max	Unit
SCL clock frequency (slave)	f_{SCL}	0	F_{MAX}[1]	Hz
SCL clock frequency (master)	f_{SCL}	BRGCLK/16512	BRGCLK/48	Hz
Bus free time between transmissions	t_{SDHDL}	1/(2.2 * f_{SCL})	—	s
Low period of SCL	t_{SCLCH}	1/(2.2 * f_{SCL})	—	s
High period of SCL	t_{SCHCL}	1/(2.2 * f_{SCL})	—	s
Start condition setup time [2]	t_{SCHDL}	2/(divider * f_{SCL})	—	s
Start condition hold time [2]	t_{SDLCL}	3/(divider * f_{SCL})	—	s
Data hold time [2]	t_{SCLDX}	2/(divider * f_{SCL})	—	s
Data setup time [2]	t_{SDVCH}	3/(divider * f_{SCL})	—	s
SDA/SCL rise time	t_{SRISE}	—	1/(10 * f_{SCL})	s
SDA/SCL fall time	t_{SFALL}	—	1/(33 * f_{SCL})	s
Stop condition setup time	t_{SCHDH}	2/(divider * f_{SCL})	—	s

Notes:

1. F_{MAX} = BRGCLK/(min_divider*prescaler). Where prescaler=25-I2MODE[PDIV]; and min_divider=12 if digital filter disabled and 18 if enabled.
   Example #1: if I2MODE[PDIV]=11 (prescaler=4) and I2MODE[FLT]=0 (digital filter disabled) then FMAX=BRGCLK/48
   Example #2: if I2MODE[PDIV]=00 (prescaler=32) and I2MODE[FLT]=1 (digital filter enabled) then FMAX=BRGCLK/576
2. divider = f_{SCL}/prescaler.
   In master mode: divider = BRGCLK/(f_{SCL}*prescaler) = 2*(I2BRG[DIV]+3)
   In slave mode: divider = BRGCLK/(f_{SCL}*prescaler)

Figure 30 is a a diagram of CPM I^{2}C Bus Timing.

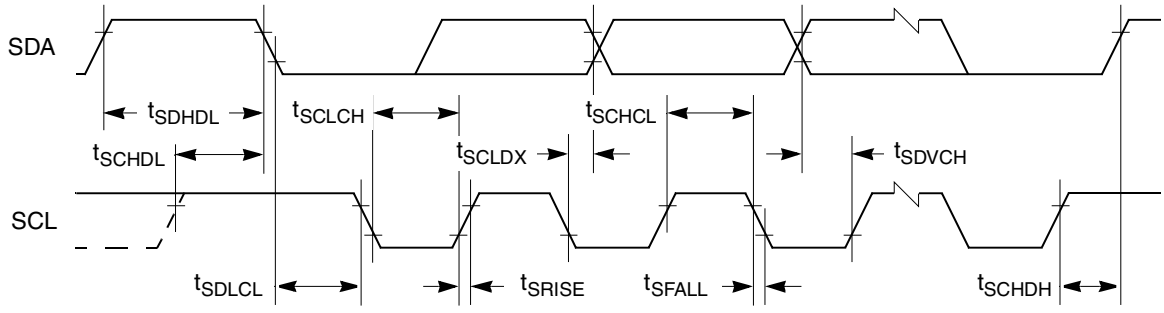


Figure 30. CPM I^{2}C Bus Timing Diagram

Table 37 and Table 38 are examples of I^2C AC parameters at I^2C clock value of 100 kHz and 400 kHz respectively.

Table 37. CPM I^2C AC Timing (f_{SCL} = 100 kHz)

Characteristic	Symbol	Min	Max	Unit
SCL clock frequency (slave)	f_{SCL}	—	100	KHz
SCL clock frequency (master)	f_{SCL}	—	100	KHz
Bus free time between transmissions	t_{SDHDL}	4.7	—	µs
Low period of SCL	t_{SCLCH}	4.7	—	µs
High period of SCL	t_{SCHCL}	4	—	µs
Start condition setup time [2]	t_{SCHDL}	2	—	µs
Start condition hold time [2]	t_{SDLCL}	3	—	µs
Data hold time [2]	t_{SCLDX}	2	—	µs
Data setup time [2]	t_{SDVCH}	3	—	µs
SDA/SCL rise time	t_{SRISE}	—	1	µs
SDA/SCL fall time	t_{SFALL}	—	303	ns
Stop condition setup time	t_{SCHDH}	2	—	µs

Table 38. CPM I^2C AC Timing (f_{SCL} = 400 kHz)

Characteristic	Symbol	Min	Max	Unit
SCL clock frequency (slave)	f_{SCL}	—	400	KHz
SCL clock frequency (master)	f_{SCL}	—	400	KHz
Bus free time between transmissions	t_{SDHDL}	1.2	—	µs
Low period of SCL	t_{SCLCH}	1.2	—	µs
High period of SCL	t_{SCHCL}	1	—	µs
Start condition setup time [2]	t_{SCHDL}	420	—	ns
Start condition hold time [2]	t_{SDLCL}	630	—	ns
Data hold time [2]	t_{SCLDX}	420	—	ns
Data setup time [2]	t_{SDVCH}	630	—	ns
SDA/SCL rise time	t_{SRISE}	—	250	ns
SDA/SCL fall time	t_{SFALL}	—	75	ns
Stop condition setup time	t_{SCHDH}	420	—	ns

Table 44. PCI-X AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	—	clocks	11
$\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time	t_{PCRHIX}	0	50	ns	6, 11

Notes:

1.See the timing measurement conditions in the *PCI-X 1.0a Specification*.

2.Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.

3.Setup time for point-to-point signals applies to $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ only. All other signals are bused.

4.For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

5.Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.

6.Maximum value is also limited by delay to the first transaction (time for $\overline{\text{HRESET}}$ high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of $\overline{\text{HRESET}}$ must be negated no later than two clocks before the first $\overline{\text{FRAME}}$ and must be floated no later than one clock before $\overline{\text{FRAME}}$ is asserted.

7.A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.

8.Device must meet this specification independent of how many outputs switch simultaneously.

9.The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*

10.Guaranteed by characterization.

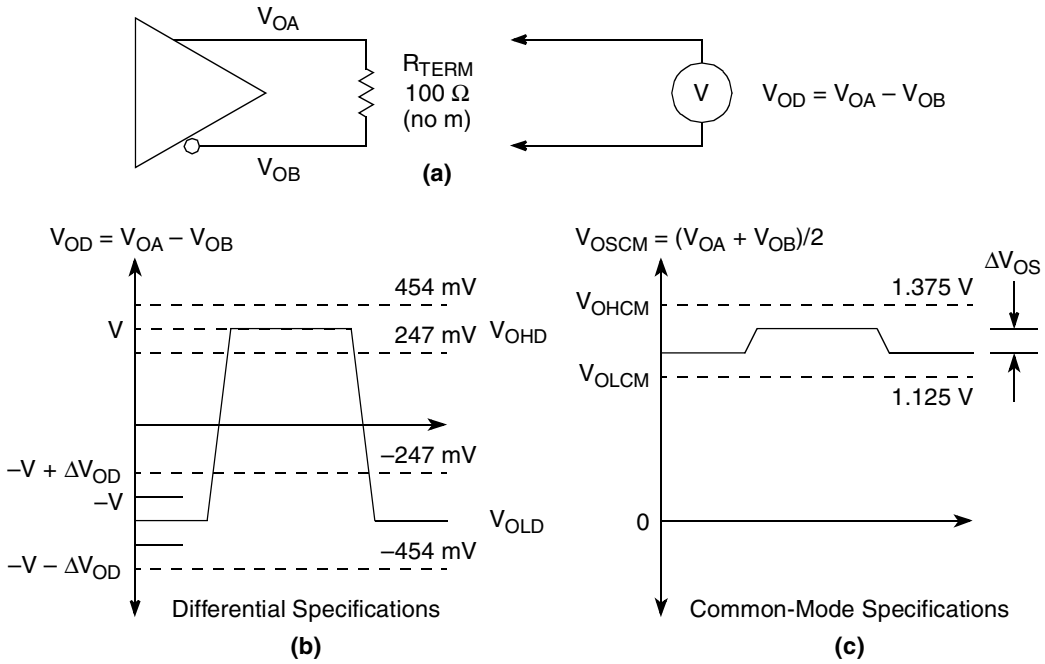
11.Guaranteed by design.

Table 45 provides the PCI-X AC timing specifications at 133 MHz.

Table 45. PCI-X AC Timing Specifications at 133 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	—	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t_{PCKHOX}	0.7	—	ns	1, 11
SYSCLK to output high impedance	t_{PCKHOZ}	—	7	ns	1, 4, 8, 12
Input setup time to SYSCLK	t_{PCIVKH}	1.4	—	ns	3, 5, 9, 11
Input hold time from SYSCLK	t_{PCIXKH}	0.5	—	ns	11
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time	t_{PCRVRH}	10	—	clocks	12
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	12
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	10, 12
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	—	clocks	12

Figure 41 shows the DC driver signal levels.



Note: V_{OA} refers to voltage at output A; V_{OB} refers to voltage at output B.

Figure 41. DC Driver Signal Levels

13.2 RapidIO AC Electrical Specifications

This section contains the AC electrical specifications for a RapidIO 8/16 LP-LVDS device. The interface defined is a parallel differential low-power high-speed signal interface. Note that the source of the transmit clock on the RapidIO interface is dependent on the settings of the LGPL[0:1] signals at reset. Note that the default setting makes the core complex bus (CCB) clock the source of the transmit clock. See Chapter 4 of the Reference Manual for more details on reset configuration settings.

13.3 RapidIO Concepts and Definitions

This section specifies signals using differential voltages. Figure 42 shows how the signals are defined. The figure shows waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- The transmitter output and receiver input signals TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ each have a peak-to-peak swing of A-B volts.
- The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} - V_{\overline{TD}}$.
- The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} - V_{\overline{RD}}$.
- The differential output signal of the transmitter or input signal of the receiver, ranges from A – B volts to – (A – B) volts.

13.3.2 RapidIO Receiver AC Timing Specifications

The RapidIO receiver AC timing specifications are provided in Table 51. A receiver shall comply with the specifications for each data rate/frequency for which operation of the receiver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The specifications apply over the receiver common mode and differential input voltage ranges.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7])

Table 51. RapidIO Receiver AC Timing Specifications—500 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1, 5
Data valid	DV	1080		ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}	—	380	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–300	300	ps	4

Notes:
1.Measured at V_{ID} = 0 V.
2.Measured using the RapidIO receive mask shown in Figure 46.
3.See Figure 49.
4.See Figure 48 and Figure 49.
5.Guaranteed by design.

Table 52. RapidIO Receiver AC Timing Specifications—750 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1, 5
Data valid	DV	600	—	ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}	—	400	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–267	267	ps	4

Notes:
1.Measured at V_{ID} = 0 V.
2.Measured using the RapidIO receive mask shown in Figure 46.
3.See Figure 49.
4.See Figure 48 and Figure 49.
5.Guaranteed by design.

14.2 Mechanical Dimensions of the MPC8560 FC-PBGA

Figure 50 the mechanical dimensions and bottom surface nomenclature of the MPC8560, 783 FC-PBGA package.

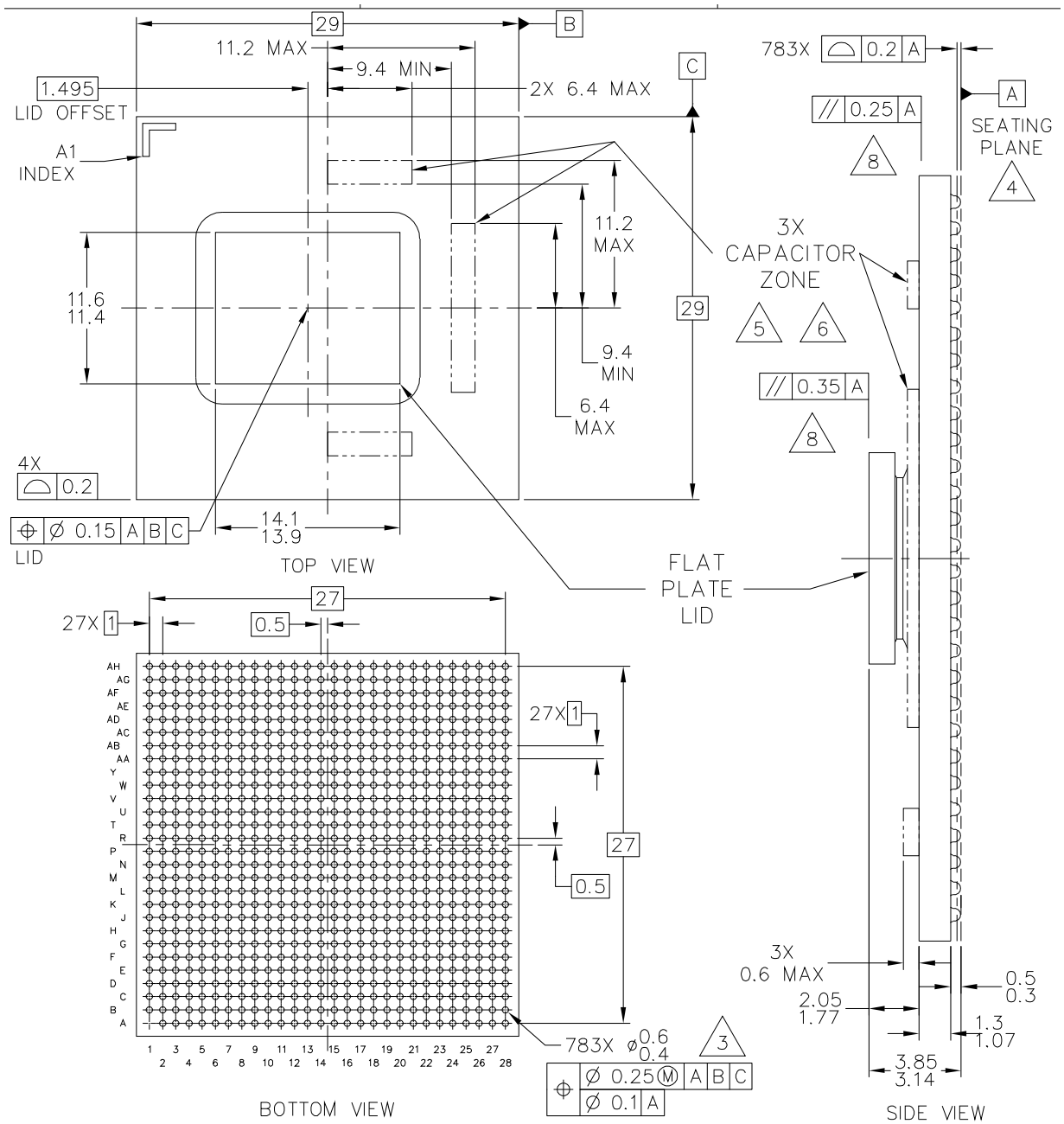


Figure 50. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8560 FC-PBGA

NOTES

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.

15 Clocking

This section describes the PLL configuration of the MPC8560. Note that the platform clock is identical to the CCB clock.

15.1 Clock Ranges

Table 55 provides the clocking specifications for the processor core and Table 56 provides the clocking specifications for the memory bus.

Table 55. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	667 MHz		833 MHz		1 GHz			
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	400	667	400	833	400	1000	MHz	1, 2, 3

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, "Platform/System PLL Ratio," and Section 15.3, "e500 Core PLL Ratio," for ratio settings.
2.)The minimum e500 core frequency is based on the minimum platform frequency of 200 MHz.
3.)The 1.0 GHz core frequency is based on a 1.3 V VDD supply voltage.

Table 56. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	667 MHz		833 MHz		1 GHz			
	Min	Max	Min	Max	Min	Max		
Memory bus frequency	100	166	100	166	100	166	MHz	1, 2, 3

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, "Platform/System PLL Ratio," and Section 15.3, "e500 Core PLL Ratio," for ratio settings.
2. The memory bus speed is half of the DDR data rate, hence, half of the platform clock frequency.
3.)The 1.0 GHz core frequency is based on a 1.3 V VDD supply voltage.

15.4 Frequency Options

Table 59 shows the expected frequency values for the platform frequency when using a CCB to SYSCLK ratio in comparison to the memory bus speed.

Table 59. Frequency Options with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)								
	16.67	25	33.33	41.63	66.67	83	100	111	133.33
	Platform/CCB Frequency (MHz)								
2							200	222	267
3					200	250	300	333	
4					267	333			
5				208	333				
6			200	250					
8		200	267	333					
9		225	300						
10		250	333						
12	200	300							
16	267								

16 Thermal

This section describes the thermal specifications of the MPC8560.

16.1 Thermal Characteristics

Table 60 provides the package thermal characteristics for the MPC8560.

Table 60. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection on four layer board (2s2p)	$R_{\theta JMA}$	16	°C/W	1, 2
Junction-to-ambient (@100 ft/min or 0.5 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	14	°C/W	1, 2
Junction-to-ambient (@200 ft/min or 1 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	12	°C/W	1, 2
Junction-to-board thermal	$R_{\theta JB}$	7.5	°C/W	3

Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-millennium.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the MPC8560 to function in various environments.

16.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8560 thermal model is shown in Figure 52. Five cuboids are used to represent this device. To simplify the model, the solder balls and substrate are modeled as a single block 29x29x1.47 mm with the conductivity adjusted accordingly. For modeling, the planar dimensions of the die are rounded to the nearest mm, so the die is modeled as 10x12 mm at a thickness of 0.76 mm. The bump/underfill layer is modeled as a collapsed resistance between the die and substrate assuming a conductivity of 0.6 in-plane and 1.9 W/m•K in the thickness dimension of 0.76 mm. The lid attach adhesive is also modeled as a collapsed resistance with dimensions of 10x12x0.050 mm and the conductivity of 1 W/m•K. The nickel plated copper lid is modeled as 12x14x1 mm. Note that the die and lid are not centered on the substrate; there is a 1.5 mm offset documented in the case outline drawing in Figure 50.

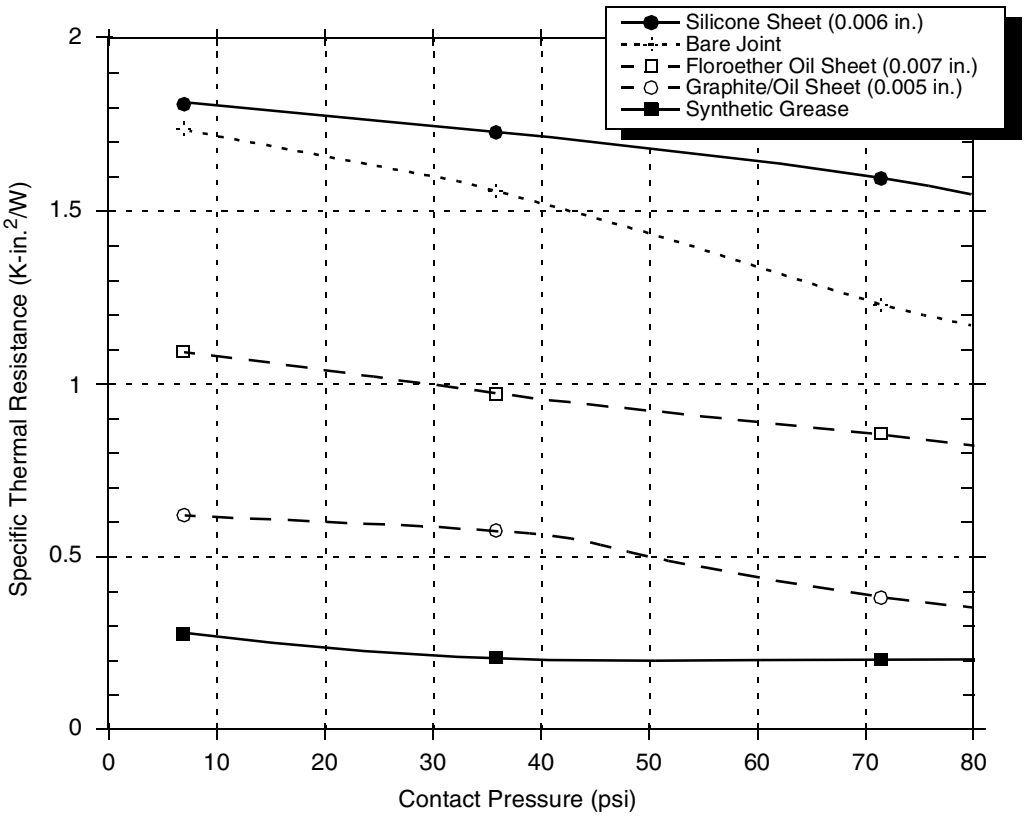


Figure 54. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

Table 62. Document Revision History (continued)

Rev. No.	Substantive Change(s)
3.2	Updated Table 1 and Table 2 with 1.0 GHz device parameter requirements. Added Section 2.1.2, “Power Sequencing”. Added CPM port signal drive strength to Table 3. Updated Table 4 with Maximum power data. Updated Table 4 and Table 5 with 1 GHz speed grade information. Updated Table 6 with corrected typical I/O power numbers. Updated Table 7 Note 2 lower voltage measurement point. Replaced Table 7 Note 5 with spread spectrum clocking guidelines. Added to Table 8 rise and fall time information. Added Section 4.4, “Real Time Clock Timing”. Added precharge information to Section 6.2.2, “DDR SDRAM Output AC Timing Specifications”. Removed V_{IL} and V_{IH} references from Table 21, Table 22, Table 23, and Table 24. Added reference level note to Table 21, Table 22, Table 23, Table 24, Table 25, Table 26, and Table 27. Updated TXD references to TCG in Section 7.2.3.1, “TBI Transmit AC Timing Specifications”. Updated t_{TTKHDX} value in Table 25. Updated PMA_RX_CLK references to RX_CLK in Section 7.2.3.2, “TBI Receive AC Timing Specifications”. Updated RXD references to RCG in Section 7.2.3.2, “TBI Receive AC Timing Specifications”. Updated Table 27 Note 2. Corrected Table 29 f_{MDC} and t_{MDC} to reflect the correct minimum operating frequency. Updated Table 29 t_{MDKHDV} and t_{MDKHDX} values for clarification. Added t_{LBKHKT} and updated Note 2 in Table 32. Corrected $\overline{\text{LGTA}}$ timing references in Figure 17. Updated Figure 18, Figure 20, and Figure 22. Corrected FCC output timing reference labels in Figure 24 and Figure 25. Updated Figure 50. Clarified Table 54 Note 5. Updated Table 55 and Table 56 with 1 GHz information. Added heat sink removal discussion to Section 16.2.3, “Thermal Interface Materials”. Corrected and added 1 GHz part number to Table 63.
3.1	Updated Table 4 and Table 5. Added Table 6. Added MCK duty cycle to Table 16. Updated f_{MDC}, t_{MDC}, t_{MDKHDV}, and t_{MDKHDX} parameters in Table 29. Added LALE to $t_{LBKHOV3}$ parameter in Table 31 and Table 32, and updated Figure 17. Corrected active level designations of some of the pins in Table 54. Updated Table 63.

Table 62. Document Revision History (continued)

Rev. No.	Substantive Change(s)
2.0	Section 1.1—Updated features list to coincide with latest version of the reference manual Table 1 and Table 2— Addition of CPM to OV_{DD} and OV_{IN}; Addition of SYSCLK to OV_{IN} Table 2—Addition of notes 1 and 2 Table 3—Addition of note 1 Table 5—New Section 4—New Table 13—Addition of I_{VREF} Table 15—Modified maximum values for t_{DISKEW} Table 16—Added MSYNC_OUT to $t_{MCKSKEW2}$ Figure 5—New Section 6.2.1—Removed Figure 4, "DDR SDRAM Input Timing Diagram" Section 7.1—Removed references to 2.5 V from first paragraph Figure 8—New Table 19 and Table 20—Modified “conditions” for I_{IH} and I_{IL} Table 21—Addition of min and max for GTX_CLK125 reference clock duty cycle Table 25—Addition of min and max for GTX_CLK125 reference clock duty cycle Table 27—Addition of min and max for GTX_CLK125 reference clock duty cycle Figure 17 and Figure 19—Changed LSYNC_IN to Internal clock at top of each figure Table 34—Modified values for t_{FIIVKH}, t_{NIIVKH}, and t_{TDIVKH}; addition of t_{PIIVKH} and t_{PIIXKH}. Table 35—Modified values for t_{FEKHOX}, t_{NIKHOX},t_{NEKHOX}, t_{TDKHOX}; addition of t_{PIKHOX}. Figure 16—New Figure 30—New Figure 16—New Figure 16—New Table 31—Removed row for $t_{LBKHOX3}$ Table 44—New (AC timing of PCI-X at 66 MHz) Table 54—Addition of note 19 Figure 61—Addition of jumper and note at top of diagram Table 56—Changed max bus freq for 667 core to 166 Section 16.2.1—Modified first paragraph Figure 52—Modified Figure 53—New Table 60—Modified thermal resistance data Section 16.2.4.2—Modified first and second paragraphs