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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 833MHz |
| Co-Processors/DSP | Communications; CPM |
| RAM Controllers | DDR, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | - |
| Voltage - I/O | 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 783-BFBGA, FCBGA |
| Supplier Device Package | 783-FCPBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8560px833lc |

# 1 Overview

The following section provides a high-level overview of the MPC8560 features. Figure 1 shows the major functional units within the MPC8560.

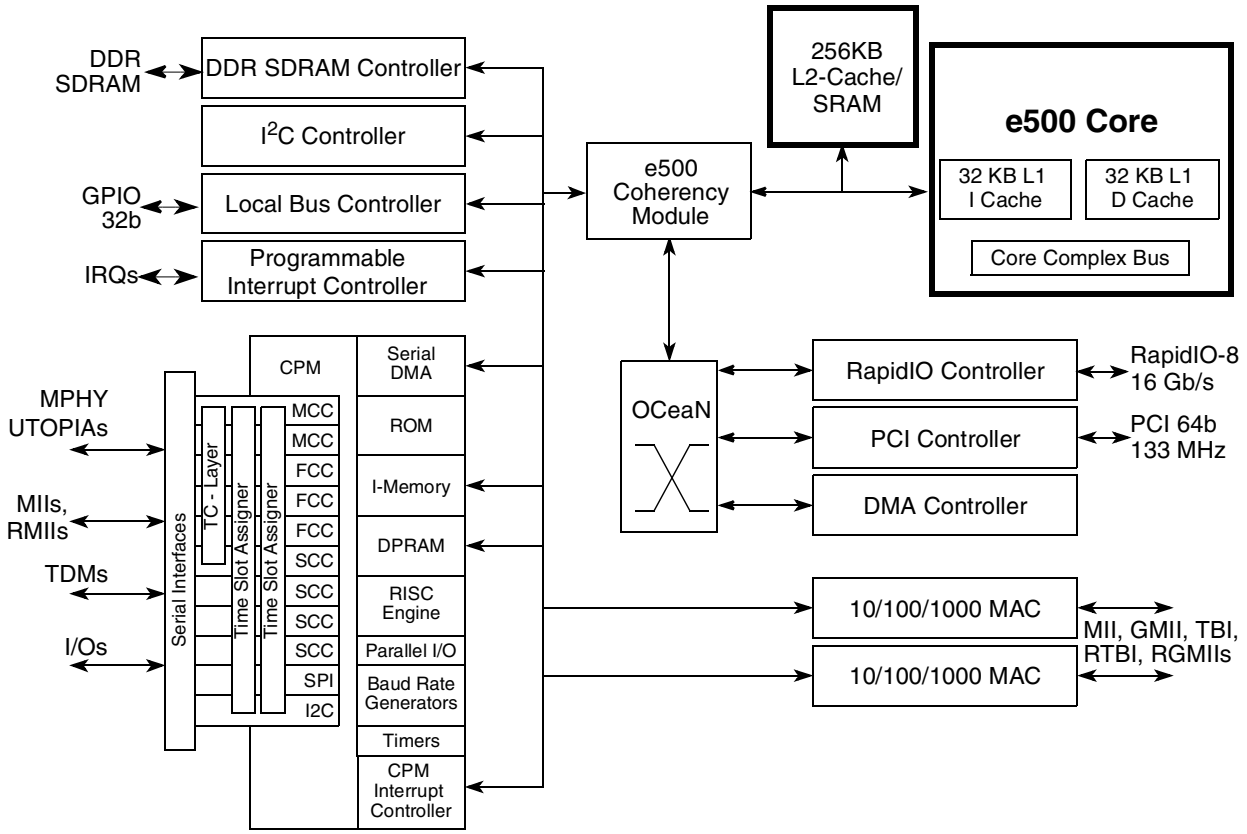



**Figure 1. MPC8560 Block Diagram**

## 1.1 Key Features

The following lists an overview of the MPC8560 feature set.

- High-performance, 32-bit Book E–enhanced core that implements the Power Architecture
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis. Separate locking for instructions and data
  - Memory management unit (MMU) especially designed for embedded applications
  - Enhanced hardware and software debug support
  - Performance monitor facility (similar to but different from the MPC8560 performance monitor described in Chapter 18, “Performance Monitor.”
- High-performance RISC CPM operating at up to 333 MHz
  - CPM software compatibility with previous PowerQUICC families
  - One instruction per clock

# 3 Power Characteristics

The estimated power dissipation on the $V_{DD}$ supply for the MPC8560 is shown in Table 4.

**Table 4. MPC8560 $V_{DD}$ Power Dissipation [1,2]**

| CCB Frequency (MHz) | Core Frequency (MHz) | Typical Power[3,4] | Maximum Power[5] | Unit |
|---|---|---|---|---|
| 200 | 400 | 5.1 | 7.7 | W |
| | 500 | 5.4 | 8.0 | |
| | 600 | 5.8 | 8.4 | |
| 267 | 533 | 6.0 | 8.7 | W |
| | 667 | 6.4 | 9.2 | |
| | 800 | 6.9 | 10.7 | |
| 333 | 667 | 6.8 | 9.8 | W |
| | 833 | 7.4 | 11.4 | |
| | 1000 [6] | 11.9 | 16.5 | |

**Notes:**

1. The values do not include I/O supply power ($OV_{DD}$, $LV_{DD}$, $GV_{DD}$) or $AV_{DD}$.
2. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, air flow, power dissipation of other components on the board, and board thermal resistance. Any customer design must take these considerations into account to ensure the maximum 105 °C junction temperature is not exceeded on this device.
3. Typical Power is based on a nominal voltage of $V_{DD}$ = 1.2 V, a nominal process, a junction temperature of $T_j$ = 105 °C, and a Dhrystone 2.1 benchmark application.
4. Thermal solutions will likely need to design to a number higher than Typical Power based on the end application, $T_A$ target, and I/O power.
5. Maximum power is based on a nominal voltage of $V_{DD}$ = 1.2 V, worst case process, a junction temperature of $T_j$ = 105 °C, and an artificial smoke test.
6. The nominal recommended $V_{DD}$ is 1.3 V for this speed grade.

The estimated power dissipation on the $AV_{DD}$ supplies for the MPC8560 PLLs is shown in Table 5.

**Table 5. MPC8560 $AV_{DD}$ Power Dissipation**

| $AV_{DD}n$ | Typical[1] | Unit |
|---|---|---|
| $AV_{DD}1$ | 0.007 | W |
| $AV_{DD}2$ | 0.014 | W |
| $AV_{DD}3$ | 0.004 | W |

**Notes:**

1. $V_{DD}$ = 1.2 V(1.3 V for 1.0 GHz device), $T_J$ = 105°C

Table 6 provides estimated I/O power numbers for each block: DDR, PCI, Local Bus, RapidIO, TSEC, and CPM.

**Table 6. Estimated Typical I/O Power Consumption**

| Interface | Parameter | $GV_{DD}$ (2.5 V) | $OV_{DD}$ (3.3 V) | $LV_{DD}$ (3.3 V) | $LV_{DD}$ (2.5 V) | Units | Notes |
|---|---|---|---|---|---|---|---|
| DDR I/O | CCB = 200 MHz | 0.46 | — | — | — | W | 1 |
| | CCB = 266 MHz | 0.59 | — | — | — | | |
| | CCB = 300 MHz | 0.66 | — | — | — | | |
| | CCB = 333 MHz | 0.73 | — | — | — | | |
| PCI/PCI-X I/O | 32-bit, 33 MHz | — | 0.04 | — | — | W | 2 |
| | 32-bit 66 MHz | — | 0.07 | — | — | | |
| | 64-bit, 66 MHz | — | 0.14 | — | — | | |
| | 64-bit, 133 MHz | — | 0.25 | — | — | | |
| Local Bus I/O | 32-bit, 33 MHz | — | 0.07 | — | — | W | 3 |
| | 32-bit, 66 MHz | — | 0.13 | — | — | | |
| | 32-bit, 133 MHz | — | 0.24 | — | — | | |
| | 32-bit, 167 MHz | — | 0.30 | — | — | | |
| RapidIO I/O | 500 MHz data rate | — | 0.96 | — | — | W | 4 |
| TSEC I/O | MII | — | — | 10 | — | mW | 5, 6 |
| | GMII, TBI (2.5 V) | — | — | — | 40 | | |
| | GMII, TBI (3.3 V) | — | — | 70 | — | | |
| | RGMII, RTBI | — | — | — | 40 | | |
| CPM-FCC | MII | — | 15 | — | — | mW | 7 |
| | RMII | — | 13 | — | — | | |
| | HDLC 16 Mbps | — | 9 | — | — | | |
| | UTOPIA-8 SPHY | — | 60 | — | — | | |
| | UTOPIA-8 MPHY | — | 100 | — | — | | |
| | UTOPIA-16 SPHY | — | 94 | — | — | | |
| | UTOPIA-16 MPHY | — | 135 | — | — | | |
| CPM-SCC | HDLC 16 Mbps | — | 4 | — | — | mW | 7 |

**Table 31. Local Bus General Timing Parameters—DLL Enabled (continued)**

| Parameter | POR Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Local bus clock to output high impedance for LAD/LDP | TSEC2_TXD[6:5] = 00 | $t_{LBKHOZ2}$ | — | 2.5 | ns | 7, 9 |
| | TSEC2_TXD[6:5] = 11 (default) | | | 3.8 | | |

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for DLL enabled mode.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $OV_{DD}/2$.
4. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for DLL enabled to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of $t_{LBOTOT}$ is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins TSEC2_TXD[6:5].
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.
9. Guaranteed by design.

Table 32 describes the general timing parameters of the local bus interface of the MPC8560 with the DLL bypassed.

**Table 32. Local Bus General Timing Parameters—DLL Bypassed**

| Parameter | POR Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Local bus cycle time | — | $t_{LBK}$ | 6.0 | — | ns | 2 |
| Internal launch/capture clock to LCLK delay | — | $t_{LBKHKT}$ | 2.3 | 3.9 | ns | 8 |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | — | $t_{LBKSKEW}$ | — | 150 | ps | 3, 9 |
| Input setup to local bus clock (except LUPWAIT) | — | $t_{LBIVKH1}$ | 5.7 | — | ns | 4, 5 |
| LUPWAIT input setup to local bus clock | — | $t_{LBIVKH2}$ | 5.6 | — | ns | 4, 5 |
| Input hold from local bus clock (except LUPWAIT) | — | $t_{LBIXKH1}$ | -1.8 | — | ns | 4, 5 |
| LUPWAIT input hold from local bus clock | — | $t_{LBIXKH2}$ | -1.3 | — | ns | 4, 5 |
| LALE output transition to LAD/LDP output transition (LATCH hold time) | — | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | TSEC2_TXD[6:5] = 00 | $t_{LBKLOV1}$ | — | -0.3 | ns | 4 |
| | TSEC2_TXD[6:5] = 11 (default) | | | 1.2 | | |

**Table 33. CPM DC Electrical Characteristics (continued)**

| Characteristic | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Output high voltage ($I_{OH}$ = –2.0 mA) | $V_{OH}$ | 2.4 | — | V | 1 |
| Output low voltage ($I_{OL}$ = 3.2 mA) | $V_{OL}$ | — | 0.4 | V | 1 |

**Note:**
1. This specification applies to the following pins: PA[0–31], PB[4–31], PC[0–31], and PD[4–31].
2. $V_{IL}$(max) for the IIC interface is 0.8 V rather than the 1.5 V specified in the IIC standard

## 9.2 CPM AC Timing Specifications

Table 34 and Table 35 provide the CPM input and output AC timing specifications, respectively.

**NOTE: Rise/Fall Time on CPM Input Pins**

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

**Table 34. CPM Input AC Timing Specifications [1]**

| Characteristic | Symbol [2] | Min [3] | Unit |
|---|---|---|---|
| FCC inputs—internal clock (NMSI) input setup time | $t_{FIIVKH}$ | 6 | ns |
| FCC inputs—internal clock (NMSI) hold time | $t_{FIIXKH}$ | 0 | ns |
| FCC inputs—external clock (NMSI) input setup time | $t_{FEIVKH}$ | 2.5 | ns |
| FCC inputs—external clock (NMSI) hold time | $t_{FEIXKH}$b | 2 | ns |
| SCC/SPI inputs—internal clock (NMSI) input setup time | $t_{NIIVKH}$ | 6 | ns |
| SCC/SPI inputs—internal clock (NMSI) input hold time | $t_{NIIXKH}$ | 0 | ns |
| SCC/SPI inputs—external clock (NMSI) input setup time | $t_{NEIVKH}$ | 4 | ns |
| SCC/SPI inputs—external clock (NMSI) input hold time | $t_{NEIXKH}$ | 2 | ns |
| TDM inputs/SI—input setup time | $t_{TDIVKH}$ | 4 | ns |
| TDM inputs/SI—hold time | $t_{TDIXKH}$ | 3 | ns |

Figure 24 shows the FCC internal clock.

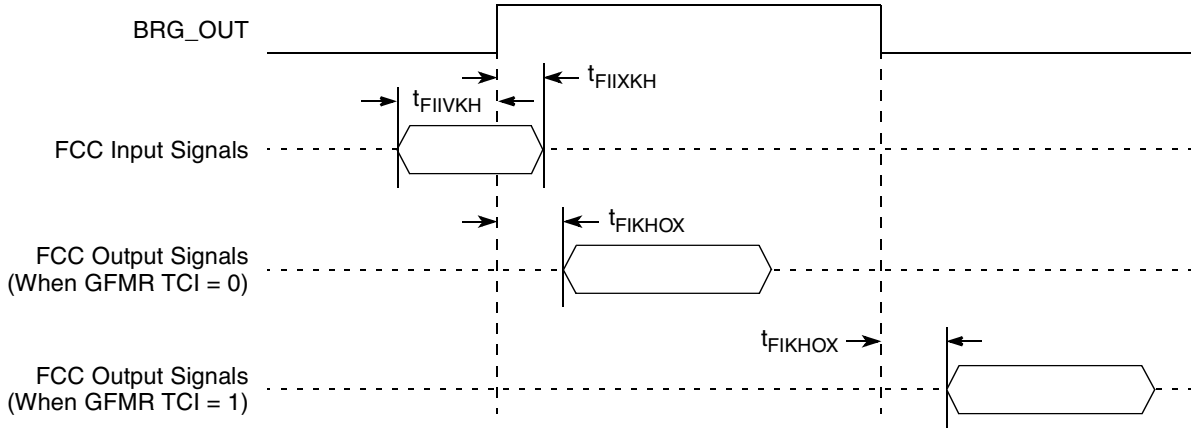



**Figure 24. FCC Internal AC Timing Clock Diagram**

Figure 25 shows the FCC external clock.

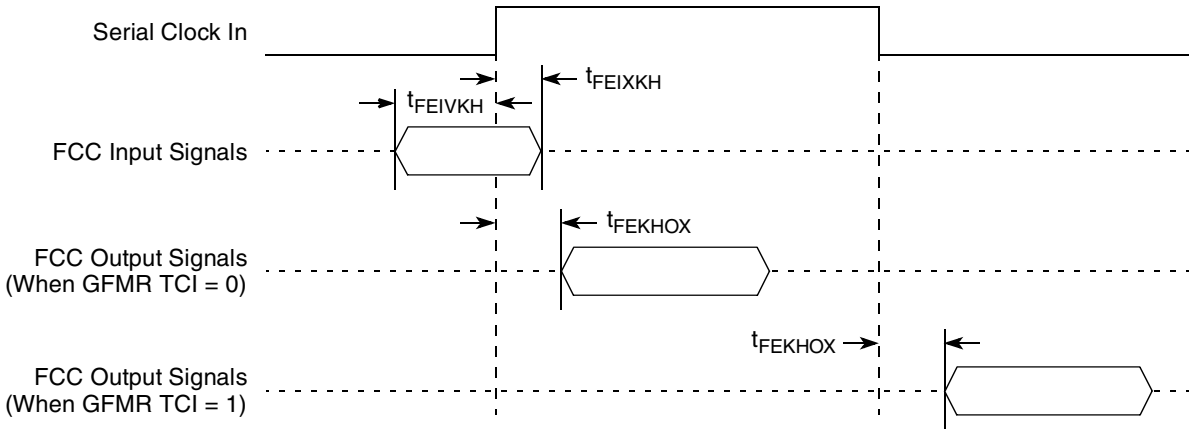



**Figure 25. FCC External AC Timing Clock Diagram**

Figure 26 shows Ethernet collision timing on FCCs.

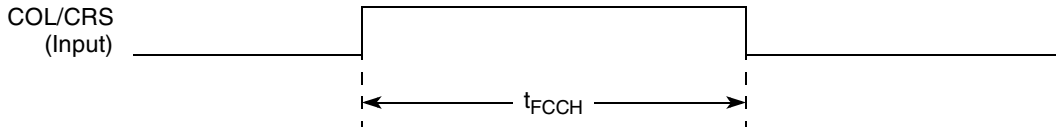
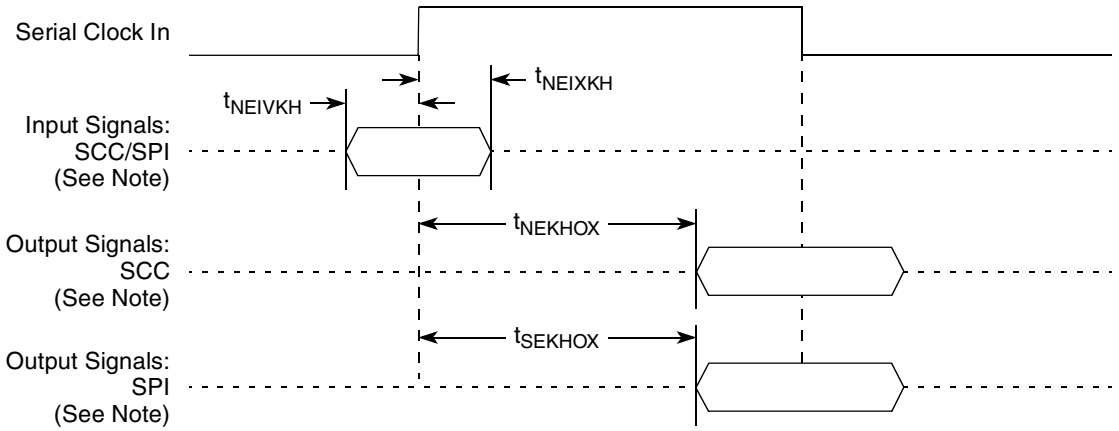



**Figure 26. Ethernet Collision AC Timing Diagram (FCC)**

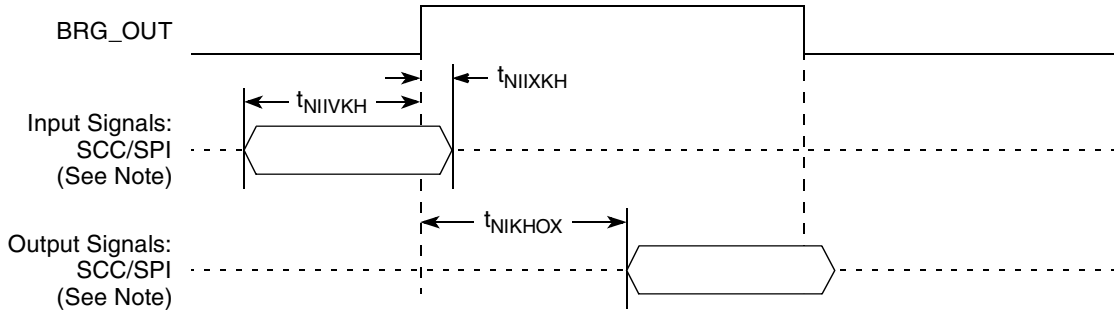
Figure 27 shows the SCC/SPI external clock.




**Note:** The clock edge is selectable on SCC and SPI.

**Figure 27. SCC/SPI AC Timing External Clock Diagram**

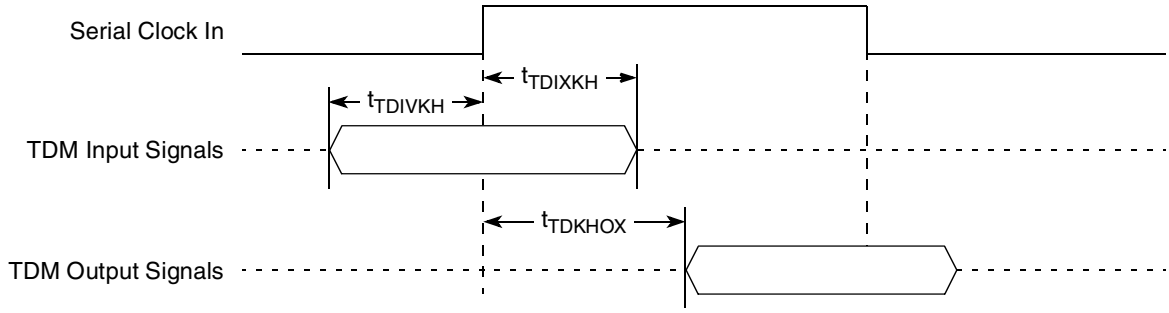
Figure 28 shows the SCC/SPI internal clock.




**Note:** The clock edge is selectable on SCC and SPI.

**Figure 28. SCC/SPI AC Timing Internal Clock Diagram**

Figure 29 shows TDM input and output signals.




**Note:** There are 4 possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 29. TDM Signal AC Timing Diagram**

# 10 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8560.

Table 39 provides the JTAG AC timing specifications as defined in Figure 32 through Figure 35.

**Table 39. JTAG AC Timing Specifications (Independent of SYSCLK) [1]**

At recommended operating conditions (see Table 2).

| Parameter | Symbol [2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | — |
| JTAG external clock pulse width measured at 1.4 V | $t_{JTKHKL}$ | 15 | — | ns | — |
| JTAG external clock rise and fall times | $t_{JTGR}$ & $t_{JTGF}$ | 0 | 2 | ns | 6 |
| $\overline{\text{TRST}}$ assert time | $t_{TRST}$ | 25 | — | ns | 3 |
| Input setup times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDVKH}$<br>$t_{JTIVKH}$ | <br>4<br>0 | <br>—<br>— | ns | 4 |
| Input hold times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDXKH}$<br>$t_{JTIXKH}$ | <br>20<br>25 | <br>—<br>— | ns | 4 |
| Valid times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDV}$<br>$t_{JTKLOV}$ | <br>4<br>4 | <br>20<br>25 | ns | 5 |
| Output hold times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDX}$<br>$t_{JTKLOX}$ | | — | ns | 5 |
| JTAG external clock to output high impedance:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDZ}$<br>$t_{JTKLOZ}$ | <br>3<br>3 | <br>19<br>9 | ns | 5, 6 |

**Notes:**

1. All outputs are measured from the midpoint voltage of the falling/rising edge of $t_{TCLK}$ to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 31). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to $t_{TCLK}$.
5. Non-JTAG signal output timing with respect to $t_{TCLK}$.
6. Guaranteed by design.

**Table 46. RapidIO 8/16 LP-LVDS Driver DC Electrical Characteristics (continued)**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 5%.

| Characteristic | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Common mode offset voltage | $\Delta V_{OSCM}$ | — | 50 | mV | 1, 6 |
| Differential termination | $R_{TERM}$ | 90 | 220 | W | — |
| Short circuit current (either output) | $\lvert I_{SS} \rvert$ | — | 24 | mA | 7 |
| Bridged short circuit current | $\lvert I_{SB} \rvert$ | — | 12 | mA | 8 |

**Notes:**

1.Bridged 100-Ω load.

2.See Figure 41(a).

3.Differential offset voltage = $\lvert V_{OHD}+V_{OLD} \rvert$. See Figure 41(b).

4.$V_{OHCM} = (V_{OA} + V_{OB})/2$ when measuring $V_{OHD}$.

5.$V_{OLCM} = (V_{OA} + V_{OB})/2$ when measuring $V_{OLD}$.

6.Common mode offset $\Delta V_{OSCM} = \lvert V_{OHCM} - V_{OLCM} \rvert$. See Figure 41(c).

7.Outputs shorted to $V_{DD}$ or GND.

8.Outputs shorted together.

**Table 47. RapidIO 8/16 LP-LVDS Receiver DC Electrical Characteristics**

| Characteristic | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Voltage at either input | $V_I$ | 0 | 2.4 | V | — |
| Differential input high voltage | $V_{IHD}$ | 100 | 600 | mV | 1 |
| Differential input low voltage | $V_{ILD}$ | –600 | –100 | mV | 1 |
| Common mode input range (referenced to receiver ground) | $V_{ICM}$ | 0.050 | 2.350 | V | 2 |
| Input differential resistance | $R_{IN}$ | 90 | 110 | W | — |

**Notes:**

1.Over the common mode range.

2.Limited by $V_I$. See Figure 48.

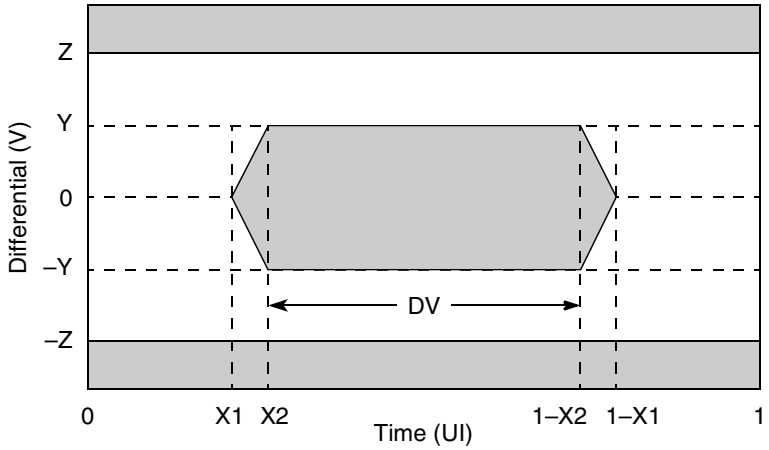



**Figure 43. Example Compliance Mask**

Y = minimum data valid amplitude

Z = maximum amplitude

1 UI = 1 unit interval = 1/baud rate

X1 = end of zero crossing region

X2 = beginning of data valid window

DV = data valid window = $1 - 2 \times X2$

The waveform of the signal under test must fall within the unshaded area of the mask to be compliant. Different masks are used for the driver output and the receiver input allowing each to be separately specified.

## 13.3.1 RapidIO Driver AC Timing Specifications

Driver AC timing specifications are provided in Table 48, Table 49, and Table 50. A driver shall comply with the specifications for each data rate/frequency for which operation of the driver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The output of a driver shall be connected to a 100 Ω, ±1%, differential (bridged) resistive load.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7]).

**Table 48. RapidIO Driver AC Timing Specifications—500 Mbps Data Rate**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Differential output high voltage | $V_{OHD}$ | 200 | 540 | mV | 1 |
| Differential output low voltage | $V_{OLD}$ | –540 | –200 | mV | 1 |

The eye pattern for a data signal is generated by making a large number of recordings of the signal and then overlaying the recordings. The number of recordings used to generate the eye shall be large enough that further increasing the number of recordings used does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not. Each data signal in the interface shall be carrying random or pseudo-random data when the recordings are made. If pseudo-random data is used, the length of the pseudo-random sequence (repeat length) shall be long enough that increasing the length of the sequence does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not comply with the mask. The data carried by any given data signal in the interface may not be correlated with the data carried by any other data signal in the interface. The zero-crossings of the clock associated with a data signal shall be used as the timing reference for aligning the multiple recordings of the data signal when the recordings are overlaid.

While the method used to make the recordings and overlay them to form the eye pattern is not specified, the method used shall be demonstrably equivalent to the following method. The signal under test is repeatedly recorded with a digital oscilloscope in infinite persistence mode. Each recording is triggered by a zero-crossing of the clock associated with the data signal under test. Roughly half of the recordings are triggered by positive-going clock zero-crossings and roughly half are triggered by negative-going clock zero-crossings. Each recording is at least 1.9 UI in length (to ensure that at least one complete eye is formed) and begins 0.5 UI before the trigger point (0.5 UI before the associated clock zero-crossing). Depending on the length of the individual recordings used to generate the eye pattern, one or more complete eyes will be formed. Regardless of the number of eyes, the eye whose center is immediately to the right of the trigger point is the eye used for compliance testing.

An example of an eye pattern generated using the above method with recordings 3 UI in length is shown in Figure 45. In this example, there is no skew between the signal under test and the associated clock used to trigger the recordings. If skew was present, the eye pattern would be shifted to the left or right relative to the oscilloscope trigger point.

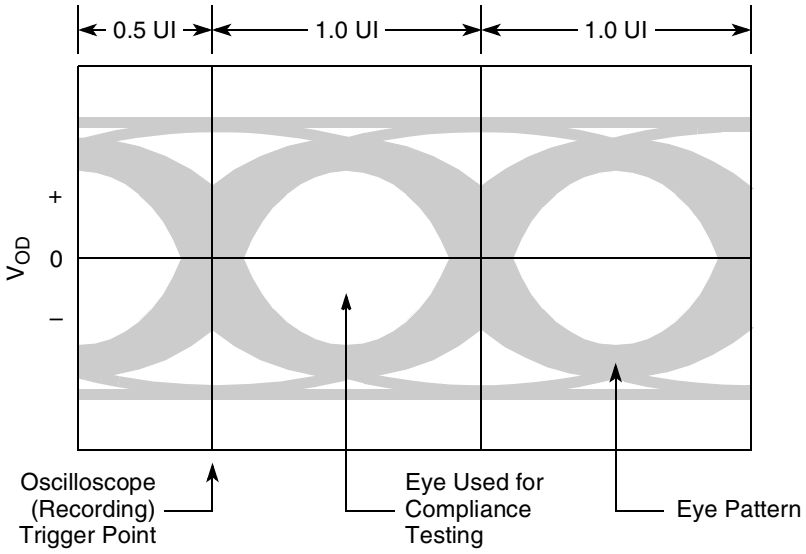



**Figure 45. Example Driver Output Eye Pattern**

# 14 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions.

## 14.1 Package Parameters for the MPC8560 FC-PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip plastic ball grid array (FC-PBGA).

| | |
|---|---|
| Die size | 12.2 mm × 9.5 mm |
| Package outline | 29 mm × 29 mm |
| Interconnects | 783 |
| Pitch | 1 mm |
| Minimum module height | 3.07 mm |
| Maximum module height | 3.75 mm |
| Solder Balls | 62 Sn/36 Pb/2 Ag |
| Ball diameter (typical) | 0.5 mm |

**Table 54. MPC8560 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| LCS6/DMA_DACK2 | P27 | O | $OV_{DD}$ | 1 |
| LCS7/DMA_DDONE2 | P28 | O | $OV_{DD}$ | 1 |
| LDP[0:3] | AA27, AA28, T26, P21 | I/O | $OV_{DD}$ | |
| LGPL0/LSDA10 | U19 | O | $OV_{DD}$ | 5, 9 |
| LGPL1/LSDWE | U22 | O | $OV_{DD}$ | 5, 9 |
| LGPL2/LOE/LSDRAS | V28 | O | $OV_{DD}$ | 8, 9 |
| LGPL3/LSDCAS | V27 | O | $OV_{DD}$ | 5, 9 |
| LGPL4/LGTA/LUPWAIT/ LPBSE | V23 | I/O | $OV_{DD}$ | 22 |
| LGPL5 | V22 | O | $OV_{DD}$ | 5, 9 |
| LSYNC_IN | T27 | I | $OV_{DD}$ | — |
| LSYNC_OUT | T28 | O | $OV_{DD}$ | — |
| LWE[0:1]/LSDDQM[0:1]/LBS[0:1] | AB28, AB27 | O | $OV_{DD}$ | 1, 5, 9 |
| LWE[2:3]/LSDDQM[2:3]/LBS[2:3] | T23, P24 | O | $OV_{DD}$ | 1, 5, 9 |
| **DMA** | | | | |
| DMA_DREQ[0:1] | H5, G4 | I | $OV_{DD}$ | — |
| DMA_DACK[0:1] | H6, G5 | O | $OV_{DD}$ | — |
| DMA_DDONE[0:1] | H7, G6 | O | $OV_{DD}$ | — |
| **Programmable Interrupt Controller** | | | | |
| MCP | AG17 | I | $OV_{DD}$ | — |
| UDE | AG16 | I | $OV_{DD}$ | — |
| IRQ[0:7] | AA18, Y18, AB18, AG24, AA21, Y19, AA19, AG25 | I | $OV_{DD}$ | — |
| IRQ8 | AB20 | I | $OV_{DD}$ | 9 |
| IRQ9/DMA_DREQ3 | Y20 | I | $OV_{DD}$ | 1 |
| IRQ10/DMA_DACK3 | AF26 | I/O | $OV_{DD}$ | 1 |
| IRQ11/DMA_DDONE3 | AH24 | I/O | $OV_{DD}$ | 1 |
| IRQ_OUT | AB21 | O | $OV_{DD}$ | 2, 4 |
| **Ethernet Management Interface** | | | | |
| EC_MDC | F1 | O | $OV_{DD}$ | 5, 9 |
| EC_MDIO | E1 | I/O | $OV_{DD}$ | — |

**Table 54. MPC8560 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **JTAG** | | | | |
| TCK | AF21 | I | $OV_{DD}$ | — |
| TDI | AG21 | I | $OV_{DD}$ | 12 |
| TDO | AF19 | O | $OV_{DD}$ | 11 |
| TMS | AF23 | I | $OV_{DD}$ | 12 |
| $\overline{\text{TRST}}$ | AG23 | I | $OV_{DD}$ | 12 |
| **DFT** | | | | |
| $\overline{\text{LSSD\_MODE}}$ | AG19 | I | $OV_{DD}$ | 21 |
| L1_TSTCLK | AB22 | I | $OV_{DD}$ | 21 |
| L2_TSTCLK | AG22 | I | $OV_{DD}$ | 21 |
| $\overline{\text{TEST\_SEL}}$ | AH20 | I | $OV_{DD}$ | 3 |
| **Thermal Management** | | | | |
| THERM0 | AG2 | I | — | 14 |
| THERM1 | AH3 | I | — | 14 |
| **Power Management** | | | | |
| ASLEEP | AG18 | I/O | | 9, 19 |
| **Power and Ground Signals** | | | | |
| $AV_{DD}1$ | AH19 | Power for e500 PLL (1.2 V) | $AV_{DD}1$ | — |
| $AV_{DD}2$ | AH18 | Power for CCB PLL (1.2 V) | $AV_{DD}2$ | — |
| $AV_{DD}3$ | AH17 | Power for CPM PLL (1.2 V) | $AV_{DD}3$ | — |
| GND | A12, A17, B3, B14, B20, B26, B27, C2, C4, C11,C17, C19, C22, C27, D8, E3, E12, E24, F11, F18, F23, G9, G12, G25, H4, H12, H14, H17, H20, H22, H27, J19, J24, K5, K9, K18, K23, K28, L6, L20, L25, M4, M12, M14, M16, M22, M27, N2, N13, N15, N17, P12, P14, P16, P23, R13, R15, R17, R20, R26, T3, T8, T10, T12, T14, T16, U6, U13, U15, U16, U17, U21, V7, V10, V26, W5, W18, W23, Y8, Y16, AA6, AA13, AB4, AB11, AB19, AC6, AC9, AD3, AD8, AD17, AF2, AF4, AF10, AF13, AF15, AF27, AG3, AG7, AG26 | — | — | — |
| $GV_{DD}$ | A14, A20, A25, A26, A27, A28, B17, B22, B28, C12, C28, D16, D19, D21, D24, D28, E17, E22, F12, F15, F19, F25, G13, G18, G20, G23, G28, H19, H24, J12, J17, J22, J27, K15, K20, K25, L13, L23, L28, M25, N21 | Power for DDR DRAM I/O Voltage (2.5 V) | $GV_{DD}$ | — |

## 15.2 Platform/System PLL Ratio

The platform clock is the clock that drives the L2 cache, the DDR SDRAM data rate, and the e500 core complex bus (CCB), and is also called the CCB clock. The values are determined by the binary value on LA[28:31] at power up, as shown in Table 57.

There is no default for this PLL ratio; these signals must be pulled to the desired values.

**Table 57. CCB Clock Ratio**

| Binary Value of LA[28:31] Signals | Ratio Description |
|---|---|
| 0000 | 16:1 ratio CCB clock: SYSCLK (PCI bus) |
| 0001 | Reserved |
| 0010 | 2:1 ratio CCB clock: SYSCLK (PCI bus) |
| 0011 | 3:1 ratio CCB clock: SYSCLK (PCI bus) |
| 0100 | 4:1 ratio CCB clock: SYSCLK (PCI bus) |
| 0101 | 5:1 ratio CCB clock: SYSCLK (PCI bus) |
| 0110 | 6:1 ratio CCB clock: SYSCLK (PCI bus) |
| 0111 | Reserved |
| 1000 | 8:1 ratio CCB clock: SYSCLK (PCI bus) |
| 1001 | 9:1 ratio CCB clock: SYSCLK (PCI bus) |
| 1010 | 10:1 ratio CCB clock: SYSCLK (PCI bus) |
| 1011 | Reserved |
| 1100 | 12:1 ratio CCB clock: SYSCLK (PCI bus) |
| 1101 | Reserved |
| 1110 | Reserved |
| 1111 | Reserved |

## 15.3 e500 Core PLL Ratio

Table 58 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LALE and LGPL2 at power up, as shown in Table 58.

**Table 58. e500 Core to CCB Ratio**

| Binary Value of LALE, LGPL2 Signals | Ratio Description |
|---|---|
| 00 | 2:1 e500 core:CCB |
| 01 | 5:2 e500 core:CCB |
| 10 | 3:1 e500 core:CCB |
| 11 | 7:2 e500 core:CCB |

| | |
|---|---|
| Alpha Novatech<br>473 Sapena Ct. #15<br>Santa Clara, CA 95054<br>Internet: www.alphanovatech.com | 408-749-7601 |
| International Electronic Research Corporation (IERC)<br>413 North Moss St.<br>Burbank, CA 91502<br>Internet: www.ctscorp.com | 818-842-7277 |
| Millennium Electronics (MEI)<br>Loroco Sites<br>671 East Brokaw Road<br>San Jose, CA 95112<br>Internet: www.mei-millennium.com | 408-436-8770 |
| Tyco Electronics<br>Chip Coolers™<br>P.O. Box 3668<br>Harrisburg, PA 17105-3668<br>Internet: www.chipcoolers.com | 800-522-6752 |
| Wakefield Engineering<br>33 Bridge St.<br>Pelham, NH 03076<br>Internet: www.wakefield.com | 603-635-5102 |

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the MPC8560 to function in various environments.

### 16.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8560 thermal model is shown in Figure 52. Five cuboids are used to represent this device. To simplify the model, the solder balls and substrate are modeled as a single block 29x29x1.47 mm with the conductivity adjusted accordingly. For modeling, the planar dimensions of the die are rounded to the nearest mm, so the die is modeled as 10x12 mm at a thickness of 0.76 mm. The bump/underfill layer is modeled as a collapsed resistance between the die and substrate assuming a conductivity of 0.6 in-plane and 1.9 W/m•K in the thickness dimension of 0.76 mm. The lid attach adhesive is also modeled as a collapsed resistance with dimensions of 10x12x0.050 mm and the conductivity of 1 W/m•K. The nickel plated copper lid is modeled as 12x14x1 mm. Note that the die and lid are not centered on the substrate; there is a 1.5 mm offset documented in the case outline drawing in Figure 50.

Figure 58 shows the PLL power supply filter circuit.

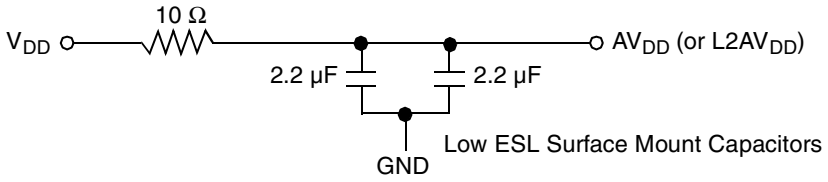



**Figure 58. PLL Power Supply Filter Circuit**

## 17.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8560 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8560 system, and the MPC8560 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each $V_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$ pins of the MPC8560. These decoupling capacitors should receive their power from separate $V_{DD}$, $OV_{DD}$, $GV_{DD}$, $LV_{DD}$, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the $V_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$ planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

## 17.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to $OV_{DD}$, $GV_{DD}$, or $LV_{DD}$ as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external $V_{DD}$, $GV_{DD}$, $LV_{DD}$, $OV_{DD}$, and GND pins of the MPC8560.

## 17.5 Output Buffer DC Impedance

The MPC8560 drivers are characterized over process, voltage, and temperature. There are two driver types: a push-pull single-ended driver (open drain for $I^2C$) for all buses except RapidIO, and a current-steering differential driver for the RapidIO port.

To measure $Z_0$ for the single-ended drivers, an external resistor is connected from the chip pad to $OV_{DD}$ or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 59). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices.

## 17.8 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 60 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 60, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

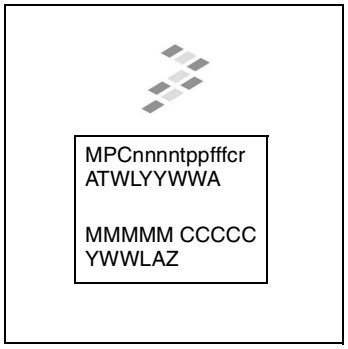
There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 60 is common to all known emulators.

**Table 62. Document Revision History (continued)**

| Rev. No. | Substantive Change(s) |
|---|---|
| 1.2 | Section 1.1.1—Updated feature list.<br>Section 1.2.1.1—Updated notes for Table 1.<br>Section 1.2.1.2—Removed 5-V PCI interface overshoot and undershoot figure.<br>Section 1.2.1.3—Added this section to summarize impedance driver settings for various interfaces.<br>Section 1.4—Updated rows in Reset Initialization timing specifications table. Added a table with DLL and PLL timing specifications.<br>Section 1.5.2.2—Updated note 6 of DDR SDRAM Output AC Timing Specifications table.<br>Section 1.7—Changed the minimum input low current from -600 to -15 μA for the RGMII DC electrical characteristics.<br>Section 1.7.2—Changed LCS[3:4] to TSEC1_TXD[6:5]. Updated notes regarding LCS[3:4].<br>Section 1.13.2—Updated the mechanical dimensions diagram for the package.<br>Section 1.13.3—Updated the notes for LBCTL, TRIG_OUT, and ASLEEP. Corrected pin assignments for IIC_SDA and IIC_SCL. Corrected reserved pin assignment of V11 to U11. V11 is actually $\overline{\text{PCI\_STOP}}$.<br>Section 1.14.1—Updated the table for frequency options with respect to platform/CCB frequencies.<br>Section 1.14.4—Edited Frequency options with respect to memory bus speeds. |
| 1.1 | Made updates throughout document.<br>Section 1.6.1—Added symbols and note for the GTX_CLK125 timing parameters.<br>Section 1.11.3—Updated pin list table: LGPL5/LSDAMUX to LGPL5, LA[27:29] and LA[30:31] to LA[27:31], TRST to $\overline{\text{TRST}}$, added GBE Clocking section and EC_GTX_CLK125 signal.<br>Figure 50—Updated pin 2 connection information. |
| 1 | Original Customer Version. |

## 19.2 Part Marking

Parts are marked as the example shown in Figure 62.




FC-PBGA

**Notes:**

MMMMM is the 5-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.
YWWLAZ is the assembly traceability code.

**Figure 62. Part Marking for FC-PBGA Device**