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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8560pxaqfb

- Interrupts can be routed to the e500 core's standard or critical interrupt inputs
- Interrupt summary registers allow fast identification of interrupt source
- I²C controller
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I²C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I²C addressing mode
 - Data integrity checked with preamble signature and CRC
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data operating at up to 166 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
 - Three protocol engines available on a per chip select basis:
 - General purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)
 - Dedicated single data rate SDRAM controller
 - Parity support
 - Default boot ROM chip select with configurable bus width (8-,16-, or 32-bit)
- Two three-speed (10/100/1Gb) Ethernet controllers (TSECs)
 - Dual IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab compliant controllers
 - Support for different Ethernet physical interfaces:
 - 10/100/1Gb Mbps IEEE 802.3 GMII
 - 10/100 Mbps IEEE 802.3 MII
 - 10 Mbps IEEE 802.3 MII
 - 1000 Mbps IEEE 802.3z TBI
 - 10/100/1Gb Mbps RGMII/RTBI
 - Full- and half-duplex support
 - Buffer descriptors are backward compatible with MPC8260 and MPC860T 10/100 programming models
 - 9.6-Kbyte jumbo frame support
 - RMON statistics support
 - 2-Kbyte internal transmit and receive FIFOs

- System performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter-specific events
 - Supports 64 reference events that can be counted on any of the 8 counters
 - Supports duration and quantity threshold counting
 - Burstiness feature that permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- System access port
 - Uses JTAG interface and a TAP controller to access entire system memory map
 - Supports 32-bit accesses to configuration registers
 - Supports cache-line burst accesses to main memory
 - Supports large block (4-Kbyte) uploads and downloads
 - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1™-compliant, JTAG boundary scan
- 783 FC-PBGA package

2 Electrical Characteristics

This section provides the electrical specifications and thermal characteristics for the MPC8560. The MPC8560 is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings ¹

Characteristic	Symbol	Max Value	Unit	Notes
Core supply voltage For devices rated at 667 and 833 MHz For devices rated at 1 GHz	V _{DD}	–0.3 to 1.32 –0.3 to 1.43	V	—
PLL supply voltage For devices rated at 667 and 833 MHz For devices rated at 1 GHz	AV _{DD}	–0.3 to 1.32 –0.3 to 1.43	V	—

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8560.

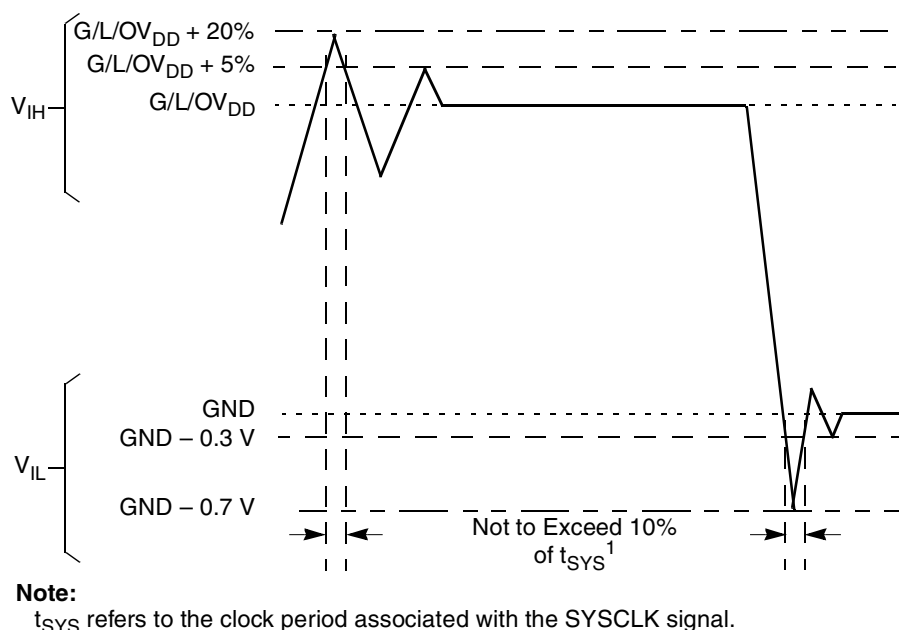


Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

The MPC8560 core voltage must always be provided at nominal 1.2 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8560 for the 3.3-V signals, respectively.

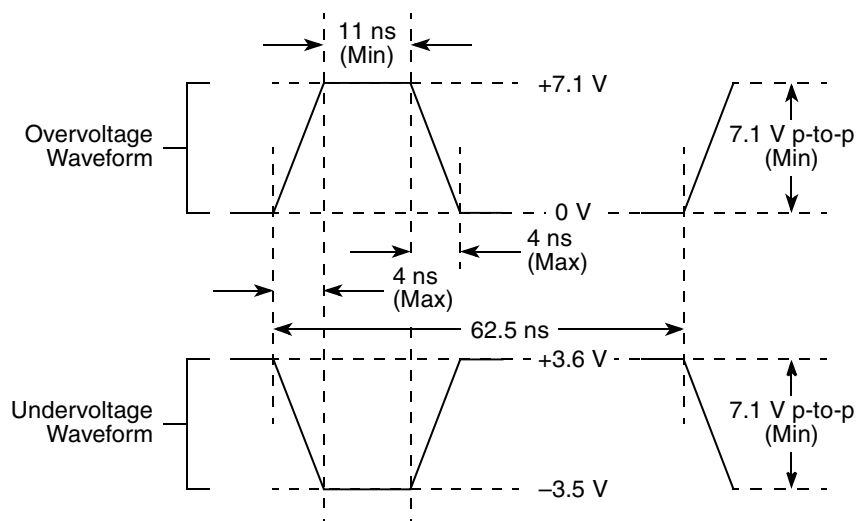


Figure 3. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

2.1.4 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25	$OV_{DD} = 3.3\text{ V}$	1
	42 (default)		
PCI signals	25		2
	42 (default)		
DDR signal	20	$GV_{DD} = 2.5\text{ V}$	—
CPM PA, PB, PC, and PD signals	42	$OV_{DD} = 3.3\text{ V}$	—
TSEC/10/100 signals	42	$LV_{DD} = 2.5/3.3\text{ V}$	—
DUART, system control, I2C, JTAG	42	$OV_{DD} = 3.3\text{ V}$	—
RapidIO N/A (LVDS signaling)	N/A		—

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSR.
2. The drive strength of the PCI interface is determined by the setting of the $\overline{PCI_GNT1}$ signal at reset.

4.4 Real Time Clock Timing

Table 10 provides the real time clock (RTC) AC timing specifications for the MPC8560.

Table 10. RTC AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
RTC clock high time	t_{RTCH}	2 x t_{CCB_CLK}	—	—	ns	—
RTC clock low time	t_{RTCL}	2 x t_{CCB_CLK}	—	—	ns	—

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8560. Table 7 provides the RESET initialization AC timing specifications for the MPC8560.

Table 11. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of \overline{HRESET}	100	—	μs	—
Minimum assertion time for \overline{SRESET}	512	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before \overline{HRESET} negation	100	—	μs	—
Input setup time for POR configs (other than PLL config) with respect to negation of \overline{HRESET}	4	—	SYSCLKs	1
Input hold time for POR configs (including PLL config) with respect to negation of \overline{HRESET}	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of \overline{HRESET}	—	5	SYSCLKs	1

Notes:

1. SYSCLK is identical to the PCI_CLK signal and is the primary clock input for the MPC8560. See the MPC8560 PowerQUICC III™ Integrated Communications Processor Preliminary Reference Manual for more details.

Table 12 provides the PLL and DLL lock times.

Table 12. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	—
DLL lock times	7680	122,880	CCB Clocks	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the platform (or CCB) clock. A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The CCB clock is determined by the $SYSCLK \times \text{platform PLL ratio}$.

Table 16. DDR SDRAM Output AC Timing Specifications–DLL Mode (continued)

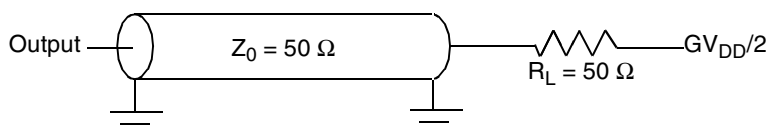
At recommended operating conditions with GV_{DD} of 2.5 V \pm 5%.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDSHME}	1.5	4.0	ns	7, 8

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (OX or DX). For example, $t_{DDKH OV}$ symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (O) are valid (V) or output valid time. Also, $t_{DDKL DX}$ symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/\overline{MCK} referenced measurements are made from the crossing of the two signals ± 0.1 V.
- Maximum possible clock skew between a clock $MCK[n]$ and its relative inverse clock $\overline{MCK}[n]$, or between a clock $MCK[n]$ and a relative clock $MCK[m]$ or $MSYNC_OUT$. Skew measured between complementary signals at $GV_{DD}/2$.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/\overline{MCK} and $MDQ/MECC/MDM/MDQS$.
- Note that t_{DDSHMH} follows the symbol conventions described in note 1. For example, t_{DDSHMH} describes the DDR timing (DD) from the rising edge of the $MSYNC_IN$ clock (SH) until the MDQS signal is valid (MH). t_{DDSHMH} can be modified through control of the DQSS override bits in the $TIMING_CFG_2$ register. These controls allow the relationship between the synchronous clock control timing and the source-synchronous DQS domain to be modified by the user. For best turnaround times, these may need to be set to delay t_{DDSHMH} an additional $0.25t_{MCK}$. This will also affect t_{DDSHMP} and t_{DDSHME} accordingly. See the *MPC8560 PowerQUICC III Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8560.
- All outputs are referenced to the rising edge of $MSYNC_IN$ (S) at the pins of the MPC8560. Note that t_{DDSHMP} follows the symbol conventions described in note 1. For example, t_{DDSHMP} describes the DDR timing (DD) from the rising edge of the $MSYNC_IN$ clock (SH) for the duration of the MDQS signal precharge period (MP).
- Guaranteed by design.
- Guaranteed by characterization.

Figure 5 provides the AC test load for the DDR bus.

**Figure 5. DDR AC Test Load****Table 17. DDR SDRAM Measurement Conditions**

Symbol	DDR	Unit	Notes
V_{TH}	$MV_{REF} \pm 0.31$ V	V	1
V_{OUT}	$0.5 \times GV_{DD}$	V	2

Notes:

- Data input threshold measurement point.
- Data output measurement point.

Figure 6 shows the DDR SDRAM output timing diagram.

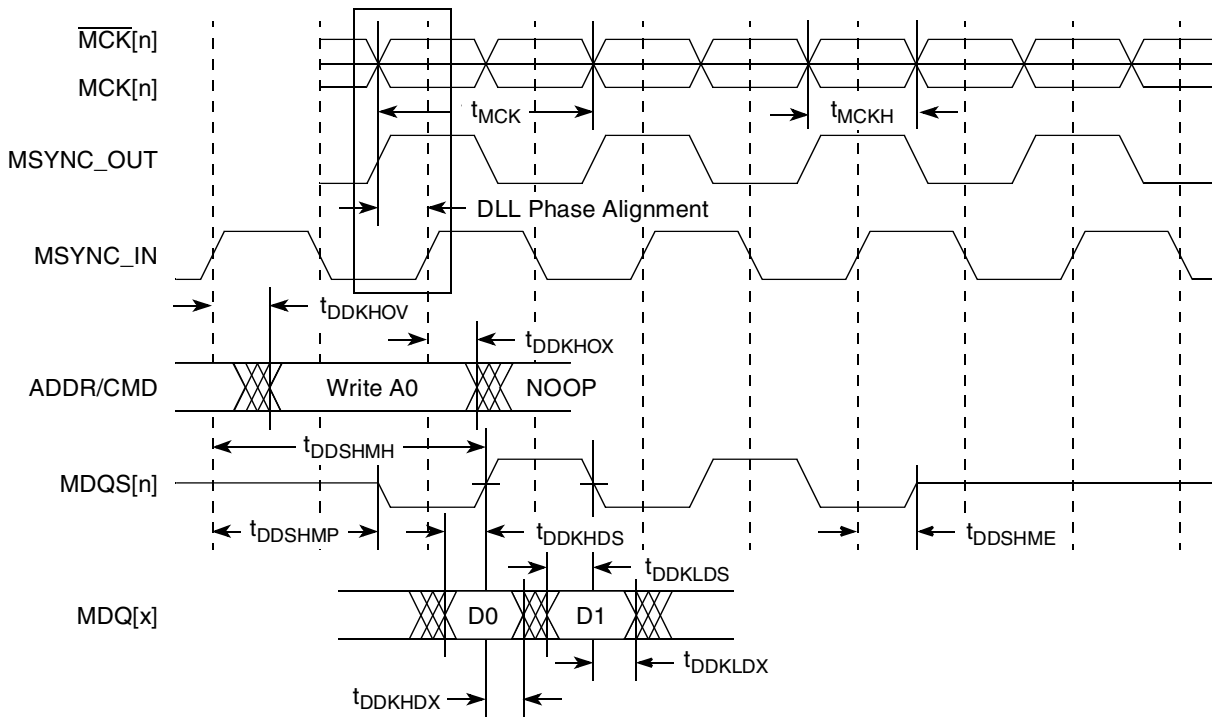


Figure 6. DDR SDRAM Output Timing Diagram

6.2.2.2 Load Effects on Address/Command Bus

Table 18 provides approximate delay information that can be expected for the address and command signals of the DDR controller for various loadings. These numbers are the result of simulations for one topology. The delay numbers will strongly depend on the topology used. These delay numbers show the total delay for the address and command to arrive at the DRAM devices. The actual delay could be different than the delays seen in simulation, depending on the system topology. If a heavily loaded system is used, the DLL loop may need to be adjusted to meet setup requirements at the DRAM.

Table 18. Expected Delays for Address/Command

Load	Delay	Unit
4 devices (12 pF)	3.0	ns
9 devices (27 pF)	3.6	ns
36 devices (108 pF) + 40 pF compensation capacitor	5.0	ns
36 devices (108 pF) + 80 pF compensation capacitor	5.2	ns

Table 22. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of $3.3\text{ V} \pm 5\%$, or $LV_{DD}=2.5\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock rise and fall time	t_{GRXR} , t_{GRXF} ^{2,3}	—	—	1.0	ns

Note:

- The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$ (reference)(state) for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Signal timings are measured at 0.7 V and 1.9 V voltage levels.
- Guaranteed by design.

Figure 8 provides the AC test load for TSEC.

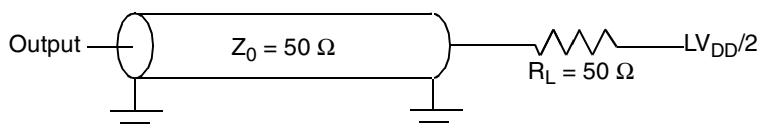
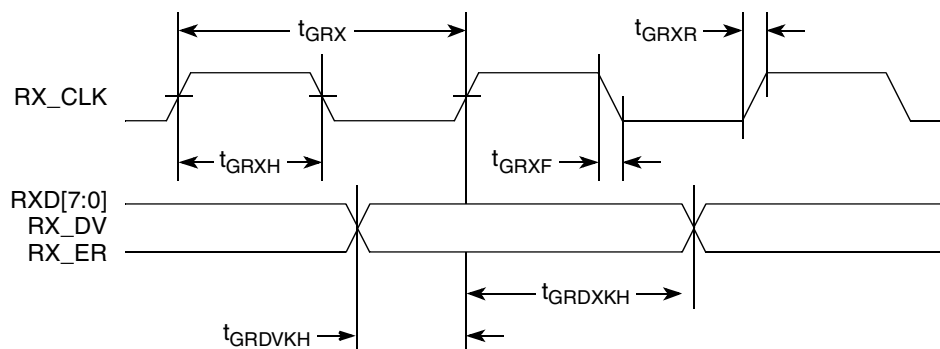
**Figure 8. TSEC AC Test Load**

Figure 9 shows the GMII receive AC timing diagram.

**Figure 9. GMII Receive AC Timing Diagram**

7.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

7.2.2.1 MII Transmit AC Timing Specifications

Table 23 provides the MII transmit AC timing specifications.

Table 23. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of $3.3\text{ V} \pm 5\%$, or $LV_{DD}=2.5\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}^2	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise and fall time	t_{MTXR} , $t_{MTXF}^{2,3}$	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$ (reference)(state) for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Signal timings are measured at 0.7 V and 1.9 V voltage levels.
- Guaranteed by design.

Figure 10 shows the MII transmit AC timing diagram.

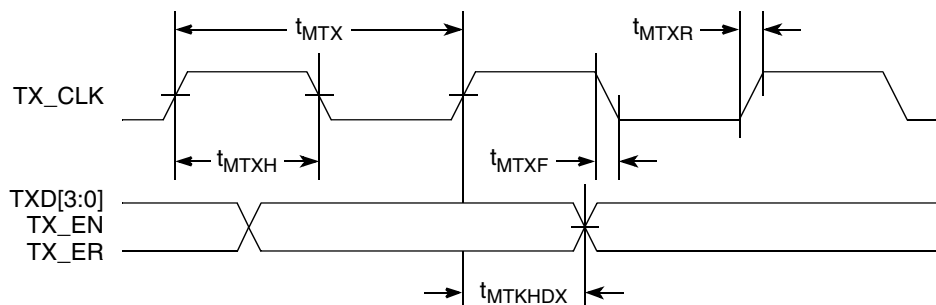


Figure 10. MII Transmit AC Timing Diagram

7.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

7.2.3.1 TBI Transmit AC Timing Specifications

Table 25 provides the TBI transmit AC timing specifications.

Table 25. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of $3.3\text{ V} \pm 5\%$, or $LV_{DD}=2.5\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t_{TTKHDX}	1.0	—	—	ns
GTX_CLK clock rise and fall time	t_{TTXR} , t_{TTXF} ^{2,3}	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)}}^{\text{(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.

3. Guaranteed by design.

Figure 12 shows the TBI transmit AC timing diagram.

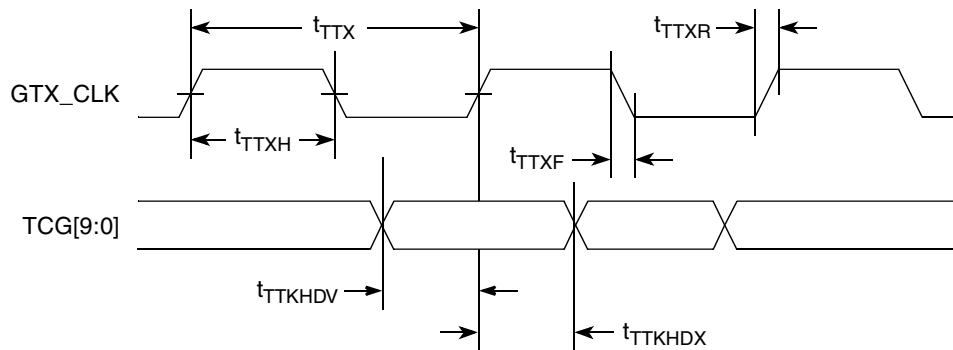


Figure 12. TBI Transmit AC Timing Diagram

Figure 14 shows the RGMII and RTBI AC timing and multiplexing diagrams.

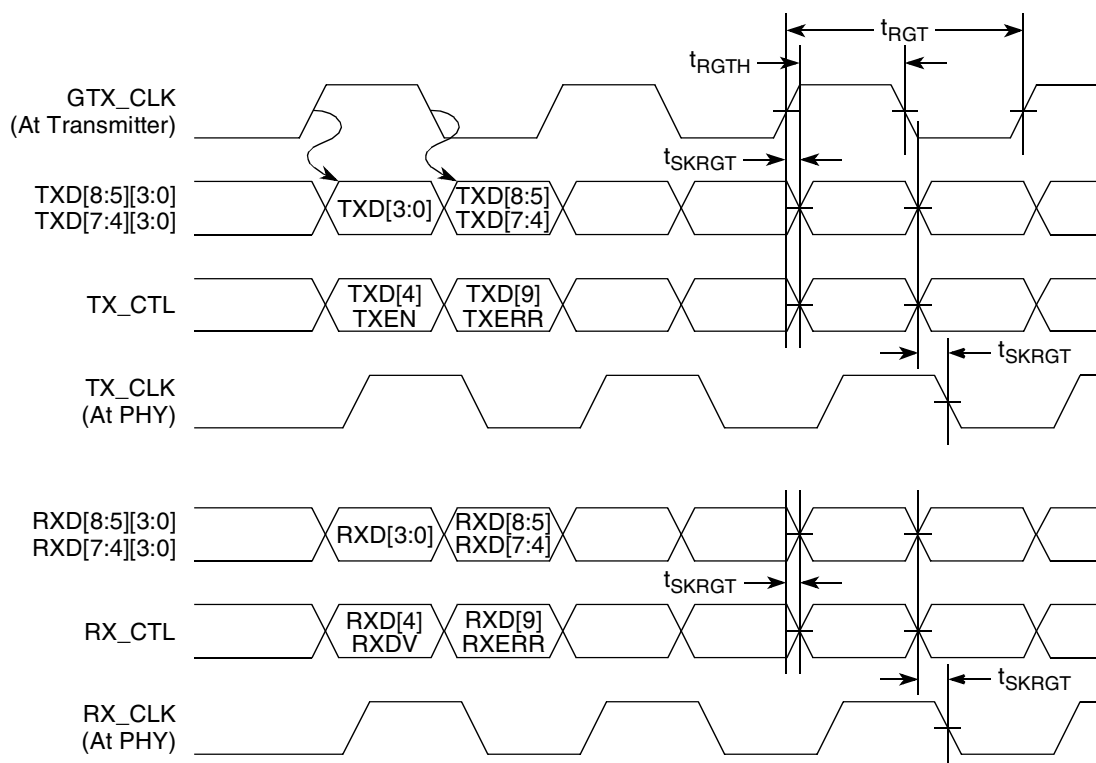


Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

7.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in [Section 7.1, “Three-Speed Ethernet Controller \(TSEC\) \(10/100/1Gb Mbps\)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics.”](#)

7.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in [Table 28](#).

Table 28. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.13	3.47	V
Output high voltage ($OV_{DD} = \text{Min}$, $I_{OH} = -1.0 \text{ mA}$)	V_{OH}	2.10	$OV_{DD} + 0.3$	V
Output low voltage ($OV_{DD} = \text{Min}$, $I_{OL} = 1.0 \text{ mA}$)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	1.70	—	V
Input low voltage	V_{IL}	—	0.90	V

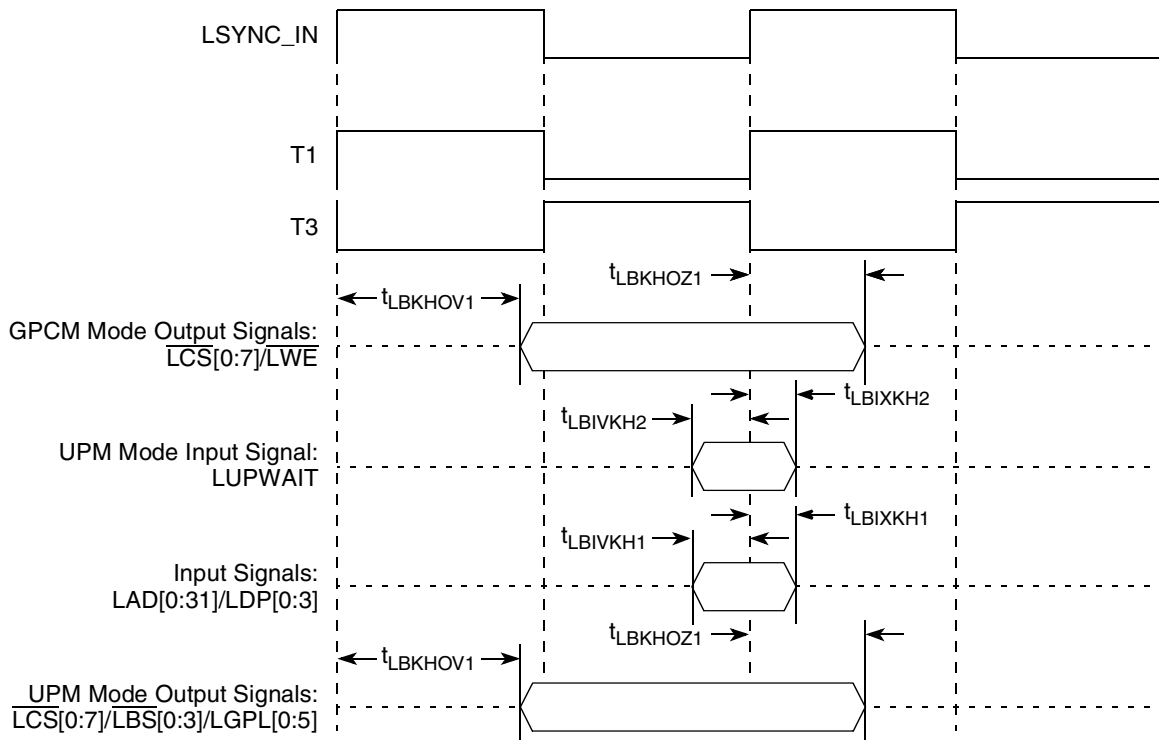


Figure 19. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

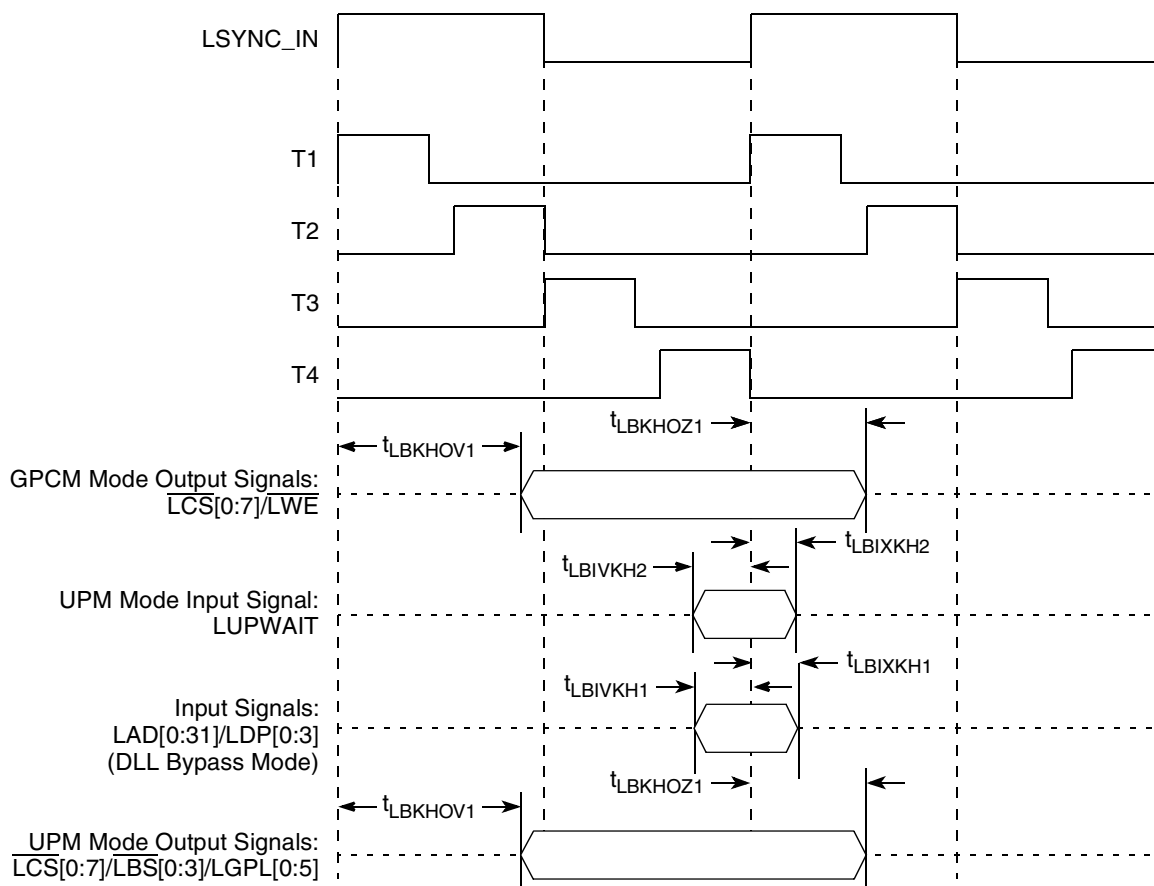


Figure 21. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Enabled)

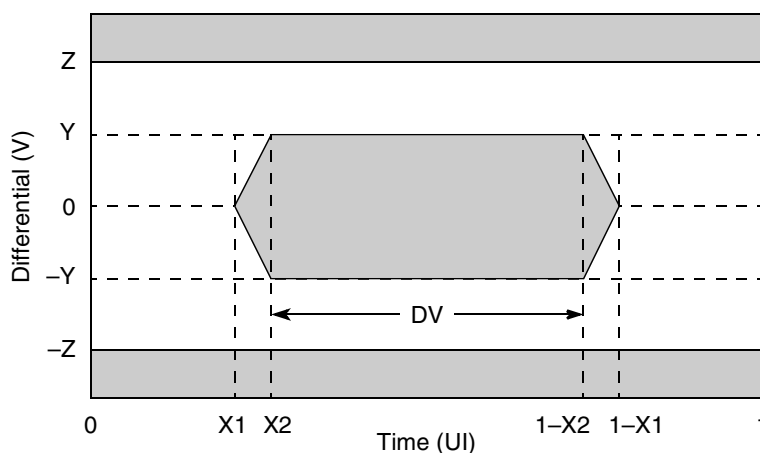


Figure 43. Example Compliance Mask

Y = minimum data valid amplitude

Z = maximum amplitude

1 UI = 1 unit interval = 1/baud rate

X1 = end of zero crossing region

X2 = beginning of data valid window

DV = data valid window = $1 - 2 \times X2$

The waveform of the signal under test must fall within the unshaded area of the mask to be compliant. Different masks are used for the driver output and the receiver input allowing each to be separately specified.

13.3.1 RapidIO Driver AC Timing Specifications

Driver AC timing specifications are provided in [Table 48](#), [Table 49](#), and [Table 50](#). A driver shall comply with the specifications for each data rate/frequency for which operation of the driver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The output of a driver shall be connected to a $100\ \Omega$, $\pm 1\%$, differential (bridged) resistive load.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7]).

Table 48. RapidIO Driver AC Timing Specifications—500 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential output high voltage	V_{OHD}	200	540	mV	1
Differential output low voltage	V_{OLD}	-540	-200	mV	1

Figure 48 shows the definitions of the data to clock static skew parameter $t_{\text{SKEW,PAIR}}$ and the data valid window parameter DV. The data and frame bits are those that are associated with the clock. The figure applies for all zero-crossings of the clock. All of the signals are differential signals. V_D represents V_{OD} for the transmitter and V_{ID} for the receiver. The center of the eye is defined as the midpoint of the region in which the magnitude of the signal voltage is greater than or equal to the minimum DV voltage.

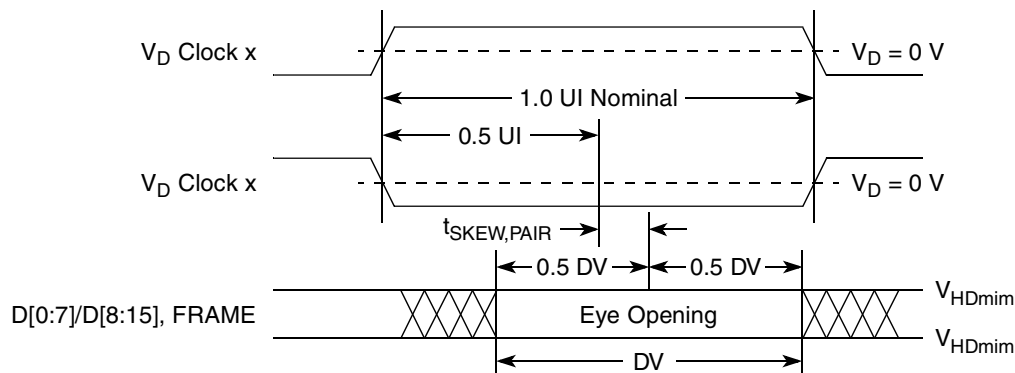


Figure 48. Data to Clock Skew

Figure 49 shows the definition of the data to data static skew parameter t_{DPAIR} and how the skew parameters are applied.

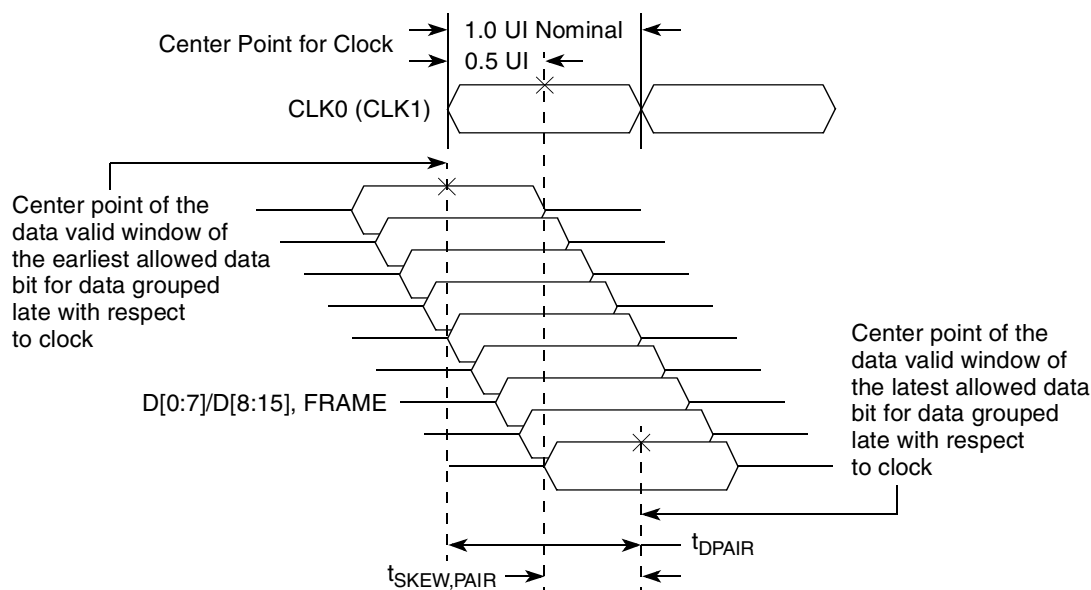


Figure 49. Static Skew Diagram

Table 54. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Gigabit Reference Clock				
EC_GTX_CLK125	E2	I	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_TXD[7:4]	A6, F7, D7, C7	O	LV _{DD}	5, 9
TSEC1_TXD[3:0]	B7, A7, G8, E8	O	LV _{DD}	9, 19
TSEC1_TX_EN	C8	O	LV _{DD}	11
TSEC1_TX_ER	B8	O	LV _{DD}	—
TSEC1_TX_CLK	C6	I	LV _{DD}	—
TSEC1_GTX_CLK	B6	O	LV _{DD}	18
TSEC1_CRS	C3	I	LV _{DD}	—
TSEC1_COL	G7	I	LV _{DD}	—
TSEC1_RXD[7:0]	D4, B4, D3, D5, B5, A5, F6, E6	I	LV _{DD}	—
TSEC1_RX_DV	D2	I	LV _{DD}	—
TSEC1_RX_ER	E5	I	LV _{DD}	—
TSEC1_RX_CLK	D6	I	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_TXD[7:2]	B10, A10, J10, K11, J11, H11	O	LV _{DD}	5, 9
TSEC2_TXD[1:0]	G11, E11	O	LV _{DD}	—
TSEC2_TX_EN	B11	O	LV _{DD}	11
TSEC2_TX_ER	D11	O	LV _{DD}	—
TSEC2_TX_CLK	D10	I	LV _{DD}	—
TSEC2_GTX_CLK	C10	O	LV _{DD}	18
TSEC2_CRS	D9	I	LV _{DD}	—
TSEC2_COL	F8	I	LV _{DD}	—
TSEC2_RXD[7:0]	F9, E9, C9, B9, A9, H9, G10, F10	I	LV _{DD}	—
TSEC2_RX_DV	H8	I	LV _{DD}	—
TSEC2_RX_ER	A8	I	LV _{DD}	—
TSEC2_RX_CLK	E10	I	LV _{DD}	—
RapidIO Interface				
RIO_RCLK	Y25	I	OV _{DD}	—
$\overline{\text{RIO_RCLK}}$	Y24	I	OV _{DD}	—

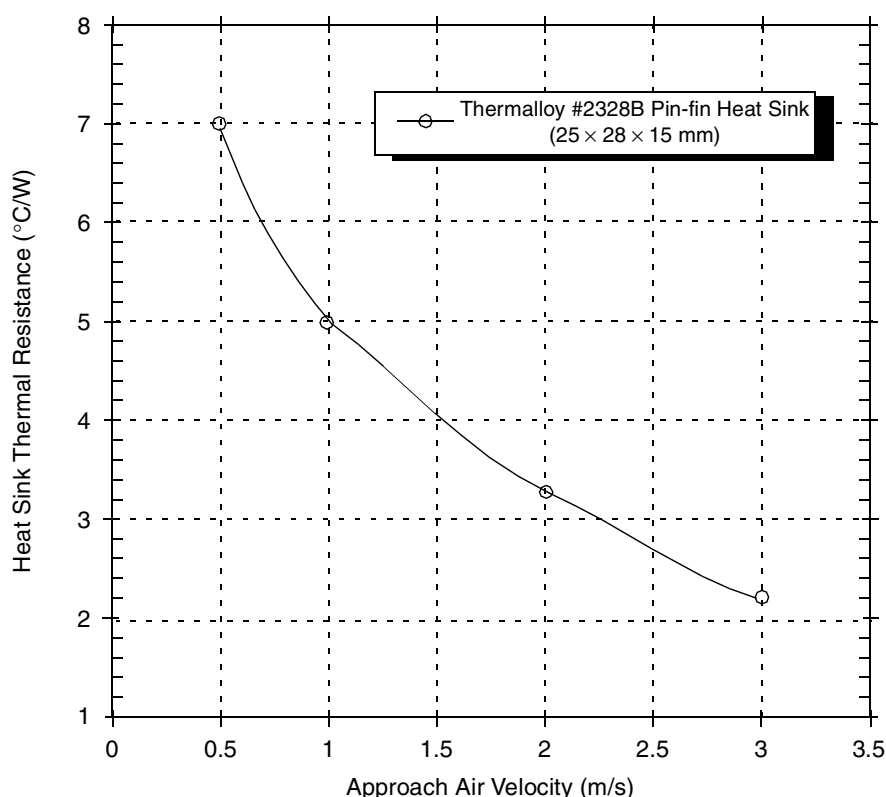


Figure 55. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

16.2.4.2 Case 2

Every system application has different conditions that the thermal management solution must solve. As an alternate example, assume that the air reaching the component is 85 °C with an approach velocity of 1 m/sec. For a maximum junction temperature of 105 °C at 7 W, the total thermal resistance of junction to case thermal resistance plus thermal interface material plus heat sink thermal resistance must be less than 2.8 °C/W. The value of the junction to case thermal resistance in [Table 60](#) includes the thermal interface resistance of a thin layer of thermal grease as documented in footnote 4 of the table. Assuming that the heat sink is flat enough to allow a thin layer of grease or phase change material, then the heat sink must be less than 2 °C/W.

Millennium Electronics (MEI) has tooled a heat sink M THERM-1051 for this requirement assuming a compact PCI environment at 1 m/sec and a heat sink height of 12 mm. The MEI solution is illustrated in [Figure 56](#) and [Figure 57](#). This design has several significant advantages:

- The heat sink is clipped to a plastic frame attached to the application board with screws or plastic inserts at the corners away from the primary signal routing areas.
- The heat sink clip is designed to apply the force holding the heat sink in place directly above the die at a maximum force of less than 10 lbs.
- For applications with significant vibration requirements, silicone damping material can be applied between the heat sink and plastic frame.

17.6 Configuration Pin Muxing

The MPC8560 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 k Ω . This value should permit the 4.7-k Ω resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform/system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

17.7 Pull-Up Resistor Requirements

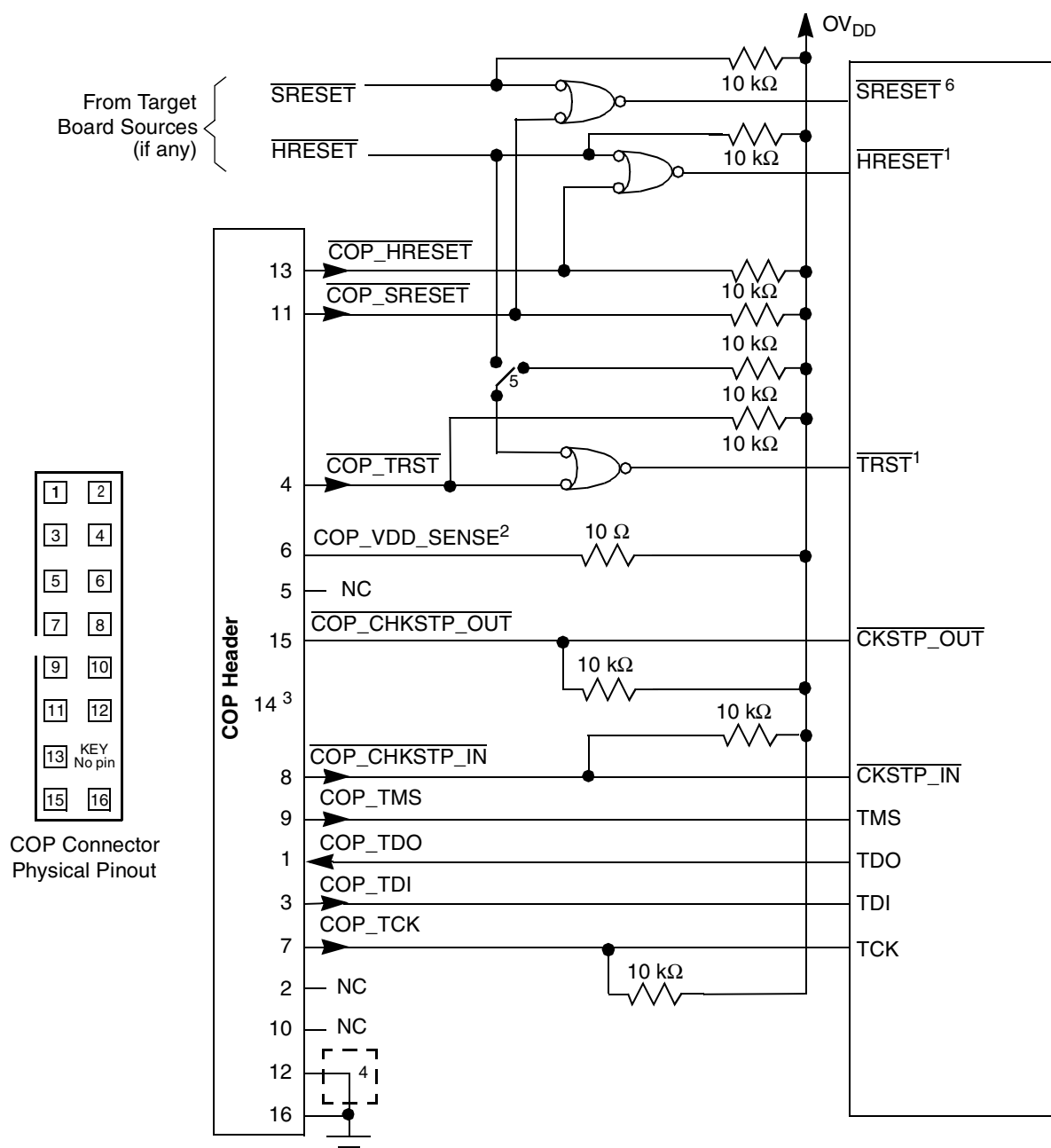
The MPC8560 requires high resistance pull-up resistors (10 k Ω is recommended) on open drain type pins including EPIC interrupt pins. I²C open drain type pins should be pulled up with ~1 k Ω resistors.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in [Figure 61](#). Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

TSEC1_TXD[3:0] must not be pulled low during reset. Some PHY chips have internal pulldowns that could cause this to happen. If such PHY chips are used, then a pullup must be placed on these signals strong enough to restore these signals to a logical 1 during reset.

Three test pins also require pull-up resistors (100 Ω - 1 k Ω). These pins are L1_TSTCLK, L2_TSTCLK, and $\overline{\text{LSSD_MODE}}$. These signals are for factory use only and must be pulled up to OVDD for normal machine operation.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

**Notes:**

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 61. JTAG Interface Connection

Table 62. Document Revision History (continued)

Rev. No.	Substantive Change(s)
2.0	<p>Section 1.1—Updated features list to coincide with latest version of the reference manual</p> <p>Table 1 and Table 2— Addition of CPM to OV_{DD} and OV_{IN}; Addition of SYSCLK to OV_{IN}</p> <p>Table 2—Addition of notes 1 and 2</p> <p>Table 3—Addition of note 1</p> <p>Table 5—New</p> <p>Section 4—New</p> <p>Table 13—Addition of I_{VREF}</p> <p>Table 15—Modified maximum values for t_{DISKEW}</p> <p>Table 16—Added MSYNC_OUT to t_{MCKSKEW2}</p> <p>Figure 5—New</p> <p>Section 6.2.1—Removed Figure 4, "DDR SDRAM Input Timing Diagram"</p> <p>Section 7.1—Removed references to 2.5 V from first paragraph</p> <p>Figure 8—New</p> <p>Table 19 and Table 20—Modified "conditions" for I_{IH} and I_{IL}</p> <p>Table 21—Addition of min and max for GTX_CLK125 reference clock duty cycle</p> <p>Table 25—Addition of min and max for GTX_CLK125 reference clock duty cycle</p> <p>Table 27—Addition of min and max for GTX_CLK125 reference clock duty cycle</p> <p>Figure 17 and Figure 19—Changed LSYNC_IN to Internal clock at top of each figure</p> <p>Table 34—Modified values for t_{FIIVKH}, t_{NIIVKH}, and t_{TDIVKH}; addition of t_{PIIVKH} and t_{PIIXKH}.</p> <p>Table 35—Modified values for t_{FEKHOX}, t_{NIKHOX}, t_{NEKHOX}, t_{TDKHOX}; addition of t_{PIKHOX}.</p> <p>Figure 16—New</p> <p>Figure 30—New</p> <p>Figure 16—New</p> <p>Figure 16—New</p> <p>Table 31—Removed row for t_{LBKHOX3}</p> <p>Table 44—New (AC timing of PCI-X at 66 MHz)</p> <p>Table 54—Addition of note 19</p> <p>Figure 61—Addition of jumper and note at top of diagram</p> <p>Table 56—Changed max bus freq for 667 core to 166</p> <p>Section 16.2.1—Modified first paragraph</p> <p>Figure 52—Modified</p> <p>Figure 53—New</p> <p>Table 60—Modified thermal resistance data</p> <p>Section 16.2.4.2—Modified first and second paragraphs</p>