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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8560vt667lb

1 Overview

The following section provides a high-level overview of the MPC8560 features. Figure 1 shows the major functional units within the MPC8560.

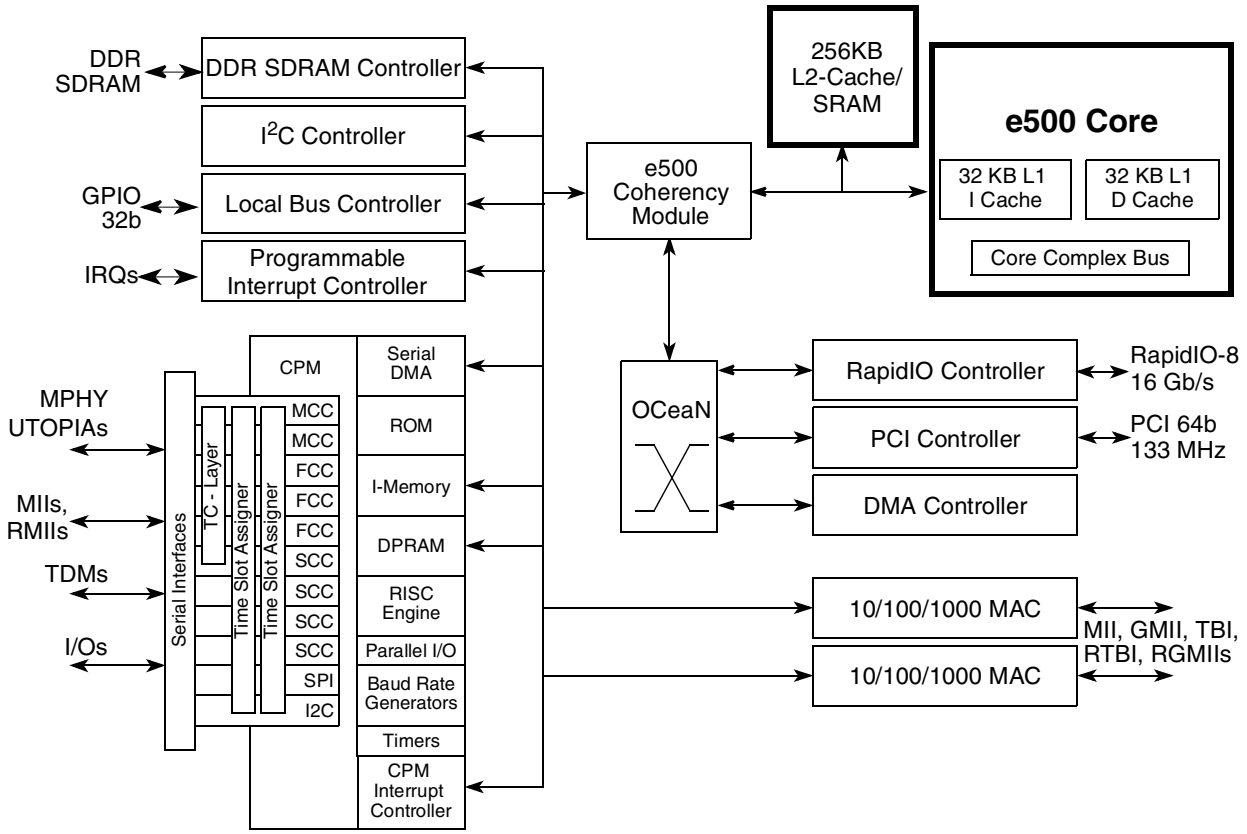


Figure 1. MPC8560 Block Diagram

1.1 Key Features

The following lists an overview of the MPC8560 feature set.

- High-performance, 32-bit Book E–enhanced core that implements the Power Architecture
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis. Separate locking for instructions and data
  - Memory management unit (MMU) especially designed for embedded applications
  - Enhanced hardware and software debug support
  - Performance monitor facility (similar to but different from the MPC8560 performance monitor described in Chapter 18, “Performance Monitor.”
- High-performance RISC CPM operating at up to 333 MHz
  - CPM software compatibility with previous PowerQUICC families
  - One instruction per clock

6 DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8560.

6.1 DDR SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8560.

Table 13. DDR SDRAM DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	4
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.18$	V	4
Output leakage current	I_{OZ}	–10	10	μA	5
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–15.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	15.2	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	100	μA	—

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. V_{IH} can tolerate an overshoot of 1.2V over GV_{DD} for a pulse width of ≤3 ns, and the pulse width cannot be greater than t_{MCK}. V_{IL} can tolerate an undershoot of 1.2V below GND for a pulse width of ≤3 ns, and the pulse width cannot be greater than t_{MCK}.
5. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

Table 14 provides the DDR capacitance.

Table 14. DDR SDRAM Capacitance

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, MSYNC_IN	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak to peak) = 0.2 V.

6.2.2 DDR SDRAM Output AC Timing Specifications

For chip selects $\overline{\text{MCS1}}$ and $\overline{\text{MCS2}}$, there will always be at least 200 DDR memory clocks coming out of self-refresh after an $\overline{\text{HRESET}}$ before a precharge occurs. This will not necessarily be the case for chip selects $\overline{\text{MCS0}}$ and $\overline{\text{MCS3}}$.

6.2.2.1 DLL Enabled Mode

Table 16 and Table 17 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface with the DDR DLL enabled.

Table 16. DDR SDRAM Output AC Timing Specifications–DLL Mode

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing)	t_{MCK}	6	10	ns	2
On chip Clock Skew	$t_{MCKSKEW}$	—	150	ps	3, 8
MCK[n] duty cycle	t_{MCKH}/t_{MCK}	45	55	%	8
ADDR/CMD output valid	t_{DDKHOV}	—	3	ns	4, 9
ADDR/CMD output invalid	t_{DDKHOX}	1	—	ns	4, 9
Write CMD to first MDQS capture edge	t_{DDSHMH}	t_{MCK} + 1.5	t_{MCK} + 4.0	ns	5
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 900 1100 1200	—	ps	6, 9
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 900 1100 1200	—	ps	6, 9
MDQS preamble start	t_{DDSHMP}	0.75 × t_{MCK} + 1.5	0.75 × t_{MCK} + 4.0	ns	7, 8

Table 16. DDR SDRAM Output AC Timing Specifications–DLL Mode (continued)

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDSHME}	1.5	4.0	ns	7, 8

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (OX or DX). For example, t_{DDKHOV} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (O) are valid (V) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. Maximum possible clock skew between a clock MCK[n] and its relative inverse clock $\overline{\text{MCK}}$[n], or between a clock MCK[n] and a relative clock MCK[m] or MSYNC_OUT. Skew measured between complementary signals at $GV_{DD}/2$.
4. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$ and MDQ/MECC/MDM/MDQS.
5. Note that t_{DDSHMH} follows the symbol conventions described in note 1. For example, t_{DDSHMH} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) until the MDQS signal is valid (MH). t_{DDSHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. These controls allow the relationship between the synchronous clock control timing and the source-synchronous DQS domain to be modified by the user. For best turnaround times, these may need to be set to delay t_{DDSHMH} an additional $0.25t_{MCK}$. This will also affect t_{DDSHMP} and t_{DDSHME} accordingly. See the *MPC8560 PowerQUICC III Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8560.
7. All outputs are referenced to the rising edge of MSYNC_IN (S) at the pins of the MPC8560. Note that t_{DDSHMP} follows the symbol conventions described in note 1. For example, t_{DDSHMP} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) for the duration of the MDQS signal precharge period (MP).
8. Guaranteed by design.
9. Guaranteed by characterization.

Figure 5 provides the AC test load for the DDR bus.

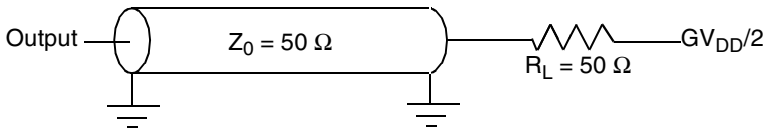


Figure 5. DDR AC Test Load

Table 17. DDR SDRAM Measurement Conditions

Symbol	DDR	Unit	Notes
V_{TH}	MV_{REF} ± 0.31 V	V	1
V_{OUT}	0.5 × GV_{DD}	V	2

Notes:

1. Data input threshold measurement point.
2. Data output measurement point.

Figure 14 shows the RGMII and RTBI AC timing and multiplexing diagrams.

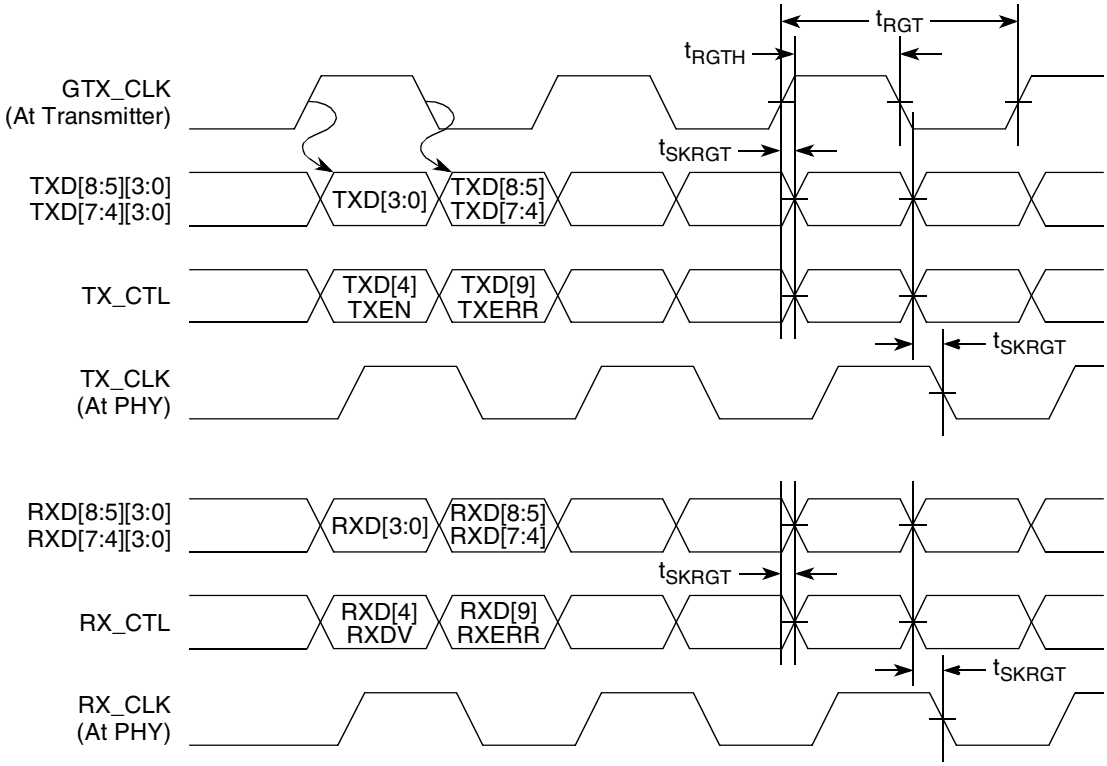


Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

7.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 7.1, "Three-Speed Ethernet Controller (TSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics."

7.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 28.

Table 28. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.13	3.47	V
Output high voltage (OV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	1.70	—	V
Input low voltage	V_{IL}	—	0.90	V

Figure 15 shows the MII management AC timing diagram.

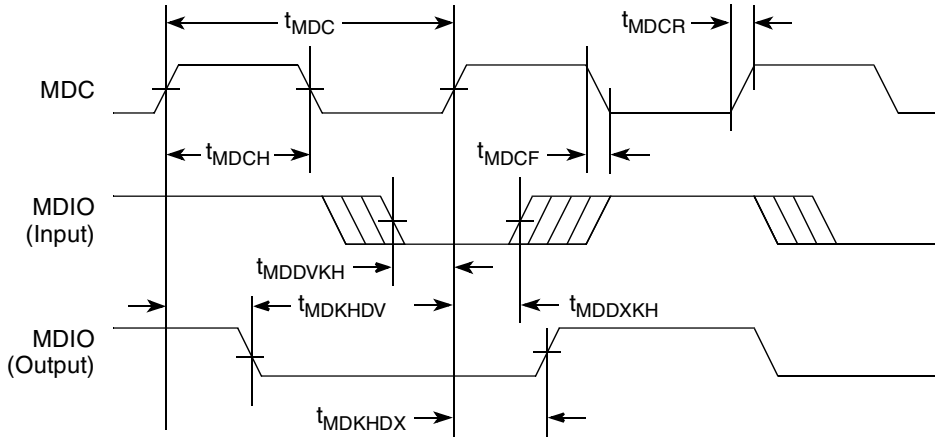


Figure 15. MII Management Interface Timing Diagram

8 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8560.

8.1 Local Bus DC Electrical Characteristics

Table 30 provides the DC electrical characteristics for the local bus interface.

Table 30. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	OV_{DD} - 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.2	V

Note:

1.Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

8.2 Local Bus AC Electrical Specifications

Table 31 describes the general timing parameters of the local bus interface of the MPC8560 with the DLL enabled.

Table 31. Local Bus General Timing Parameters—DLL Enabled

Parameter	POR Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	—	t_{LBK}	6.0	—	ns	2
LCLK[n] skew to LCLK[m] or LSYNC_OUT	—	$t_{LBKSKEW}$	—	150	ps	3, 9

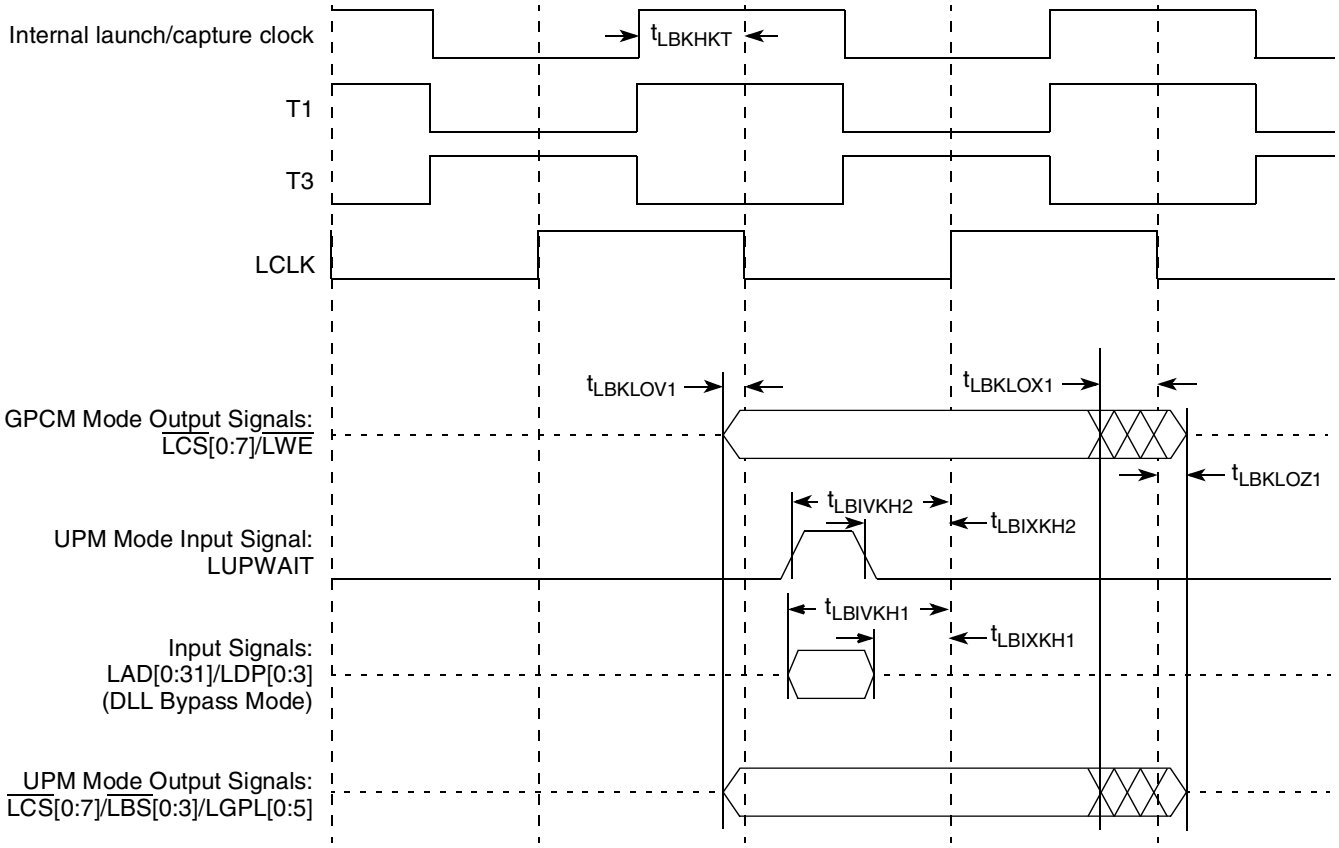


Figure 20. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

Figure 24 shows the FCC internal clock.

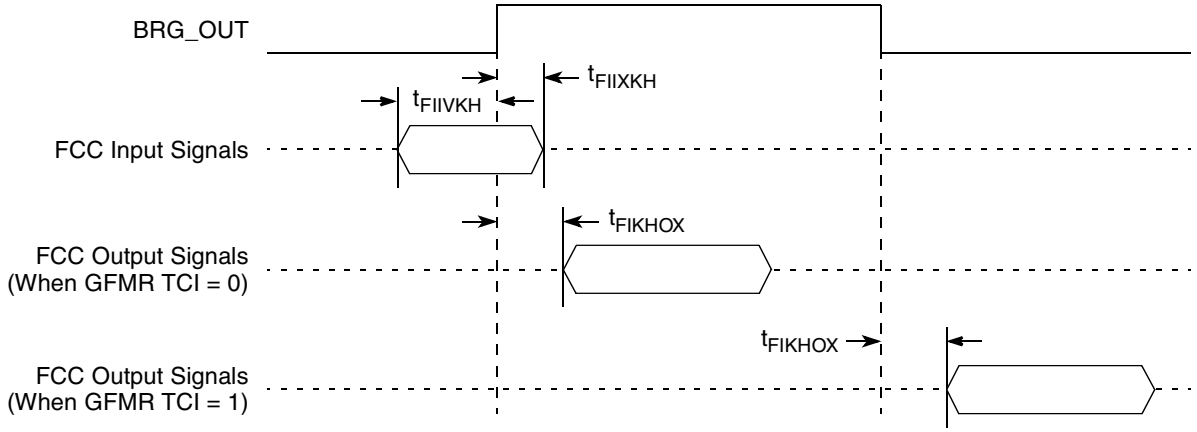


Figure 24. FCC Internal AC Timing Clock Diagram

Figure 25 shows the FCC external clock.

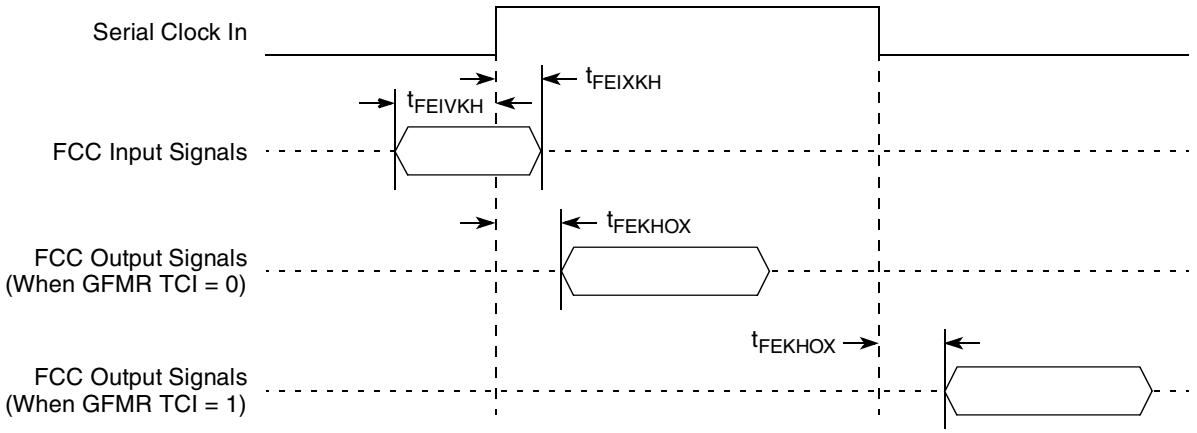


Figure 25. FCC External AC Timing Clock Diagram

Figure 26 shows Ethernet collision timing on FCCs.

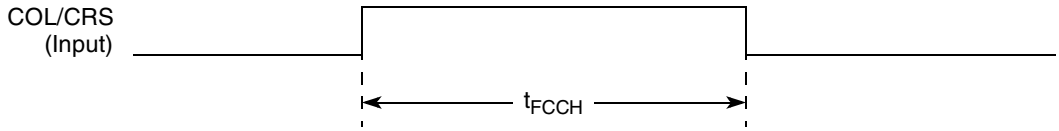
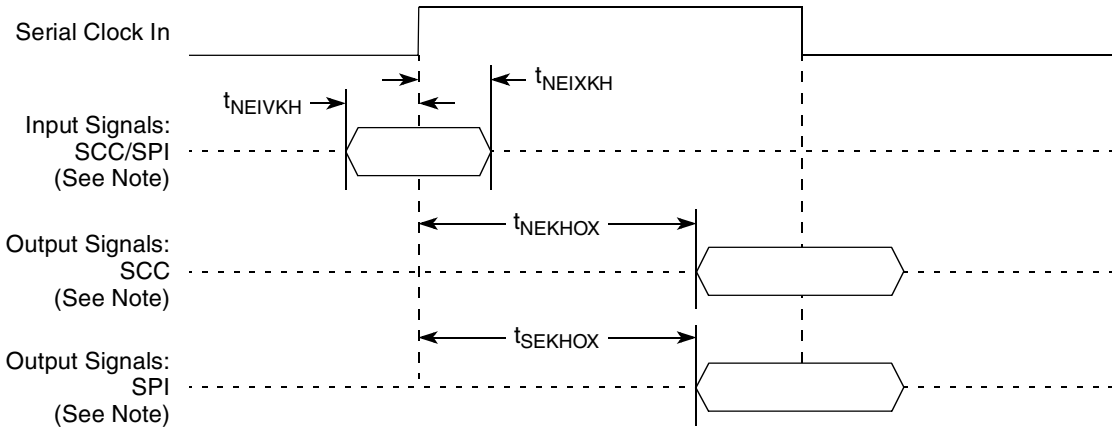


Figure 26. Ethernet Collision AC Timing Diagram (FCC)

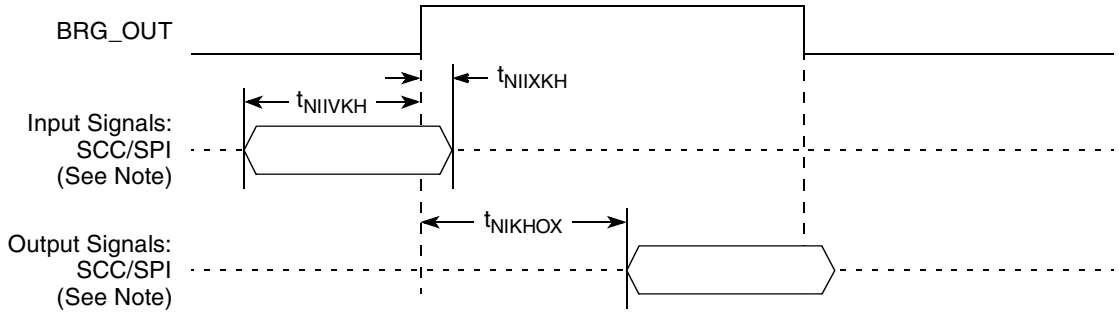
Figure 27 shows the SCC/SPI external clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 27. SCC/SPI AC Timing External Clock Diagram

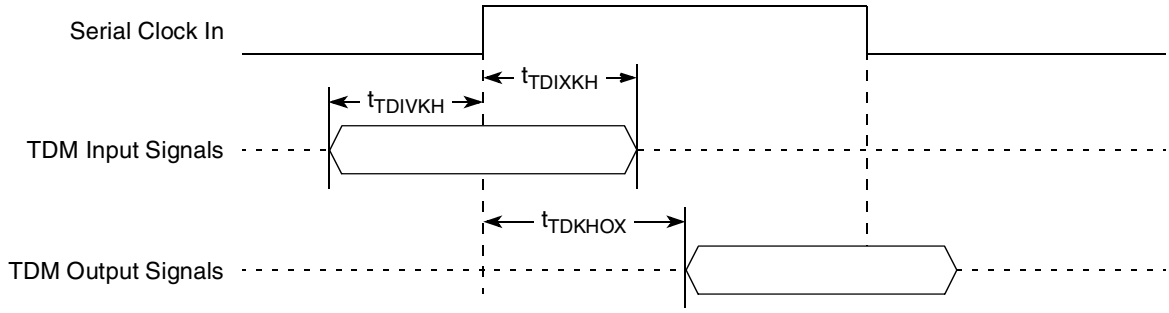
Figure 28 shows the SCC/SPI internal clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 28. SCC/SPI AC Timing Internal Clock Diagram

Figure 29 shows TDM input and output signals.



Note: There are 4 possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 29. TDM Signal AC Timing Diagram

10 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8560.

Table 39 provides the JTAG AC timing specifications as defined in Figure 32 through Figure 35.

Table 39. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions (see Table 2).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	6
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 4 4	 20 25	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}		—	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 3 3	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 31). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design.

Figure 16 provides the AC test load for PCI and PCI-X.

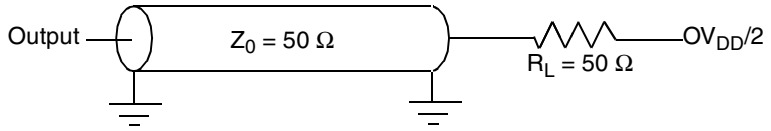


Figure 38. PCI/PCI-X AC Test Load

Figure 39 shows the PCI/PCI-X input AC timing conditions.

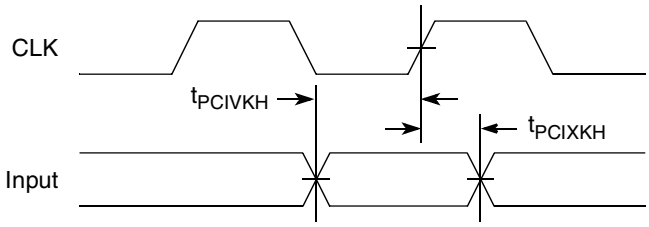


Figure 39. PCI-PCI-X Input AC Timing Measurement Conditions

Figure 40 shows the PCI/PCI-X output AC timing conditions.

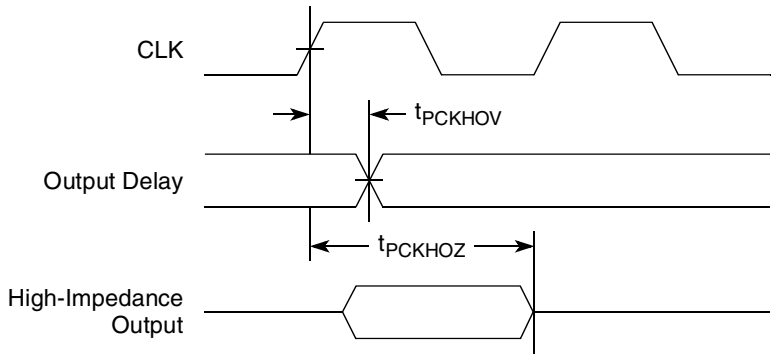


Figure 40. PCI-PCI-X Output AC Timing Measurement Condition

Table 44 provides the PCI-X AC timing specifications at 66 MHz.

Table 44. PCI-X AC Timing Specifications at 66 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	—	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t_{PCKHOX}	0.7	—	ns	1, 10
SYSCLK to output high impedance	t_{PCKHOZ}	—	7	ns	1, 4, 8, 11
Input setup time to SYSCLK	t_{PCIVKH}	1.7	—	ns	3, 5
Input hold time from SYSCLK	t_{PCIXKH}	0.5	—	ns	10
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time	t_{PCRVRH}	10	—	clocks	11
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	11
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	9, 11

Table 44. PCI-X AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	—	clocks	11
$\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time	t_{PCRHIX}	0	50	ns	6, 11

Notes:

1.See the timing measurement conditions in the *PCI-X 1.0a Specification*.

2.Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.

3.Setup time for point-to-point signals applies to $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ only. All other signals are bused.

4.For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

5.Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.

6.Maximum value is also limited by delay to the first transaction (time for $\overline{\text{HRESET}}$ high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of $\overline{\text{HRESET}}$ must be negated no later than two clocks before the first $\overline{\text{FRAME}}$ and must be floated no later than one clock before $\overline{\text{FRAME}}$ is asserted.

7.A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.

8.Device must meet this specification independent of how many outputs switch simultaneously.

9.The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*

10.Guaranteed by characterization.

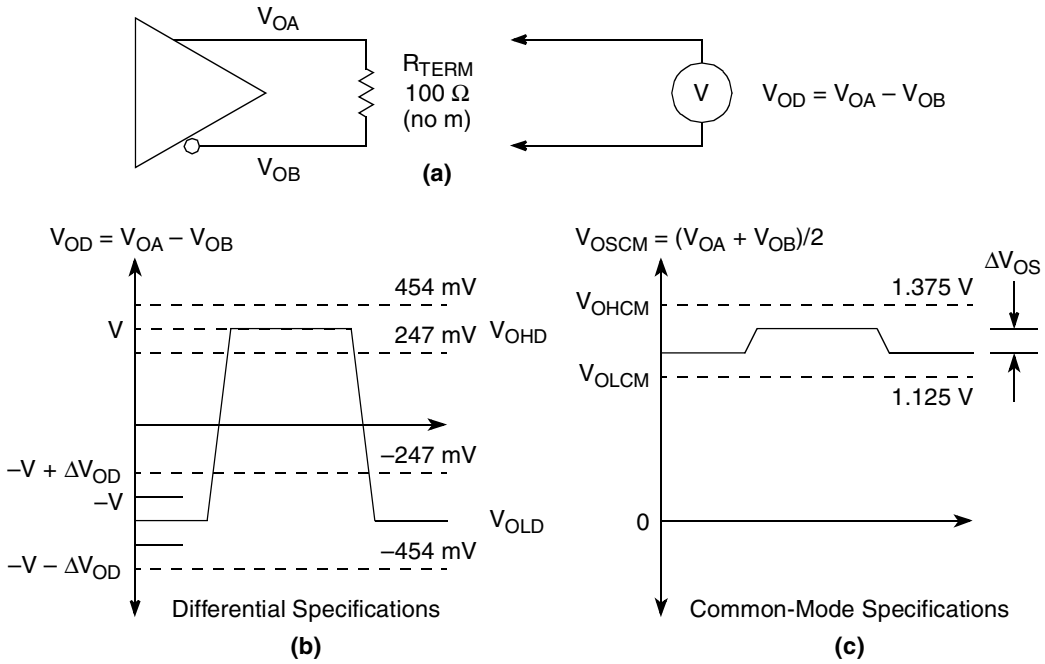
11.Guaranteed by design.

Table 45 provides the PCI-X AC timing specifications at 133 MHz.

Table 45. PCI-X AC Timing Specifications at 133 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	—	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t_{PCKHOX}	0.7	—	ns	1, 11
SYSCLK to output high impedance	t_{PCKHOZ}	—	7	ns	1, 4, 8, 12
Input setup time to SYSCLK	t_{PCIVKH}	1.4	—	ns	3, 5, 9, 11
Input hold time from SYSCLK	t_{PCIXKH}	0.5	—	ns	11
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time	t_{PCRVRH}	10	—	clocks	12
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	12
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	10, 12
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	—	clocks	12

Figure 41 shows the DC driver signal levels.



Note: V_{OA} refers to voltage at output A; V_{OB} refers to voltage at output B.

Figure 41. DC Driver Signal Levels

13.2 RapidIO AC Electrical Specifications

This section contains the AC electrical specifications for a RapidIO 8/16 LP-LVDS device. The interface defined is a parallel differential low-power high-speed signal interface. Note that the source of the transmit clock on the RapidIO interface is dependent on the settings of the LGPL[0:1] signals at reset. Note that the default setting makes the core complex bus (CCB) clock the source of the transmit clock. See Chapter 4 of the Reference Manual for more details on reset configuration settings.

13.3 RapidIO Concepts and Definitions

This section specifies signals using differential voltages. Figure 42 shows how the signals are defined. The figure shows waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- The transmitter output and receiver input signals TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ each have a peak-to-peak swing of A-B volts.
- The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} - V_{\overline{TD}}$.
- The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} - V_{\overline{RD}}$.
- The differential output signal of the transmitter or input signal of the receiver, ranges from A – B volts to – (A – B) volts.

Table 50. RapidIO Driver AC Timing Specifications—1 Gbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential output high voltage	V_{OHD}	200	540	mV	1
Differential output low voltage	V_{OLD}	–540	–200	mV	1
Duty cycle	DC	48	52	%	2, 6
V_{OD} rise time, 20%–80% of peak to peak differential signal swing	t_{FALL}	100	—	ps	3, 6
V_{OD} fall time, 20%–80% of peak to peak differential signal swing	t_{RISE}	100	—	ps	6
Data valid	DV	575	—	ps	6
Skew of any two data outputs	t_{DPAIR}	—	100	ps	4, 6
Skew of single data outputs to associated clock	$t_{SKEW,PAIR}$	–100	100	ps	5, 6

Notes:

1.See Figure 44.

2.Requires ±100 ppm long term frequency stability.

3.Measured at V_{OD} = 0 V.

4.Measured using the RapidIO transmit mask shown in Figure 44.

5.See Figure 49.

6.Guaranteed by design.

The compliance of driver output signals TD[0:15] and TFRAME with their minimum data valid window (DV) specification shall be determined by generating an eye pattern for each of the data signals and comparing the eye pattern of each data signal with the RapidIO transmit mask shown in Figure 44. The value of X2 used to construct the mask shall be $(1 - DV_{min})/2$. A signal is compliant with the data valid window specification if the transmit mask can be positioned on the signal's eye pattern such that the eye pattern falls entirely within the unshaded portion of the mask.

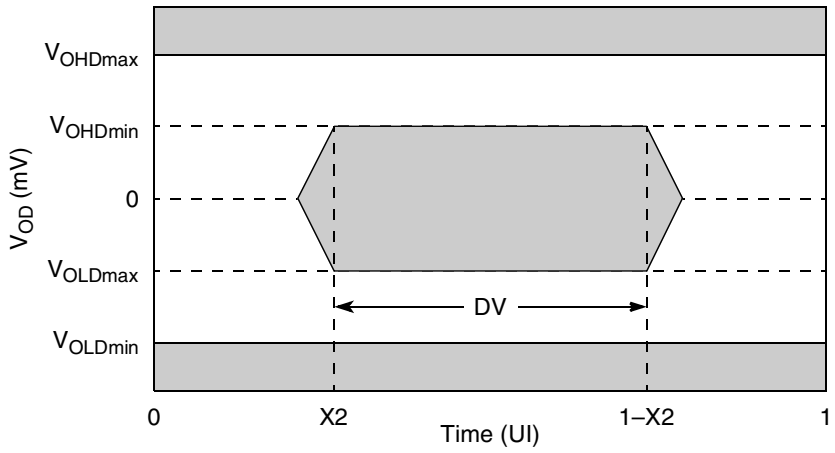


Figure 44. RapidIO Transmit Mask

13.3.2 RapidIO Receiver AC Timing Specifications

The RapidIO receiver AC timing specifications are provided in Table 51. A receiver shall comply with the specifications for each data rate/frequency for which operation of the receiver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The specifications apply over the receiver common mode and differential input voltage ranges.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7])

Table 51. RapidIO Receiver AC Timing Specifications—500 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1, 5
Data valid	DV	1080		ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}	—	380	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–300	300	ps	4

Notes:
1.Measured at V_{ID} = 0 V.
2.Measured using the RapidIO receive mask shown in Figure 46.
3.See Figure 49.
4.See Figure 48 and Figure 49.
5.Guaranteed by design.

Table 52. RapidIO Receiver AC Timing Specifications—750 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1, 5
Data valid	DV	600	—	ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}	—	400	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–267	267	ps	4

Notes:
1.Measured at V_{ID} = 0 V.
2.Measured using the RapidIO receive mask shown in Figure 46.
3.See Figure 49.
4.See Figure 48 and Figure 49.
5.Guaranteed by design.

Table 53. RapidIO Receiver AC Timing Specifications—1 Gbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1, 5
Data valid	DV	425	—	ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}	—	300	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–200	200	ps	4

Notes:

1.Measured at V_{ID} = 0 V.

2.Measured using the RapidIO receive mask shown in Figure 46.

3.See Figure 49.

4.See Figure 48 and Figure 49.

5.Guaranteed by design.

The compliance of receiver input signals RD[0:15] and RFRAME with their minimum data valid window (DV) specification shall be determined by generating an eye pattern for each of the data signals and comparing the eye pattern of each data signal with the RapidIO receive mask shown in Figure 46. The value of X2 used to construct the mask shall be $(1 – DV_{min})/2$. The ±100 mV minimum data valid and ±600 mV maximum input voltage values are from the DC specification. A signal is compliant with the data valid window specification if and only if the receive mask can be positioned on the signal's eye pattern such that the eye pattern falls entirely within the unshaded portion of the mask.

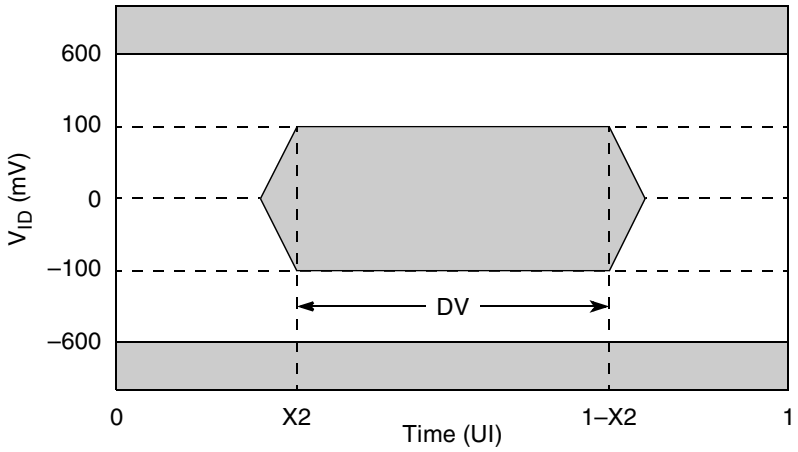


Figure 46. RapidIO Receive Mask

The eye pattern for a data signal is generated by making a large number of recordings of the signal and then overlaying the recordings. The number of recordings used to generate the eye shall be large enough that further increasing the number of recordings used does not cause the resulting eye pattern to change from one that complies with the RapidIO receive mask to one that does not. Each data signal in the interface shall be carrying random or pseudo-random data when the recordings are made. If pseudo-random data is used, the length of the pseudo-random sequence (repeat length) shall be long

15.2 Platform/System PLL Ratio

The platform clock is the clock that drives the L2 cache, the DDR SDRAM data rate, and the e500 core complex bus (CCB), and is also called the CCB clock. The values are determined by the binary value on LA[28:31] at power up, as shown in Table 57.

There is no default for this PLL ratio; these signals must be pulled to the desired values.

Table 57. CCB Clock Ratio

Binary Value of LA[28:31] Signals	Ratio Description
0000	16:1 ratio CCB clock: SYSCLK (PCI bus)
0001	Reserved
0010	2:1 ratio CCB clock: SYSCLK (PCI bus)
0011	3:1 ratio CCB clock: SYSCLK (PCI bus)
0100	4:1 ratio CCB clock: SYSCLK (PCI bus)
0101	5:1 ratio CCB clock: SYSCLK (PCI bus)
0110	6:1 ratio CCB clock: SYSCLK (PCI bus)
0111	Reserved
1000	8:1 ratio CCB clock: SYSCLK (PCI bus)
1001	9:1 ratio CCB clock: SYSCLK (PCI bus)
1010	10:1 ratio CCB clock: SYSCLK (PCI bus)
1011	Reserved
1100	12:1 ratio CCB clock: SYSCLK (PCI bus)
1101	Reserved
1110	Reserved
1111	Reserved

15.3 e500 Core PLL Ratio

Table 58 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LALE and LGPL2 at power up, as shown in Table 58.

Table 58. e500 Core to CCB Ratio

Binary Value of LALE, LGPL2 Signals	Ratio Description
00	2:1 e500 core:CCB
01	5:2 e500 core:CCB
10	3:1 e500 core:CCB
11	7:2 e500 core:CCB

When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

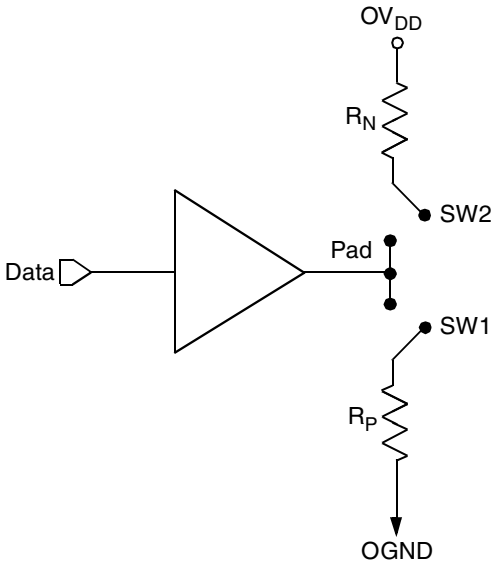


Figure 59. Driver Impedance Measurement

The output impedance of the RapidIO port drivers targets 200-Ω differential resistance. The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 61 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 61. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI/PCI-X	DDR DRAM	RapidIO	Symbol	Unit
R_N	43 Target	25 Target	20 Target	NA	Z_0	W
R_P	43 Target	25 Target	20 Target	NA	Z_0	W
Differential	NA	NA	NA	200 Target	Z_{DIFF}	W

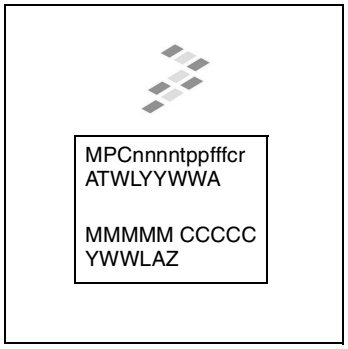
Note: Nominal supply voltages. See Table 1, T_j = 105°C.

Table 62. Document Revision History (continued)

Rev. No.	Substantive Change(s)
2.0	Section 1.1—Updated features list to coincide with latest version of the reference manual Table 1 and Table 2— Addition of CPM to OV_{DD} and OV_{IN}; Addition of SYSCLK to OV_{IN} Table 2—Addition of notes 1 and 2 Table 3—Addition of note 1 Table 5—New Section 4—New Table 13—Addition of I_{VREF} Table 15—Modified maximum values for t_{DISKEW} Table 16—Added MSYNC_OUT to $t_{MCKSKEW2}$ Figure 5—New Section 6.2.1—Removed Figure 4, "DDR SDRAM Input Timing Diagram" Section 7.1—Removed references to 2.5 V from first paragraph Figure 8—New Table 19 and Table 20—Modified “conditions” for I_{IH} and I_{IL} Table 21—Addition of min and max for GTX_CLK125 reference clock duty cycle Table 25—Addition of min and max for GTX_CLK125 reference clock duty cycle Table 27—Addition of min and max for GTX_CLK125 reference clock duty cycle Figure 17 and Figure 19—Changed LSYNC_IN to Internal clock at top of each figure Table 34—Modified values for t_{FIIVKH}, t_{NIIVKH}, and t_{TDIVKH}; addition of t_{PIIVKH} and t_{PIIXKH}. Table 35—Modified values for t_{FEKHOX}, t_{NIKHOX},t_{NEKHOX}, t_{TDKHOX}; addition of t_{PIKHOX}. Figure 16—New Figure 30—New Figure 16—New Figure 16—New Table 31—Removed row for $t_{LBKHOX3}$ Table 44—New (AC timing of PCI-X at 66 MHz) Table 54—Addition of note 19 Figure 61—Addition of jumper and note at top of diagram Table 56—Changed max bus freq for 667 core to 166 Section 16.2.1—Modified first paragraph Figure 52—Modified Figure 53—New Table 60—Modified thermal resistance data Section 16.2.4.2—Modified first and second paragraphs

19.2 Part Marking

Parts are marked as the example shown in Figure 62.



FC-PBGA

Notes:

MMMMM is the 5-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.
YWWLAZ is the assembly traceability code.

Figure 62. Part Marking for FC-PBGA Device