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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8560vtaqfb

1 Overview

The following section provides a high-level overview of the MPC8560 features. Figure 1 shows the major functional units within the MPC8560.

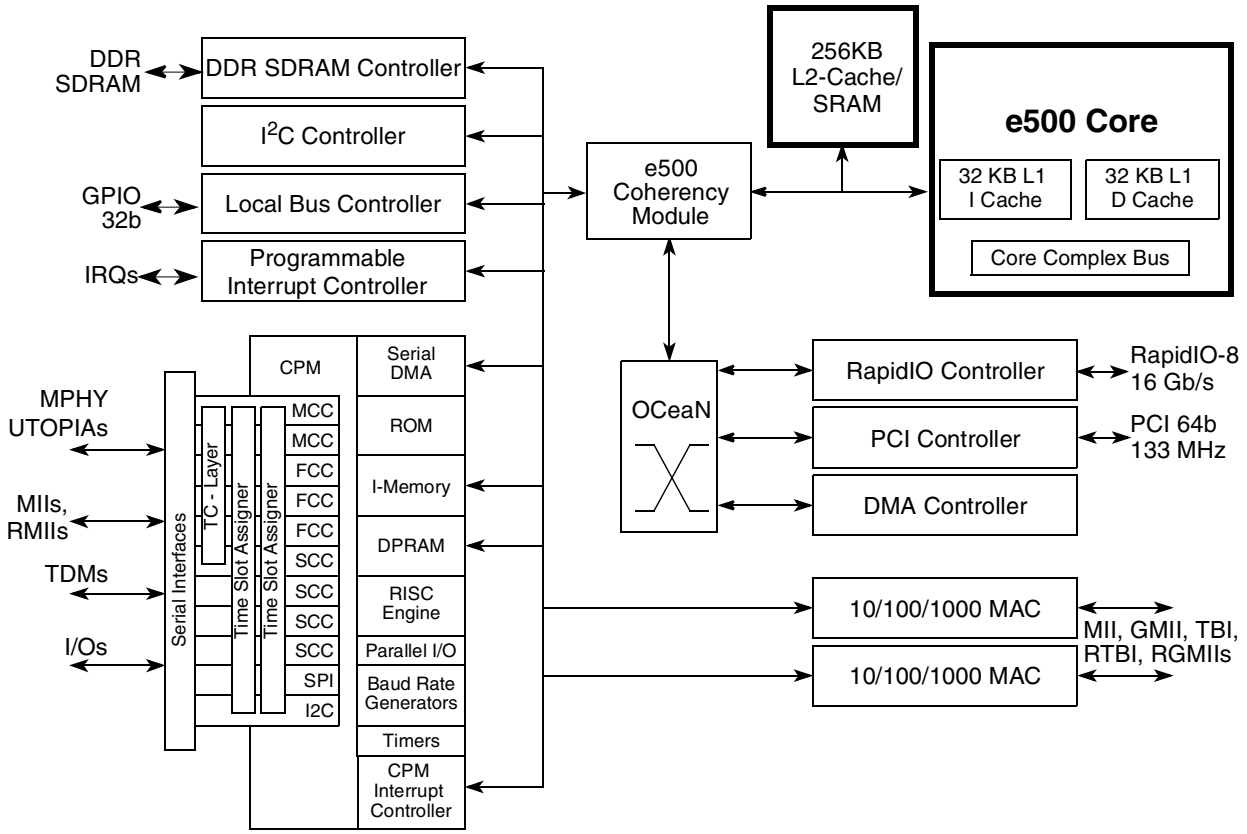


Figure 1. MPC8560 Block Diagram

1.1 Key Features

The following lists an overview of the MPC8560 feature set.

- High-performance, 32-bit Book E–enhanced core that implements the Power Architecture
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis. Separate locking for instructions and data
  - Memory management unit (MMU) especially designed for embedded applications
  - Enhanced hardware and software debug support
  - Performance monitor facility (similar to but different from the MPC8560 performance monitor described in Chapter 18, “Performance Monitor.”
- High-performance RISC CPM operating at up to 333 MHz
  - CPM software compatibility with previous PowerQUICC families
  - One instruction per clock

— Executes code from internal ROM or instruction RAM
— 32-bit RISC architecture
— Tuned for communication environments: instruction set supports CRC computation and bit manipulation.
— Internal timer
— Interfaces with the embedded e500 core processor through a 32-Kbyte dual-port RAM and virtual DMA channels for each peripheral controller
— Handles serial protocols and virtual DMA.
— Three full-duplex fast serial communications controllers (FCCs) that support the following protocols:
  – ATM protocol through UTOPIA interface (FCC1 and FCC2 only)
  – IEEE Std 802.3™/Fast Ethernet
  – HDLC
  – Totally transparent operation
— Two multi-channel controllers (MCCs) that together can handle up to 256 HDLC/transparent channels at 64 Kbps each, multiplexed on up to 8 TDM interfaces
— Four full-duplex serial communications controllers (SCCs) that support the following protocols:
  – High level/synchronous data link control (HDLC/SDLC)
  – LocalTalk (HDLC-based local area network protocol)
  – Universal asynchronous receiver transmitter (UART)
  – Synchronous UART (1x clock mode)
  – Binary synchronous communication (BISYNC)
  – Totally transparent operation
— Serial peripheral interface (SPI) support for master or slave
— I^2C bus controller
— Time-slot assigner supports multiplexing of data from any of the SCCs and FCCs onto eight time-division multiplexed (TDM) interfaces. The time-slot assigner supports the following TDM formats:
  – T1/CEPT lines
  – T3/E3
  – Pulse code modulation (PCM) highway interface
  – ISDN primary rate
  – Freescale interchip digital link (IDL)
  – General circuit interface (GCI)
— User-defined interfaces
— Eight independent baud rate generators (BRGs)
— Four general-purpose 16-bit timers or two 32-bit timers

  - Contiguous or discontiguous memory mapping
  - Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
  - Sleep mode support for self refresh SDRAM
  - Supports auto refreshing
  - On-the-fly power management using CKE signal
  - Registered DIMM support
  - Fast memory access via JTAG port
  - 2.5-V SSTL2 compatible I/O
- RapidIO interface unit
  - 8-bit RapidIO I/O and messaging protocols
  - Source-synchronous double data rate (DDR) interfaces
  - Supports small type systems (small domain, 8-bit device ID)
  - Supports four priority levels (ordering within a level)
  - Reordering across priority levels
  - Maximum data payload of 256 bytes per packet
  - Packet pacing support at the physical layer
  - CRC protection for packets
  - Supports atomic operations increment, decrement, set, and clear
  - LVDS signaling
- RapidIO–compliant message unit
  - One inbound data message structure (inbox)
  - One outbound data message structure (outbox)
  - Supports chaining and direct modes in the outbox
  - Support of up to 16 packets per message
  - Support of up to 256 bytes per packet and up to 4 Kbytes of data per message
  - Supports one inbound doorbell message structure
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts with 32-bit messages
  - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
  - Four global high resolution timers/counters that can generate interrupts
  - Supports 22 other internal interrupt sources
  - Supports fully nested interrupt delivery
  - Interrupts can be routed to external pin for external processing

6 DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8560.

6.1 DDR SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8560.

Table 13. DDR SDRAM DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	4
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.18$	V	4
Output leakage current	I_{OZ}	–10	10	μA	5
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–15.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	15.2	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	100	μA	—

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. V_{IH} can tolerate an overshoot of 1.2V over GV_{DD} for a pulse width of ≤3 ns, and the pulse width cannot be greater than t_{MCK}. V_{IL} can tolerate an undershoot of 1.2V below GND for a pulse width of ≤3 ns, and the pulse width cannot be greater than t_{MCK}.
5. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

Table 14 provides the DDR capacitance.

Table 14. DDR SDRAM Capacitance

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, MSYNC_IN	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak to peak) = 0.2 V.

7 Ethernet: Three-Speed, MII Management

This section provides the AC and DC electrical characteristics for three-speed and MII management.

7.1 Three-Speed Ethernet Controller (TSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII, MII, and TBI interfaces can be operated at 3.3 or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with the IEEE 802.3 standard. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 7.3, "Ethernet Management Interface Electrical Characteristics."

7.1.1 TSEC DC Electrical Characteristics

All GMII,MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 19 and Table 20. The potential applied to the input of a GMII,MII, TBI, RGMII, or RTBI receiver may exceed the potential of the receiver's power supply (i.e., a GMII driver powered from a 3.6 V supply driving V_{OH} into a GMII receiver powered from a 2.5 V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5 V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 19. GMII, MII, and TBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3 V	LV_{DD}	3.13	3.47	V
Output high voltage (LV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.40	LV_{DD} + 0.3	V
Output low voltage (LV_{DD} = Min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	1.70	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	–0.3	0.90	V
Input high current (V_{IN} [1] = LV_{DD})	I_{IH}	—	40	μA
Input low current (V_{IN} [1] = GND)	I_{IL}	–600	—	μA

Note:
1.The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

7.2.3.2 TBI Receive AC Timing Specifications

Table 26 provides the TBI receive AC timing specifications.

Table 26. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRX}		16.0		ns
RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising RX_CLK	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising RX_CLK	t_{TRDXKH}	1.5	—	—	ns
RX_CLK clock rise time and fall time	t_{TRXR}, t_{TRXF} [2,3]	0.7	—	2.4	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 13 shows the TBI receive AC timing diagram.

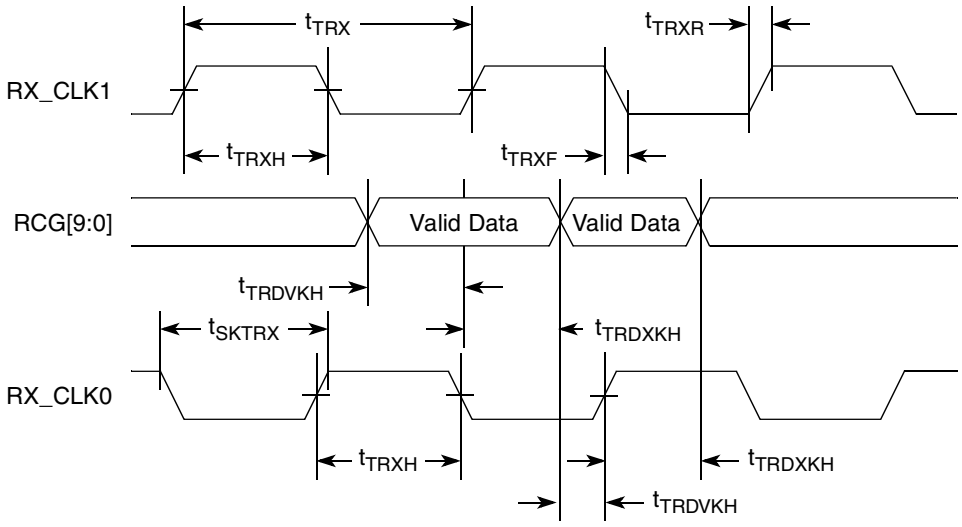


Figure 13. TBI Receive AC Timing Diagram

Figure 14 shows the RGMII and RTBI AC timing and multiplexing diagrams.

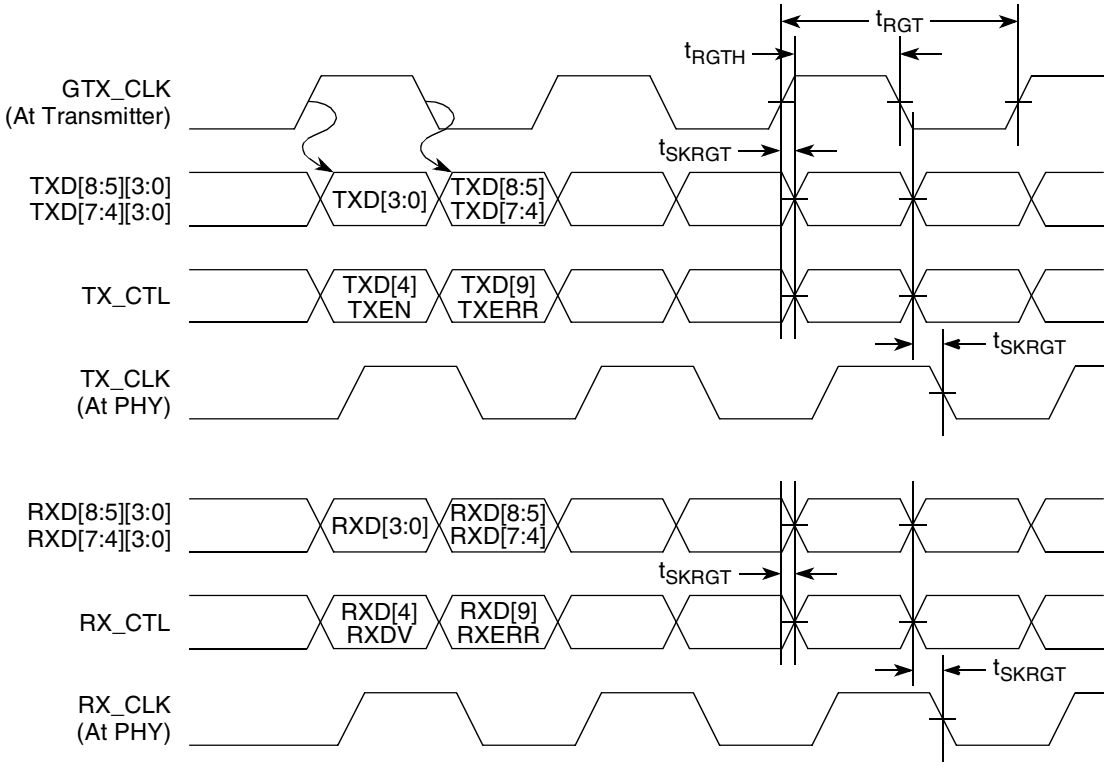


Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

7.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 7.1, "Three-Speed Ethernet Controller (TSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics."

7.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 28.

Table 28. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.13	3.47	V
Output high voltage (OV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	1.70	—	V
Input low voltage	V_{IL}	—	0.90	V

Figure 15 shows the MII management AC timing diagram.

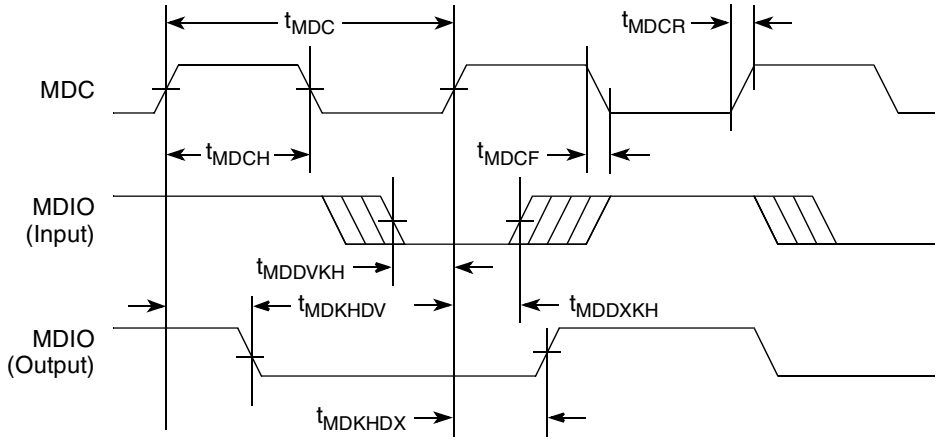


Figure 15. MII Management Interface Timing Diagram

8 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8560.

8.1 Local Bus DC Electrical Characteristics

Table 30 provides the DC electrical characteristics for the local bus interface.

Table 30. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	OV_{DD} - 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.2	V

Note:

1.Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

8.2 Local Bus AC Electrical Specifications

Table 31 describes the general timing parameters of the local bus interface of the MPC8560 with the DLL enabled.

Table 31. Local Bus General Timing Parameters—DLL Enabled

Parameter	POR Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	—	t_{LBK}	6.0	—	ns	2
LCLK[n] skew to LCLK[m] or LSYNC_OUT	—	$t_{LBKSKEW}$	—	150	ps	3, 9

Table 32. Local Bus General Timing Parameters—DLL Bypassed (continued)

Parameter	POR Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to data valid for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKLOV2}$	—	-0.1	ns	4
	TSEC2_TXD[6:5] = 11 (default)			1.4		
Local bus clock to address valid for LAD	TSEC2_TXD[6:5] = 00	$t_{LBKLOV3}$	—	0	ns	4
	TSEC2_TXD[6:5] = 11 (default)			1.5		
Local bus clock to LALE assertion		$t_{LBKHOV4}$	—	0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKLOX1}$	-3.2	—	ns	4
	TSEC2_TXD[6:5] = 11 (default)		-2.3			
Output hold from local bus clock for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKLOX2}$	-3.2	—	ns	4
	TSEC2_TXD[6:5] = 11 (default)		-2.3			
Local bus clock to output high Impedance (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKLOZ1}$	—	0.2	ns	7
	TSEC2_TXD[6:5] = 11 (default)			1.5		
Local bus clock to output high impedance for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKLOZ2}$	—	0.2	ns	7
	TSEC2_TXD[6:5] = 11 (default)			1.5		

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for DLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t_{LBKHKT}.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $OV_{DD}/2$.
4. All signals are measured from $OV_{DD}/2$ of the rising edge of local bus clock for DLL bypass mode to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins TSEC2_TXD[6:5].
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.
9. Guaranteed by design.

Table 36 shows CPM I^{2}C AC Timing.

Table 36. CPM I^{2}C AC Timing

Characteristic	Symbol	Min	Max	Unit
SCL clock frequency (slave)	f_{SCL}	0	F_{MAX}[1]	Hz
SCL clock frequency (master)	f_{SCL}	BRGCLK/16512	BRGCLK/48	Hz
Bus free time between transmissions	t_{SDHDL}	1/(2.2 * f_{SCL})	—	s
Low period of SCL	t_{SCLCH}	1/(2.2 * f_{SCL})	—	s
High period of SCL	t_{SCHCL}	1/(2.2 * f_{SCL})	—	s
Start condition setup time [2]	t_{SCHDL}	2/(divider * f_{SCL})	—	s
Start condition hold time [2]	t_{SDLCL}	3/(divider * f_{SCL})	—	s
Data hold time [2]	t_{SCLDX}	2/(divider * f_{SCL})	—	s
Data setup time [2]	t_{SDVCH}	3/(divider * f_{SCL})	—	s
SDA/SCL rise time	t_{SRISE}	—	1/(10 * f_{SCL})	s
SDA/SCL fall time	t_{SFALL}	—	1/(33 * f_{SCL})	s
Stop condition setup time	t_{SCHDH}	2/(divider * f_{SCL})	—	s

Notes:

1. F_{MAX} = BRGCLK/(min_divider*prescaler). Where prescaler=25-I2MODE[PDIV]; and min_divider=12 if digital filter disabled and 18 if enabled.
   Example #1: if I2MODE[PDIV]=11 (prescaler=4) and I2MODE[FLT]=0 (digital filter disabled) then FMAX=BRGCLK/48
   Example #2: if I2MODE[PDIV]=00 (prescaler=32) and I2MODE[FLT]=1 (digital filter enabled) then FMAX=BRGCLK/576
2. divider = f_{SCL}/prescaler.
   In master mode: divider = BRGCLK/(f_{SCL}*prescaler) = 2*(I2BRG[DIV]+3)
   In slave mode: divider = BRGCLK/(f_{SCL}*prescaler)

Figure 30 is a a diagram of CPM I^{2}C Bus Timing.

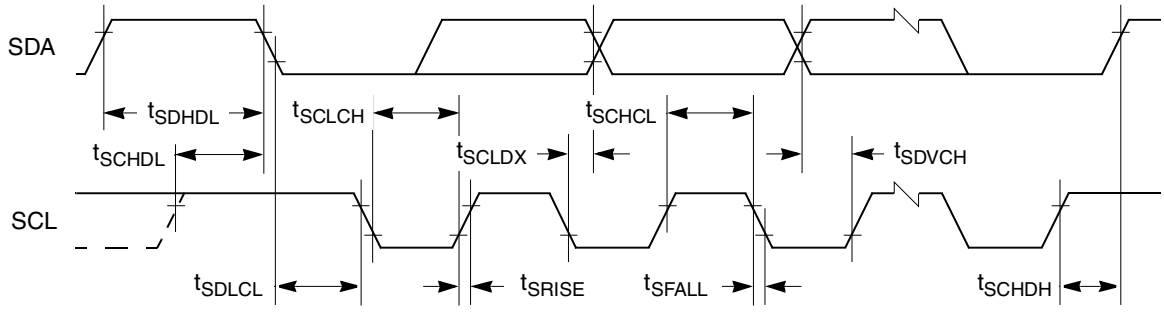


Figure 30. CPM I^{2}C Bus Timing Diagram

Figure 31 provides the AC test load for TDO and the boundary-scan outputs of the MPC8560.

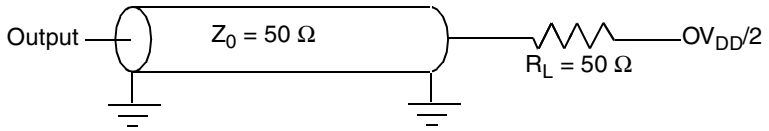


Figure 31. AC Test Load for the JTAG Interface

Figure 32 provides the JTAG clock input timing diagram.

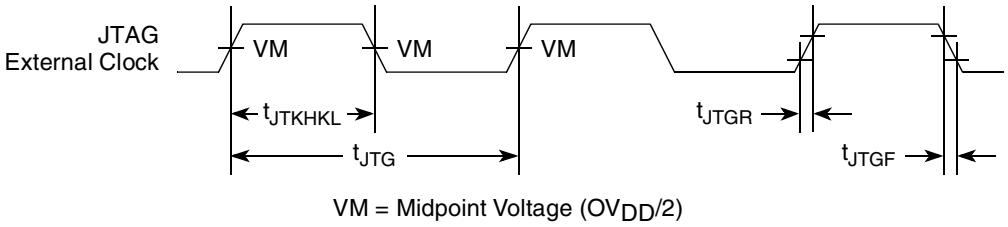


Figure 32. JTAG Clock Input Timing Diagram

Figure 33 provides the $\overline{\text{TRST}}$ timing diagram.

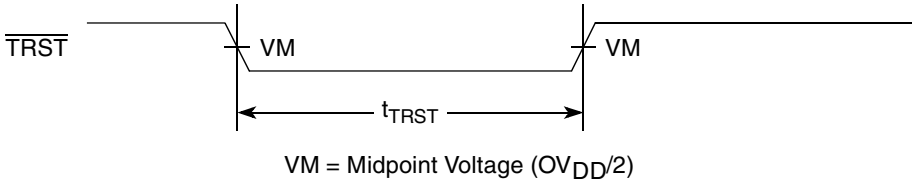


Figure 33. $\overline{\text{TRST}}$ Timing Diagram

Figure 34 provides the boundary-scan timing diagram.

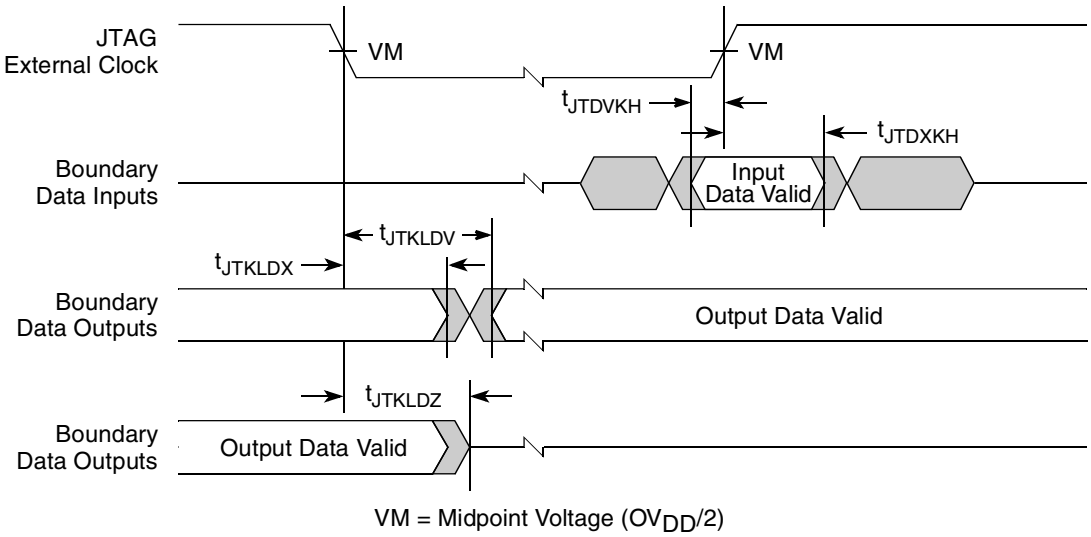


Figure 34. Boundary-Scan Timing Diagram

3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
7. The socket lid must always be oriented to A1.

14.3 Pinout Listings

Table 54 provides the pin-out listing for the MPC8560, 783 FC-PBGA package.

Table 54. MPC8560 Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI/PCI-X				
PCI_AD[63:0]	AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14, V15, W15, Y15, AA15, AB15, AC15, AD15, AG15, AH15, V16, W16, AB16, AC16, AD16, AE16, AF16, V17, W17, Y17, AA17, AB17, AE17, AF17, AF18, AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9, AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11, AG11, AH11, V12, W12, Y12, AB12, AD12, AE12, AG12, AH12, V13, Y13, AB13, AC13	I/O	OV_{DD}	17
PCI_C_$\overline{BE}$[7:0]	AG13, AH13, V14, W14, AH8, AB10, AD11, AC12	I/O	OV_{DD}	17
PCI_PAR	AA11	I/O	OV_{DD}	—
PCI_PAR64	Y14	I/O	OV_{DD}	—
$\overline{\text{PCI\_FRAME}}$	AC10	I/O	OV_{DD}	2
$\overline{\text{PCI\_TRDY}}$	AG10	I/O	OV_{DD}	2
$\overline{\text{PCI\_IRDY}}$	AD10	I/O	OV_{DD}	2
$\overline{\text{PCI\_STOP}}$	V11	I/O	OV_{DD}	2
$\overline{\text{PCI\_DEVSEL}}$	AH10	I/O	OV_{DD}	2
PCI_IDSEL	AA9	I	OV_{DD}	—
$\overline{\text{PCI\_REQ64}}$	AE13	I/O	OV_{DD}	5, 10
$\overline{\text{PCI\_ACK64}}$	AD13	I/O	OV_{DD}	2
$\overline{\text{PCI\_PERR}}$	W11	I/O	OV_{DD}	2
$\overline{\text{PCI\_SERR}}$	Y11	I/O	OV_{DD}	2, 4
$\overline{\text{PCI\_REQ0}}$	AF5	I/O	OV_{DD}	—
$\overline{\text{PCI\_REQ}}$[1:4]	AF3, AE4, AG4, AE5	I	OV_{DD}	—
$\overline{\text{PCI\_GNT}}$[0]	AE6	I/O	OV_{DD}	—
$\overline{\text{PCI\_GNT}}$[1:4]	AG5, AH5, AF6, AG6	O	OV_{DD}	5, 9

Table 54. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
RIO_RD[0:7]	T25, U25, V25, W25, AA25, AB25, AC25, AD25	I	OV_{DD}	—
$\overline{\text{RIO\_RD}}$[0:7]	T24, U24, V24, W24, AA24, AB24, AC24, AD24	I	OV_{DD}	—
RIO_RFRAME	AE27	I	OV_{DD}	—
$\overline{\text{RIO\_RFRAME}}$	AE26	I	OV_{DD}	—
RIO_TCLK	AC20	O	OV_{DD}	11
$\overline{\text{RIO\_TCLK}}$	AE21	O	OV_{DD}	11
RIO_TD[0:7]	AE18, AC18, AD19, AE20, AD21, AE22, AC22, AD23	O	OV_{DD}	—
$\overline{\text{RIO\_TD}}$[0:7]	AD18, AE19, AC19, AD20, AC21, AD22, AE23, AC23	O	OV_{DD}	—
RIO_TFRAME	AE24	O	OV_{DD}	—
$\overline{\text{RIO\_TFRAME}}$	AE25	O	OV_{DD}	—
RIO_TX_CLK_IN	AF24	I	OV_{DD}	—
$\overline{\text{RIO\_TX\_CLK\_IN}}$	AF25	I	OV_{DD}	—
I^2C interface				
IIC_SDA	AH22	I/O	OV_{DD}	4, 20
IIC_SCL	AH23	I/O	OV_{DD}	4, 20
System Control				
$\overline{\text{HRESET}}$	AH16	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	AG20	O	OV_{DD}	—
$\overline{\text{SRESET}}$	AF20	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN}}$	M11	I	OV_{DD}	—
$\overline{\text{CKSTP\_OUT}}$	G1	O	OV_{DD}	2, 4
Debug				
TRIG_IN	N12	I	OV_{DD}	—
TRIG_OUT/READY	G2	O	OV_{DD}	6, 9, 19
MSRCID[0:1]	J9, G3	O	OV_{DD}	5, 6, 9
MSRCID[2:4]	F3, F5, F2	O	OV_{DD}	6
MDVAL	F4	O	OV_{DD}	6
Clock				
SYSCLK	AH21	I	OV_{DD}	—
RTC	AB23	I	OV_{DD}	—
CLK_OUT	AF22	O	OV_{DD}	11

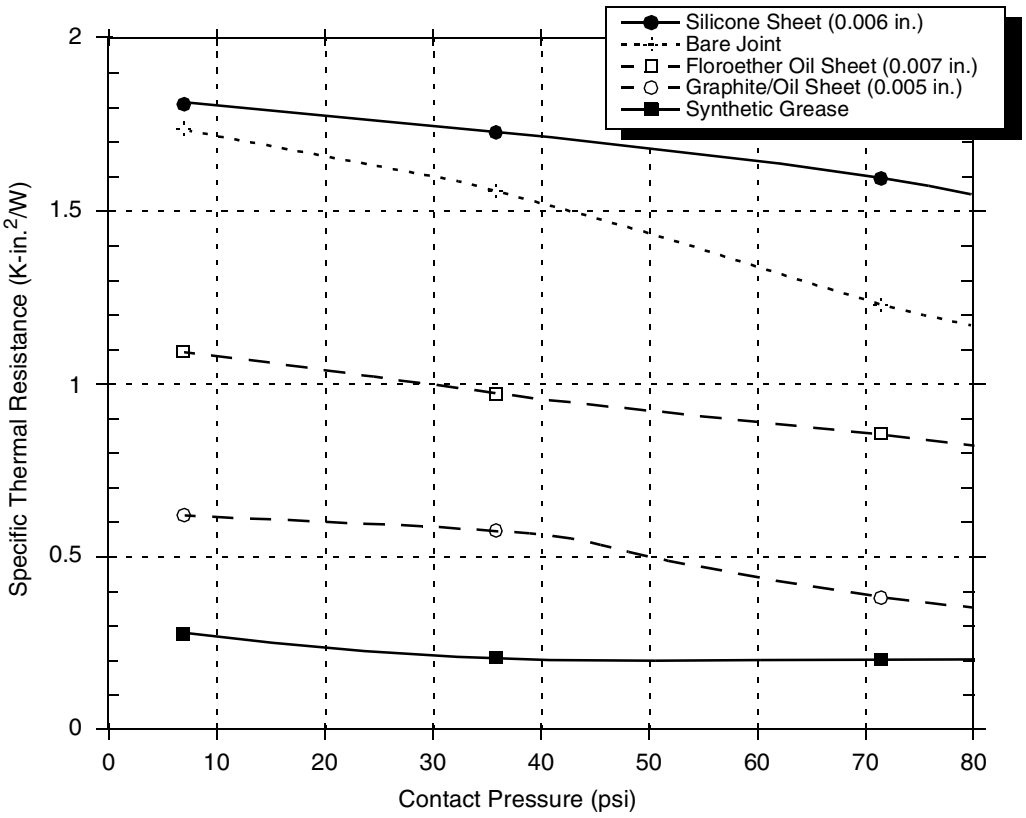
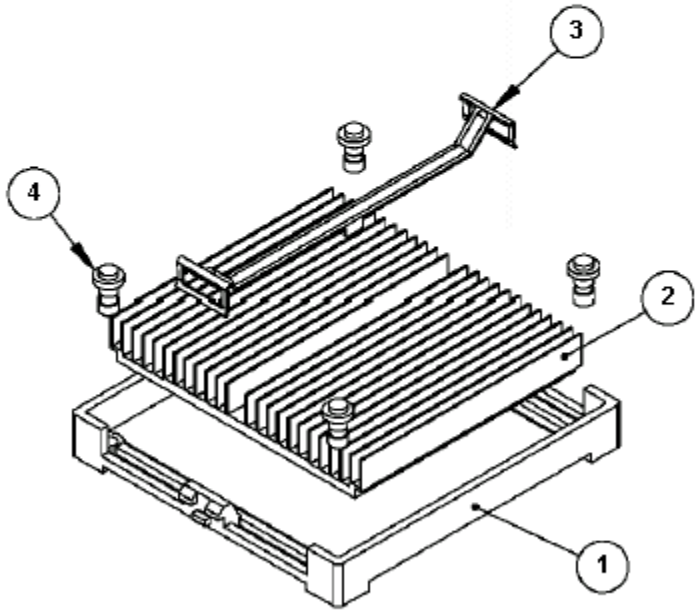


Figure 54. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

Item No	QTY	MEI PN	Description
1	1	MFRAME-2000	HEATSINK FRAME
2	1	MSNK-1120	EXTRUDED HEATSINK
3	1	MCLIP-1013	CLIP
4	4	MPPINS-1000	FRAME ATTACHMENT PINS



Illustrative source provided by
Millennium Electronics (MEI)

Figure 57. Exploded Views (2) of a Heat Sink Attachment using a Plastic Fence

The die junction-to-ambient and the heat sink-to-ambient thermal resistances are common figure-of-merits used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature: airflow, board population (local heat flux of adjacent components), system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the boards, as well as, system-level designs.

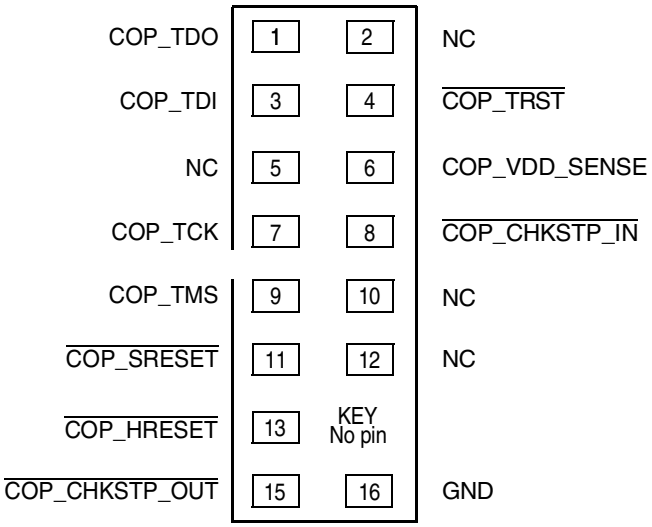


Figure 60. COP Connector Physical Pinout

17.8.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 61. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 kΩ resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

Table 62. Document Revision History (continued)

Rev. No.	Substantive Change(s)
1.2	Section 1.1.1—Updated feature list. Section 1.2.1.1—Updated notes for Table 1. Section 1.2.1.2—Removed 5-V PCI interface overshoot and undershoot figure. Section 1.2.1.3—Added this section to summarize impedance driver settings for various interfaces. Section 1.4—Updated rows in Reset Initialization timing specifications table. Added a table with DLL and PLL timing specifications. Section 1.5.2.2—Updated note 6 of DDR SDRAM Output AC Timing Specifications table. Section 1.7—Changed the minimum input low current from -600 to -15 μA for the RGMII DC electrical characteristics. Section 1.7.2—Changed LCS[3:4] to TSEC1_TXD[6:5]. Updated notes regarding LCS[3:4]. Section 1.13.2—Updated the mechanical dimensions diagram for the package. Section 1.13.3—Updated the notes for LBCTL, TRIG_OUT, and ASLEEP. Corrected pin assignments for IIC_SDA and IIC_SCL. Corrected reserved pin assignment of V11 to U11. V11 is actually $\overline{\text{PCI\_STOP}}$. Section 1.14.1—Updated the table for frequency options with respect to platform/CCB frequencies. Section 1.14.4—Edited Frequency options with respect to memory bus speeds.
1.1	Made updates throughout document. Section 1.6.1—Added symbols and note for the GTX_CLK125 timing parameters. Section 1.11.3—Updated pin list table: LGPL5/LSDAMUX to LGPL5, LA[27:29] and LA[30:31] to LA[27:31], TRST to $\overline{\text{TRST}}$, added GBE Clocking section and EC_GTX_CLK125 signal. Figure 50—Updated pin 2 connection information.
1	Original Customer Version.

19 Device Nomenclature

Ordering information for the parts fully covered by this specification document is provided in Section 19.1, "Part Numbers Fully Addressed by this Document."

19.1 Part Numbers Fully Addressed by this Document

Table 63 provides the Freescale part numbering nomenclature for the MPC8560. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 63. Part Numbering Nomenclature

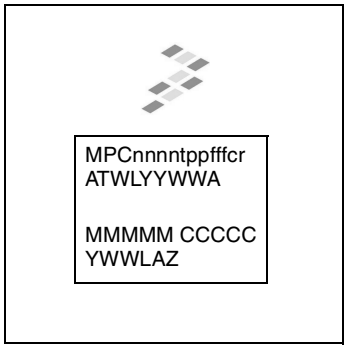
MPC	nnnn	t	pp	ff(f)	c	r
Product Code	**Part Identifier**	**Temperature Range [1]**	**Package [2]**	**Processor Frequency [3, 4]**	**Platform Frequency**	**Revision Level**
MPC	8560	Blank = 0 to 105°C C= -40 to 105°C	PX = FC-PBGA VT = FC-PBGA (Pb-free)	833 = 833 MHz 667 = 667 MHz	L = 333 MHz J= 266 MHz	B = Rev. 2.0 (SVR = 0x80700020) C = Rev. 2.1 (SVR = 0x80700021)
MPC	8560	Blank = 0 to 105°C C = –40 to 105°C	PX = FC-PBGA VT = FC-PBGA (Pb-free)	AQ = 1.0 GHz	F = 333 MHz	B = Rev. 2.0 (SVR = 0x80700020) C = Rev. 2.1 (SVR = 0x80700021)

Notes:

1. For Temperature Range=C, Processor Frequency is limited to 667 MHz.
2. See Section 14, "Package and Pin Listings" for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. The core must be clocked at a minimum frequency of 400 MHz. A device must not be used beyond the core frequency or platform frequency indicated on the device.
4. Designers should use the maximum power value corresponding to the core and platform frequency grades indicated on the device. A lower maximum power value should not be assumed for design purposes even when running at a lower frequency.

19.2 Part Marking

Parts are marked as the example shown in Figure 62.



FC-PBGA

Notes:

MMMMM is the 5-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.
YWWLAZ is the assembly traceability code.

Figure 62. Part Marking for FC-PBGA Device

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