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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 667MHz |
| Co-Processors/DSP | Communications; CPM |
| RAM Controllers | DDR, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | - |
| Voltage - I/O | 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 783-BFBGA, FCBGA |
| Supplier Device Package | 783-FCPBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8560cpx667jb |

# 3 Power Characteristics

The estimated power dissipation on the $V_{DD}$ supply for the MPC8560 is shown in Table 4.

**Table 4. MPC8560 $V_{DD}$ Power Dissipation [1,2]**

| CCB Frequency (MHz) | Core Frequency (MHz) | Typical Power[3,4] | Maximum Power[5] | Unit |
|---|---|---|---|---|
| 200 | 400 | 5.1 | 7.7 | W |
| | 500 | 5.4 | 8.0 | |
| | 600 | 5.8 | 8.4 | |
| 267 | 533 | 6.0 | 8.7 | W |
| | 667 | 6.4 | 9.2 | |
| | 800 | 6.9 | 10.7 | |
| 333 | 667 | 6.8 | 9.8 | W |
| | 833 | 7.4 | 11.4 | |
| | 1000 [6] | 11.9 | 16.5 | |

**Notes:**

1. The values do not include I/O supply power ($OV_{DD}$, $LV_{DD}$, $GV_{DD}$) or $AV_{DD}$.
2. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, air flow, power dissipation of other components on the board, and board thermal resistance. Any customer design must take these considerations into account to ensure the maximum 105 °C junction temperature is not exceeded on this device.
3. Typical Power is based on a nominal voltage of $V_{DD}$ = 1.2 V, a nominal process, a junction temperature of $T_j$ = 105 °C, and a Dhrystone 2.1 benchmark application.
4. Thermal solutions will likely need to design to a number higher than Typical Power based on the end application, $T_A$ target, and I/O power.
5. Maximum power is based on a nominal voltage of $V_{DD}$ = 1.2 V, worst case process, a junction temperature of $T_j$ = 105 °C, and an artificial smoke test.
6. The nominal recommended $V_{DD}$ is 1.3 V for this speed grade.

The estimated power dissipation on the $AV_{DD}$ supplies for the MPC8560 PLLs is shown in Table 5.

**Table 5. MPC8560 $AV_{DD}$ Power Dissipation**

| $AV_{DD}n$ | Typical[1] | Unit |
|---|---|---|
| $AV_{DD}1$ | 0.007 | W |
| $AV_{DD}2$ | 0.014 | W |
| $AV_{DD}3$ | 0.004 | W |

**Notes:**

1. $V_{DD}$ = 1.2 V(1.3 V for 1.0 GHz device), $T_J$ = 105°C

Figure 6 shows the DDR SDRAM output timing diagram.

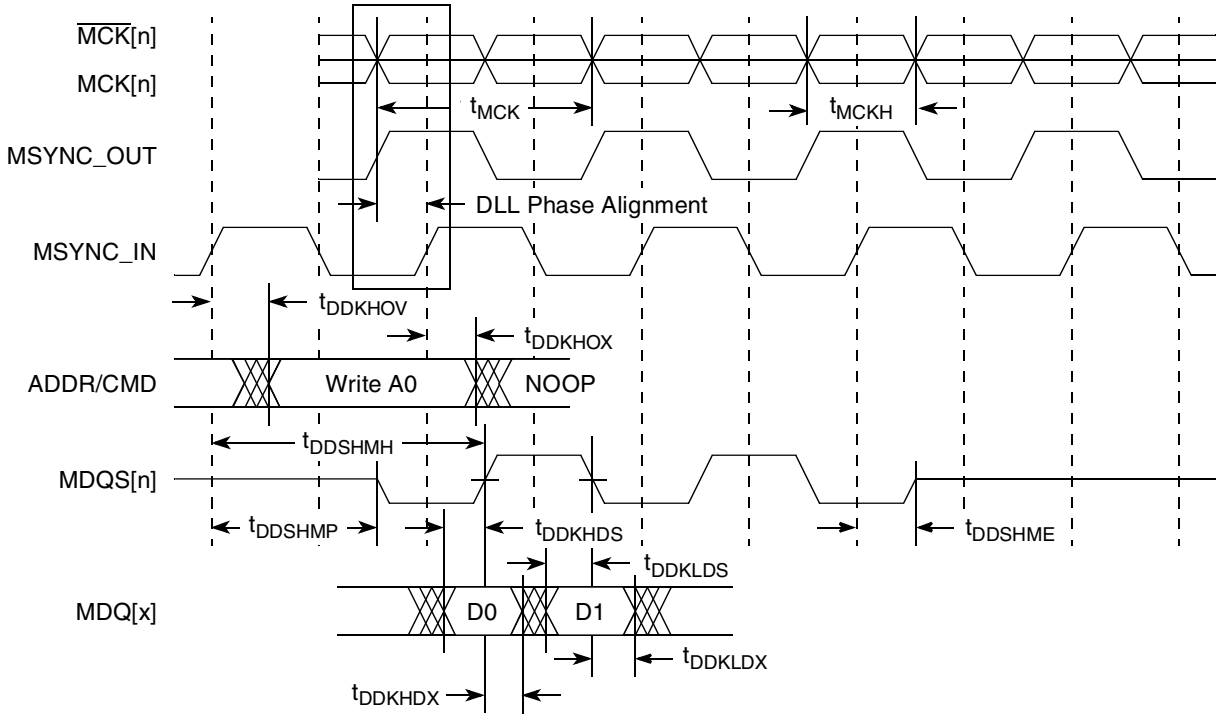



**Figure 6. DDR SDRAM Output Timing Diagram**

### 6.2.2.2 Load Effects on Address/Command Bus

Table 18 provides approximate delay information that can be expected for the address and command signals of the DDR controller for various loadings. These numbers are the result of simulations for one topology. The delay numbers will strongly depend on the topology used. These delay numbers show the total delay for the address and command to arrive at the DRAM devices. The actual delay could be different than the delays seen in simulation, depending on the system topology. If a heavily loaded system is used, the DLL loop may need to be adjusted to meet setup requirements at the DRAM.

**Table 18. Expected Delays for Address/Command**

| Load | Delay | Unit |
|---|---|---|
| 4 devices (12 pF) | 3.0 | ns |
| 9 devices (27 pF) | 3.6 | ns |
| 36 devices (108 pF) + 40 pF compensation capacitor | 5.0 | ns |
| 36 devices (108 pF) + 80 pF compensation capacitor | 5.2 | ns |

# 7 Ethernet: Three-Speed, MII Management

This section provides the AC and DC electrical characteristics for three-speed and MII management.

## 7.1 Three-Speed Ethernet Controller (TSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII, MII, and TBI interfaces can be operated at 3.3 or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with the IEEE 802.3 standard. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 7.3, "Ethernet Management Interface Electrical Characteristics."

### 7.1.1 TSEC DC Electrical Characteristics

All GMII,MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 19 and Table 20. The potential applied to the input of a GMII,MII, TBI, RGMII, or RTBI receiver may exceed the potential of the receiver's power supply (i.e., a GMII driver powered from a 3.6 V supply driving $V_{OH}$ into a GMII receiver powered from a 2.5 V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5 V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

**Table 19. GMII, MII, and TBI DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage 3.3 V | $LV_{DD}$ | 3.13 | 3.47 | V |
| Output high voltage ($LV_{DD}$ = Min, $I_{OH}$ = –4.0 mA) | $V_{OH}$ | 2.40 | $LV_{DD}$ + 0.3 | V |
| Output low voltage ($LV_{DD}$ = Min, $I_{OL}$ = 4.0 mA) | $V_{OL}$ | GND | 0.50 | V |
| Input high voltage | $V_{IH}$ | 1.70 | $LV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | –0.3 | 0.90 | V |
| Input high current ($V_{IN}$ [1] = $LV_{DD}$) | $I_{IH}$ | — | 40 | μA |
| Input low current ($V_{IN}$ [1] = GND) | $I_{IL}$ | –600 | — | μA |

**Note:**
1.The symbol $V_{IN}$, in this case, represents the $LV_{IN}$ symbol referenced in Table 1 and Table 2.

**Table 21. GMII Transmit AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}$ of 3.3 V ± 5%, or $LV_{DD}$=2.5V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| GTX_CLK data clock rise and fall time | $t_{GTXR}$, $t_{GTXF}$ [2,4] | — | — | 1.0 | ns |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{GTKHDV}$ symbolizes GMII transmit timing (GT) with respect to the $t_{GTX}$ clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, $t_{GTKHDX}$ symbolizes GMII transmit timing (GT) with respect to the $t_{GTX}$ clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{GTX}$ represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by characterization.
4. Guaranteed by design.

Figure 7 shows the GMII transmit AC timing diagram.

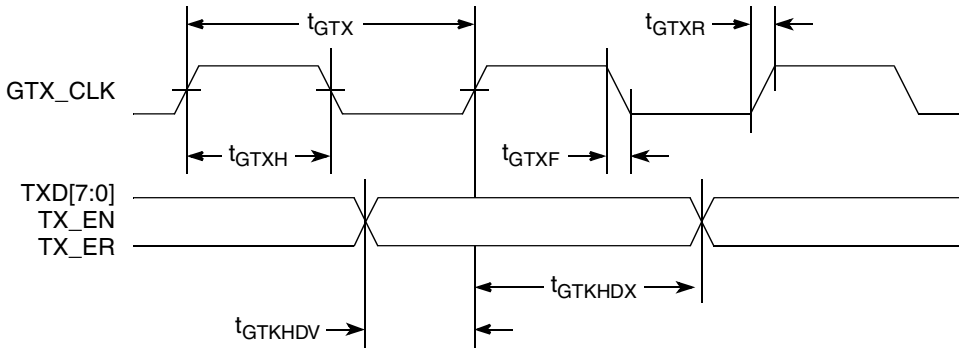



**Figure 7. GMII Transmit AC Timing Diagram**

### 7.2.1.2 GMII Receive AC Timing Specifications

Table 22 provides the GMII receive AC timing specifications.

**Table 22. GMII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ of 3.3 V ± 5%, or $LV_{DD}$=2.5V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period | $t_{GRX}$ | — | 8.0 | — | ns |
| RX_CLK duty cycle | $t_{GRXH}/t_{GRX}$ | 40 | — | 60 | ns |
| RXD[7:0], RX_DV, RX_ER setup time to RX_CLK | $t_{GRDVKH}$ | 2.0 | — | — | ns |
| RXD[7:0], RX_DV, RX_ER hold time to RX_CLK | $t_{GRDXKH}$ | 0.5 | — | — | ns |

### 7.2.4 RGMII and RTBI AC Timing Specifications

Table 27 presents the RGMII and RTBI AC timing specifications.

**Table 27. RGMII and RTBI AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ of 2.5 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Data to clock output skew (at transmitter) | $t_{SKRGT}$ [5] | –500 | 0 | 500 | ps |
| Data to clock input skew (at receiver) [2] | $t_{SKRGT}$ | 1.0 | — | 2.8 | ns |
| Clock period[3] | $t_{RGT}$ [6] | 7.2 | 8.0 | 8.8 | ns |
| Duty cycle for 1000Base-T [4] | $t_{RGTH}/t_{RGT}$ [6] | 45 | 50 | 55 | % |
| Duty cycle for 10BASE-T and 100BASE-TX [3] | $t_{RGTH}/t_{RGT}$ [6] | 40 | 50 | 60 | % |
| Rise and fall time | $t_{RGTR}$, $t_{RGTF}$ [6,7] | — | — | 0.75 | ns |

**Notes:**

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of $t_{RGT}$ represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. The RGMII specification requires that PC board designer add 1.5 ns or greater in trace delay to the RX_CLK in order to meet this specification. However, as stated above, this device will function with only 1.0 ns of delay.
3. For 10 and 100 Mbps, $t_{RGT}$ scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three $t_{RGT}$ of the lowest speed transitioned between.
5. Guaranteed by characterization.
6. Guaranteed by design.
7. Signal timings are measured at 0.5 V and 2.0 V voltage levels.

**Table 31. Local Bus General Timing Parameters—DLL Enabled (continued)**

| Parameter | POR Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Input setup to local bus clock (except LUPWAIT) | — | $t_{LBIVKH1}$ | 1.8 | — | ns | 4, 5, 8 |
| LUPWAIT input setup to local bus clock | — | $t_{LBIVKH2}$ | 1.7 | — | ns | 4, 5 |
| Input hold from local bus clock (except LUPWAIT) | — | $t_{LBIXKH1}$ | 0.5 | — | ns | 4, 5, 8 |
| LUPWAIT input hold from local bus clock | — | $t_{LBIXKH2}$ | 1.0 | — | ns | 4, 5 |
| LALE output transition to LAD/LDP output transition (LATCH hold time) | — | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | TSEC2_TXD[6:5] = 00 | $t_{LBKHOV1}$ | — | 2.0 | ns | 4, 8 |
| | TSEC2_TXD[6:5] = 11 (default) | | | 3.5 | | |
| Local bus clock to data valid for LAD/LDP | TSEC2_TXD[6:5] = 00 | $t_{LBKHOV2}$ | — | 2.2 | ns | 4, 8 |
| | TSEC2_TXD[6:5] = 11 (default) | | | 3.7 | | |
| Local bus clock to address valid for LAD | TSEC2_TXD[6:5] = 00 | $t_{LBKHOV3}$ | — | 2.3 | ns | 4, 8 |
| | TSEC2_TXD[6:5] = 11 (default) | | | 3.8 | | |
| Local bus clock to LALE assertion | | $t_{LBKHOV4}$ | — | 2.3 | ns | 4, 8 |
| Output hold from local bus clock (except LAD/LDP and LALE) | TSEC2_TXD[6:5] = 00 | $t_{LBKHOX1}$ | 0.7 | — | ns | 4, 8 |
| | TSEC2_TXD[6:5] = 11 (default) | | 1.6 | | | |
| Output hold from local bus clock for LAD/LDP | TSEC2_TXD[6:5] = 00 | $t_{LBKHOX2}$ | 0.7 | — | ns | 4, 8 |
| | TSEC2_TXD[6:5] = 11 (default) | | 1.6 | | | |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | TSEC2_TXD[6:5] = 00 | $t_{LBKHOZ1}$ | — | 2.5 | ns | 7, 9 |
| | TSEC2_TXD[6:5] = 11 (default) | | | 3.8 | | |

Figure 16 provides the AC test load for the local bus.

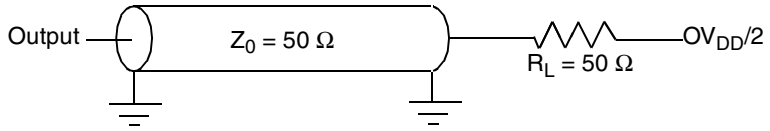



**Figure 16. Local Bus AC Test Load**

Figure 17 through Figure 22 show the local bus signals.

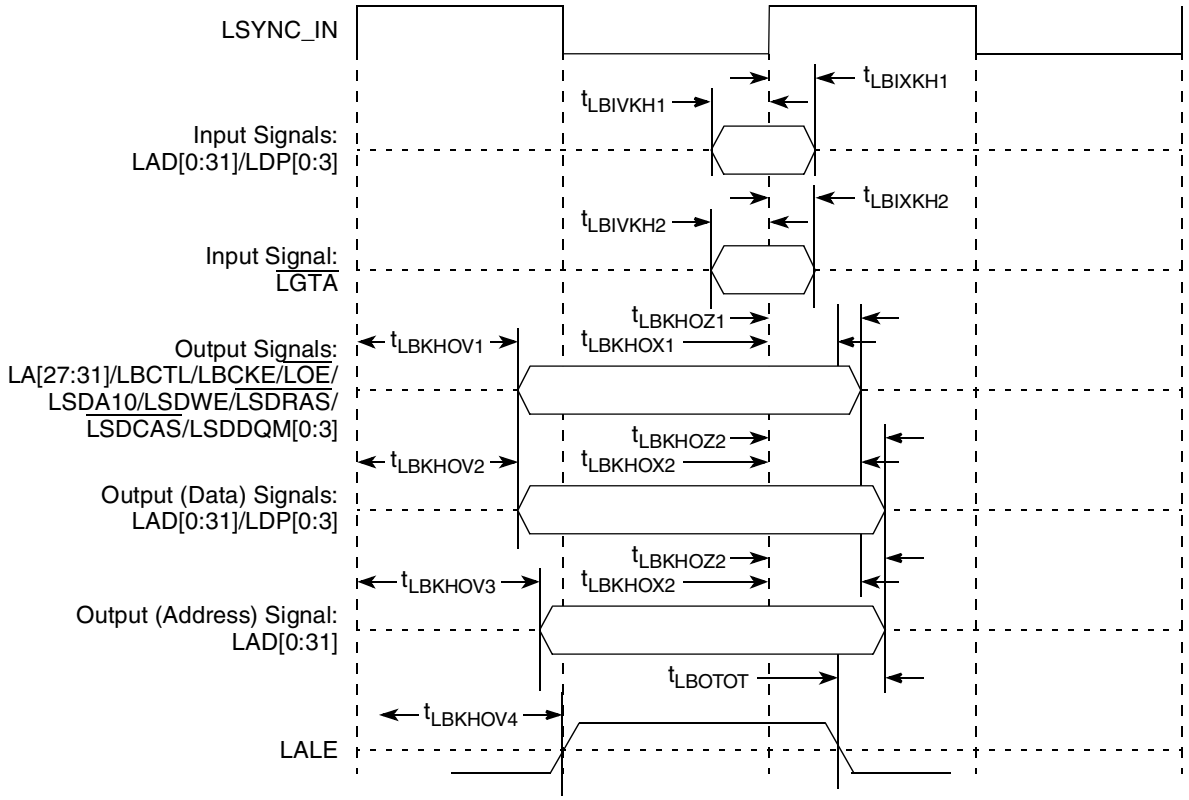



**Figure 17. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)**

# 10 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8560.

Table 39 provides the JTAG AC timing specifications as defined in Figure 32 through Figure 35.

**Table 39. JTAG AC Timing Specifications (Independent of SYSCLK) [1]**

At recommended operating conditions (see Table 2).

| Parameter | Symbol [2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | — |
| JTAG external clock pulse width measured at 1.4 V | $t_{JTKHKL}$ | 15 | — | ns | — |
| JTAG external clock rise and fall times | $t_{JTGR}$ & $t_{JTGF}$ | 0 | 2 | ns | 6 |
| $\overline{\text{TRST}}$ assert time | $t_{TRST}$ | 25 | — | ns | 3 |
| Input setup times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDVKH}$<br>$t_{JTIVKH}$ | <br>4<br>0 | <br>—<br>— | ns | 4 |
| Input hold times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDXKH}$<br>$t_{JTIXKH}$ | <br>20<br>25 | <br>—<br>— | ns | 4 |
| Valid times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDV}$<br>$t_{JTKLOV}$ | <br>4<br>4 | <br>20<br>25 | ns | 5 |
| Output hold times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDX}$<br>$t_{JTKLOX}$ | | — | ns | 5 |
| JTAG external clock to output high impedance:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDZ}$<br>$t_{JTKLOZ}$ | <br>3<br>3 | <br>19<br>9 | ns | 5, 6 |

**Notes:**

1. All outputs are measured from the midpoint voltage of the falling/rising edge of $t_{TCLK}$ to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 31). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to $t_{TCLK}$.
5. Non-JTAG signal output timing with respect to $t_{TCLK}$.
6. Guaranteed by design.

**Table 45. PCI-X AC Timing Specifications at 133 MHz (continued)**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time | $t_{PCRHIX}$ | 0 | 50 | ns | 6, 12 |

**Notes:**

1. See the timing measurement conditions in the *PCI-X 1.0a Specification*.
2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
3. Setup time for point-to-point signals applies to $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ only. All other signals are bused.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
6. Maximum value is also limited by delay to the first transaction (time for $\overline{\text{HRESET}}$ high to first configuration access, $t_{PCRHFV}$). The PCI-X initialization pattern control signals after the rising edge of $\overline{\text{HRESET}}$ must be negated no later than two clocks before the first $\overline{\text{FRAME}}$ and must be floated no later than one clock before $\overline{\text{FRAME}}$ is asserted.
7. A PCI-X device is permitted to have the minimum values shown for $t_{PCKHOV}$ and $t_{CYC}$ only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
8. Device must meet this specification independent of how many outputs switch simultaneously.
9. The timing parameter $t_{PCIVKH}$ is a minimum of 1.4 ns rather than the minimum of 1.2 ns in the *PCI-X 1.0a Specification.*
10. The timing parameter $t_{PCRHFV}$ is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*
11. Guaranteed by characterization.
12. Guaranteed by design.

# 13 RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8560.

## 13.1 RapidIO DC Electrical Characteristics

RapidIO driver and receiver DC electrical characteristics are provided in Table 46 and Table 47, respectively.

**Table 46. RapidIO 8/16 LP-LVDS Driver DC Electrical Characteristics**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 5%.

| Characteristic | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Differential output high voltage | $V_{OHD}$ | 247 | 454 | mV | 1, 2 |
| Differential output low voltage | $V_{OLD}$ | –454 | –247 | mV | 1, 2 |
| Differential offset voltage | $\Delta V_{OSD}$ | — | 50 | mV | 1,3 |
| Output high common mode voltage | $V_{OHCM}$ | 1.125 | 1.375 | V | 1, 4 |
| Output low common mode voltage | $V_{OLCM}$ | 1.125 | 1.375 | V | 1, 5 |

The eye pattern for a data signal is generated by making a large number of recordings of the signal and then overlaying the recordings. The number of recordings used to generate the eye shall be large enough that further increasing the number of recordings used does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not. Each data signal in the interface shall be carrying random or pseudo-random data when the recordings are made. If pseudo-random data is used, the length of the pseudo-random sequence (repeat length) shall be long enough that increasing the length of the sequence does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not comply with the mask. The data carried by any given data signal in the interface may not be correlated with the data carried by any other data signal in the interface. The zero-crossings of the clock associated with a data signal shall be used as the timing reference for aligning the multiple recordings of the data signal when the recordings are overlaid.

While the method used to make the recordings and overlay them to form the eye pattern is not specified, the method used shall be demonstrably equivalent to the following method. The signal under test is repeatedly recorded with a digital oscilloscope in infinite persistence mode. Each recording is triggered by a zero-crossing of the clock associated with the data signal under test. Roughly half of the recordings are triggered by positive-going clock zero-crossings and roughly half are triggered by negative-going clock zero-crossings. Each recording is at least 1.9 UI in length (to ensure that at least one complete eye is formed) and begins 0.5 UI before the trigger point (0.5 UI before the associated clock zero-crossing). Depending on the length of the individual recordings used to generate the eye pattern, one or more complete eyes will be formed. Regardless of the number of eyes, the eye whose center is immediately to the right of the trigger point is the eye used for compliance testing.

An example of an eye pattern generated using the above method with recordings 3 UI in length is shown in Figure 45. In this example, there is no skew between the signal under test and the associated clock used to trigger the recordings. If skew was present, the eye pattern would be shifted to the left or right relative to the oscilloscope trigger point.

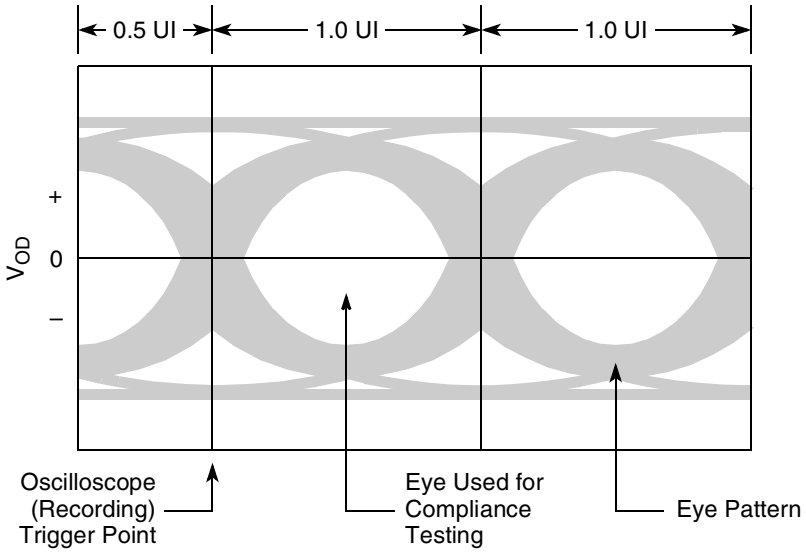



**Figure 45. Example Driver Output Eye Pattern**

3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
7. The socket lid must always be oriented to A1.

## 14.3 Pinout Listings

Table 54 provides the pin-out listing for the MPC8560, 783 FC-PBGA package.

**Table 54. MPC8560 Pinout Listing**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **PCI/PCI-X** | | | | |
| PCI_AD[63:0] | AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14, V15, W15, Y15, AA15, AB15, AC15, AD15, AG15, AH15, V16, W16, AB16, AC16, AD16, AE16, AF16, V17, W17, Y17, AA17, AB17, AE17, AF17, AF18, AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9, AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11, AG11, AH11, V12, W12, Y12, AB12, AD12, AE12, AG12, AH12, V13, Y13, AB13, AC13 | I/O | $OV_{DD}$ | 17 |
| PCI_C_$\overline{BE}$[7:0] | AG13, AH13, V14, W14, AH8, AB10, AD11, AC12 | I/O | $OV_{DD}$ | 17 |
| PCI_PAR | AA11 | I/O | $OV_{DD}$ | — |
| PCI_PAR64 | Y14 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI\_FRAME}}$ | AC10 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI\_TRDY}}$ | AG10 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI\_IRDY}}$ | AD10 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI\_STOP}}$ | V11 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI\_DEVSEL}}$ | AH10 | I/O | $OV_{DD}$ | 2 |
| PCI_IDSEL | AA9 | I | $OV_{DD}$ | — |
| $\overline{\text{PCI\_REQ64}}$ | AE13 | I/O | $OV_{DD}$ | 5, 10 |
| $\overline{\text{PCI\_ACK64}}$ | AD13 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI\_PERR}}$ | W11 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI\_SERR}}$ | Y11 | I/O | $OV_{DD}$ | 2, 4 |
| $\overline{\text{PCI\_REQ0}}$ | AF5 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI\_REQ}}$[1:4] | AF3, AE4, AG4, AE5 | I | $OV_{DD}$ | — |
| $\overline{\text{PCI\_GNT}}$[0] | AE6 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI\_GNT}}$[1:4] | AG5, AH5, AF6, AG6 | O | $OV_{DD}$ | 5, 9 |

**Table 54. MPC8560 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **DDR SDRAM Memory Interface** | | | | |
| MDQ[0:63] | M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12 | I/O | $GV_{DD}$ | — |
| MECC[0:7] | N20, M20, L19, E19, C21, A21, G19, A19 | I/O | $GV_{DD}$ | — |
| MDM[0:8] | L24, H28, F24, L21, E18, E16, G14, B13, M19 | O | $GV_{DD}$ | — |
| MDQS[0:8] | L26, J25, D25, A22, H18, F16, F14, C13, C20 | I/O | $GV_{DD}$ | — |
| MBA[0:1] | B18, B19 | O | $GV_{DD}$ | — |
| MA[0:14] | N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13 | O | $GV_{DD}$ | — |
| $\overline{\text{MWE}}$ | D17 | O | $GV_{DD}$ | — |
| $\overline{\text{MRAS}}$ | F17 | O | $GV_{DD}$ | — |
| $\overline{\text{MCAS}}$ | J16 | O | $GV_{DD}$ | — |
| $\overline{\text{MCS}}$[0:3] | H16, G16, J15, H15 | O | $GV_{DD}$ | — |
| MCKE[0:1] | E26, E28 | O | $GV_{DD}$ | 11 |
| MCK[0:5] | J20, H25, A15, D20, F28, K14 | O | $GV_{DD}$ | — |
| $\overline{\text{MCK}}$[0:5] | F20, G27, B15, E20, F27, L14 | O | $GV_{DD}$ | — |
| MSYNC_IN | M28 | I | $GV_{DD}$ | — |
| MSYNC_OUT | N28 | O | $GV_{DD}$ | — |
| **Local Bus Controller Interface** | | | | |
| LA[27] | U18 | O | $OV_{DD}$ | 5, 9 |
| LA[28:31] | T18, T19, T20, T21 | O | $OV_{DD}$ | 7, 9 |
| LAD[0:31] | AD26, AD27, AD28, AC26, AC27, AC28, AA22, AA23, AA26, Y21, Y22, Y26, W20, W22, W26, V19, T22, R24, R23, R22, R21, R18, P26, P25, P20, P19, P18, N22, N23, N24, N25, N26 | I/O | $OV_{DD}$ | — |
| LALE | V21 | O | $OV_{DD}$ | 8, 9 |
| LBCTL | V20 | O | $OV_{DD}$ | 9 |
| LCKE | U23 | O | $OV_{DD}$ | — |
| LCLK[0:2] | U27, U28, V18 | O | $OV_{DD}$ | — |
| $\overline{\text{LCS}}$[0:4] | Y27, Y28, W27, W28, R27 | O | $OV_{DD}$ | 18 |
| $\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$ | R28 | I/O | $OV_{DD}$ | 1 |

**Table 54. MPC8560 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **Gigabit Reference Clock** | | | | |
| EC_GTX_CLK125 | E2 | I | $LV_{DD}$ | — |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 1)** | | | | |
| TSEC1_TXD[7:4] | A6, F7, D7, C7 | O | $LV_{DD}$ | 5, 9 |
| TSEC1_TXD[3:0] | B7, A7, G8, E8 | O | $LV_{DD}$ | 9, 19 |
| TSEC1_TX_EN | C8 | O | $LV_{DD}$ | 11 |
| TSEC1_TX_ER | B8 | O | $LV_{DD}$ | — |
| TSEC1_TX_CLK | C6 | I | $LV_{DD}$ | — |
| TSEC1_GTX_CLK | B6 | O | $LV_{DD}$ | 18 |
| TSEC1_CRS | C3 | I | $LV_{DD}$ | — |
| TSEC1_COL | G7 | I | $LV_{DD}$ | — |
| TSEC1_RXD[7:0] | D4, B4, D3, D5, B5, A5, F6, E6 | I | $LV_{DD}$ | — |
| TSEC1_RX_DV | D2 | I | $LV_{DD}$ | — |
| TSEC1_RX_ER | E5 | I | $LV_{DD}$ | — |
| TSEC1_RX_CLK | D6 | I | $LV_{DD}$ | — |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 2)** | | | | |
| TSEC2_TXD[7:2] | B10, A10, J10, K11,J11, H11 | O | $LV_{DD}$ | 5, 9 |
| TSEC2_TXD[1:0] | G11, E11 | O | $LV_{DD}$ | — |
| TSEC2_TX_EN | B11 | O | $LV_{DD}$ | 11 |
| TSEC2_TX_ER | D11 | O | $LV_{DD}$ | — |
| TSEC2_TX_CLK | D10 | I | $LV_{DD}$ | — |
| TSEC2_GTX_CLK | C10 | O | $LV_{DD}$ | 18 |
| TSEC2_CRS | D9 | I | $LV_{DD}$ | — |
| TSEC2_COL | F8 | I | $LV_{DD}$ | — |
| TSEC2_RXD[7:0] | F9, E9, C9, B9, A9, H9, G10, F10 | I | $LV_{DD}$ | — |
| TSEC2_RX_DV | H8 | I | $LV_{DD}$ | — |
| TSEC2_RX_ER | A8 | I | $LV_{DD}$ | — |
| TSEC2_RX_CLK | E10 | I | $LV_{DD}$ | — |
| **RapidIO Interface** | | | | |
| RIO_RCLK | Y25 | I | $OV_{DD}$ | — |
| $\overline{\text{RIO\_RCLK}}$ | Y24 | I | $OV_{DD}$ | — |

**Table 54. MPC8560 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $LV_{DD}$ | A4, C5, E7, H10 | Reference Voltage; Three-Speed Ethernet I/O (2.5 V, 3.3 V) | $LV_{DD}$ | — |
| $MV_{REF}$ | N27 | Reference Voltage Signal; DDR | $MV_{REF}$ | — |
| No Connects | AH26, AH27, AH28, AG28, AF28, AE28, AH1, AG1, AH2, B1, B2, A2, A3, AH25 | — | — | 16 |
| $OV_{DD}$ | D1, E4, H3, K4, K10, L7, M5, N3, P22, R19, R25, T2, T7, U5, U20, U26, V8, W4, W13, W19, W21, Y7, Y23, AA5, AA12, AA16, AA20, AB7, AB9, AB26, AC5, AC11, AC17, AD4, AE1, AE8, AE10, AE15, AF7, AF12, AG27, AH4 | PCI/PCI-X, RapidIO, 10/100 Ethernet, and other Standard (3.3 V) | $OV_{DD}$ | — |
| RESERVED | C1, T11, U11, AF1 | — | — | 15 |
| SENSEVDD | L12 | Power for Core (1.2 V) | $V_{DD}$ | 13 |
| SENSEVSS | K12 | — | — | 13 |
| $V_{DD}$ | M13, M15, M17, N14, N16, P13, P15, P17, R12, R14, R16, T13, T15, T17, U12, U14 | Power for Core (1.2 V) | $V_{DD}$ | — |
| **CPM** | | | | |
| PA[0:31] | H1, H2, J1, J2, J3, J4, J5, J6, J7, J8, K8, K7, K6, K3, K2, K1, L1, L2, L3, L4, L5, L8, L9, L10, L11, M10, M9, M8, M7, M6, M3, M2 | I/0 | $OV_{DD}$ | — |
| PB[4:31] | M1, N1, N4, N5, N6, N7, N8, N9, N10, N11, P11, P10, P9, P8, P7, P6, P5, P4, P3, P2, P1, R1, R2, R3, R4, R5, R6, R7 | I/0 | $OV_{DD}$ | — |
| PC[0:31] | R8, R9, R10, R11, T9, T6, T5, T4, T1, U1, U2, U3, U4, U7, U8, U9, U10, V9, V6, V5, V4, V3, V2, V1, W1, W2, W3, W6, W7, W8, W9, Y9 | I/0 | $OV_{DD}$ | — |

## 15.2 Platform/System PLL Ratio

The platform clock is the clock that drives the L2 cache, the DDR SDRAM data rate, and the e500 core complex bus (CCB), and is also called the CCB clock. The values are determined by the binary value on LA[28:31] at power up, as shown in Table 57.

There is no default for this PLL ratio; these signals must be pulled to the desired values.

**Table 57. CCB Clock Ratio**

| Binary Value of LA[28:31] Signals | Ratio Description |
|---|---|
| 0000 | 16:1 ratio CCB clock: SYSCLK (PCI bus) |
| 0001 | Reserved |
| 0010 | 2:1 ratio CCB clock: SYSCLK (PCI bus) |
| 0011 | 3:1 ratio CCB clock: SYSCLK (PCI bus) |
| 0100 | 4:1 ratio CCB clock: SYSCLK (PCI bus) |
| 0101 | 5:1 ratio CCB clock: SYSCLK (PCI bus) |
| 0110 | 6:1 ratio CCB clock: SYSCLK (PCI bus) |
| 0111 | Reserved |
| 1000 | 8:1 ratio CCB clock: SYSCLK (PCI bus) |
| 1001 | 9:1 ratio CCB clock: SYSCLK (PCI bus) |
| 1010 | 10:1 ratio CCB clock: SYSCLK (PCI bus) |
| 1011 | Reserved |
| 1100 | 12:1 ratio CCB clock: SYSCLK (PCI bus) |
| 1101 | Reserved |
| 1110 | Reserved |
| 1111 | Reserved |

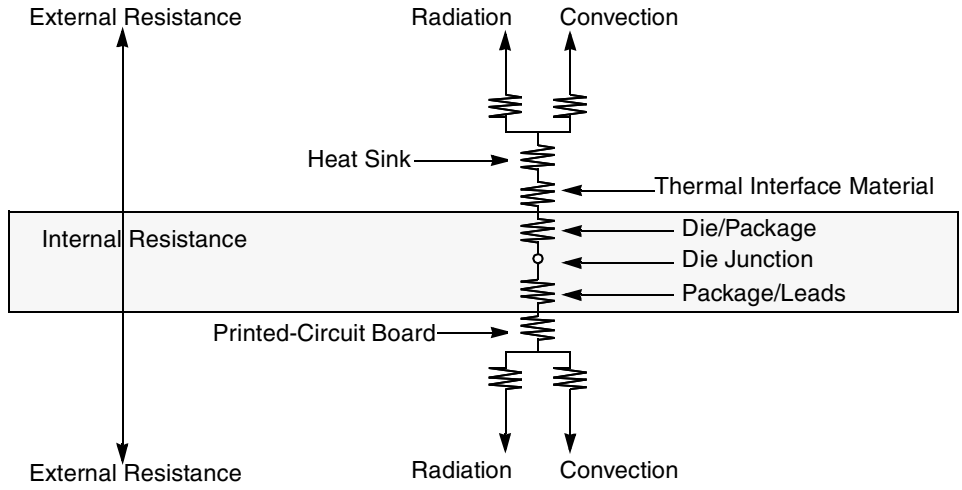
## 15.3 e500 Core PLL Ratio

Table 58 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LALE and LGPL2 at power up, as shown in Table 58.

**Table 58. e500 Core to CCB Ratio**

| Binary Value of LALE, LGPL2 Signals | Ratio Description |
|---|---|
| 00 | 2:1 e500 core:CCB |
| 01 | 5:2 e500 core:CCB |
| 10 | 3:1 e500 core:CCB |
| 11 | 7:2 e500 core:CCB |

Figure 53 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.




(Note the internal versus external package resistance)

**Figure 53. Package with Heat Sink Mounted to a Printed-Circuit Board**

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

## 16.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 54 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 51). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink, the heat sink should be slowly removed. Heating the heat sink to 40-50°C with an air gun can soften the interface material and make the removal easier. The use of an adhesive for heat sink attach is not recommended.

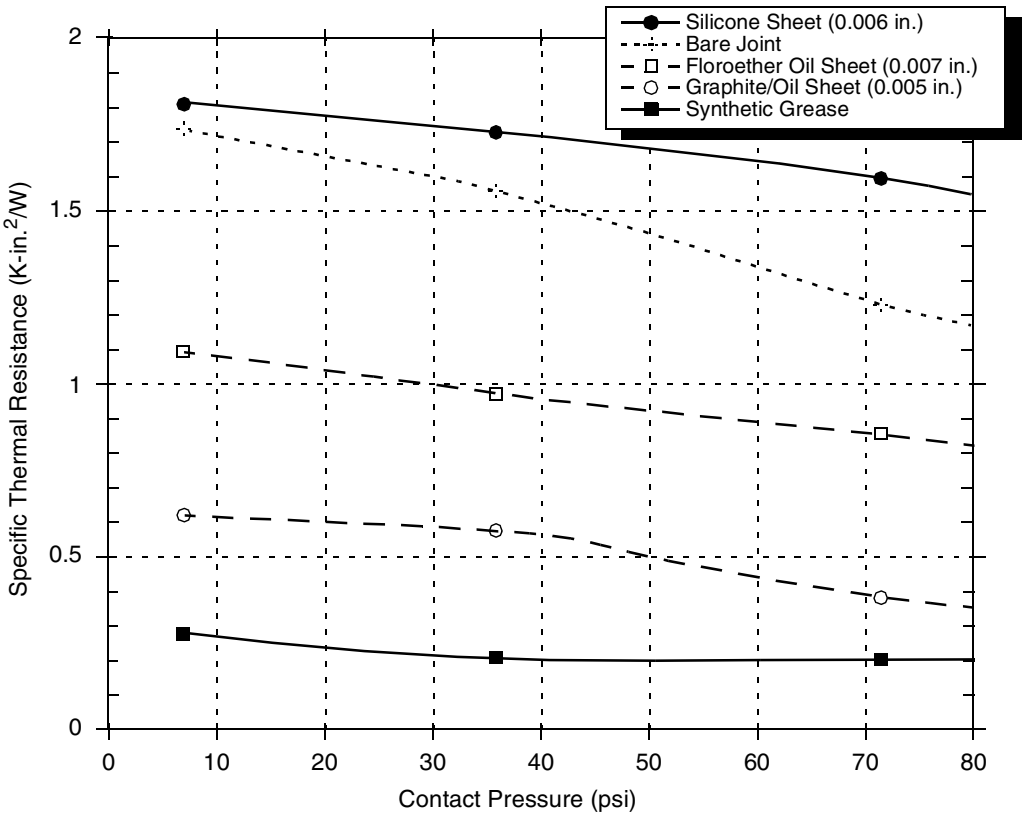



**Figure 54. Thermal Performance of Select Thermal Interface Materials**

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

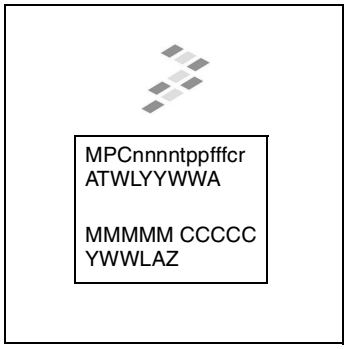
| | |
|---|---|
| Chomerics, Inc.<br>77 Dragon Ct.<br>Woburn, MA 01888-4014<br>Internet: www.chomerics.com | 781-935-4850 |
| Dow-Corning Corporation<br>Dow-Corning Electronic Materials<br>2200 W. Salzburg Rd.<br>Midland, MI 48686-0997<br>Internet: www.dowcorning.com | 800-248-2481 |
| Shin-Etsu MicroSi, Inc.<br>10028 S. 51st St.<br>Phoenix, AZ 85044<br>Internet: www.microsi.com | 888-642-7674 |
| The Bergquist Company<br>18930 West 78th St.<br>Chanhassen, MN 55317<br>Internet: www.bergquistcompany.com | 800-347-4572 |

**Table 62. Document Revision History (continued)**

| Rev. No. | Substantive Change(s) |
|---|---|
| 1.2 | Section 1.1.1—Updated feature list.<br>Section 1.2.1.1—Updated notes for Table 1.<br>Section 1.2.1.2—Removed 5-V PCI interface overshoot and undershoot figure.<br>Section 1.2.1.3—Added this section to summarize impedance driver settings for various interfaces.<br>Section 1.4—Updated rows in Reset Initialization timing specifications table. Added a table with DLL and PLL timing specifications.<br>Section 1.5.2.2—Updated note 6 of DDR SDRAM Output AC Timing Specifications table.<br>Section 1.7—Changed the minimum input low current from -600 to -15 μA for the RGMII DC electrical characteristics.<br>Section 1.7.2—Changed LCS[3:4] to TSEC1_TXD[6:5]. Updated notes regarding LCS[3:4].<br>Section 1.13.2—Updated the mechanical dimensions diagram for the package.<br>Section 1.13.3—Updated the notes for LBCTL, TRIG_OUT, and ASLEEP. Corrected pin assignments for IIC_SDA and IIC_SCL. Corrected reserved pin assignment of V11 to U11. V11 is actually $\overline{\text{PCI\_STOP}}$.<br>Section 1.14.1—Updated the table for frequency options with respect to platform/CCB frequencies.<br>Section 1.14.4—Edited Frequency options with respect to memory bus speeds. |
| 1.1 | Made updates throughout document.<br>Section 1.6.1—Added symbols and note for the GTX_CLK125 timing parameters.<br>Section 1.11.3—Updated pin list table: LGPL5/LSDAMUX to LGPL5, LA[27:29] and LA[30:31] to LA[27:31], TRST to $\overline{\text{TRST}}$, added GBE Clocking section and EC_GTX_CLK125 signal.<br>Figure 50—Updated pin 2 connection information. |
| 1 | Original Customer Version. |

## 19.2 Part Marking

Parts are marked as the example shown in Figure 62.




FC-PBGA

**Notes:**

MMMMM is the 5-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.
YWWLAZ is the assembly traceability code.

**Figure 62. Part Marking for FC-PBGA Device**

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