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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8560cpx667jc

1 Overview

The following section provides a high-level overview of the MPC8560 features. Figure 1 shows the major functional units within the MPC8560.

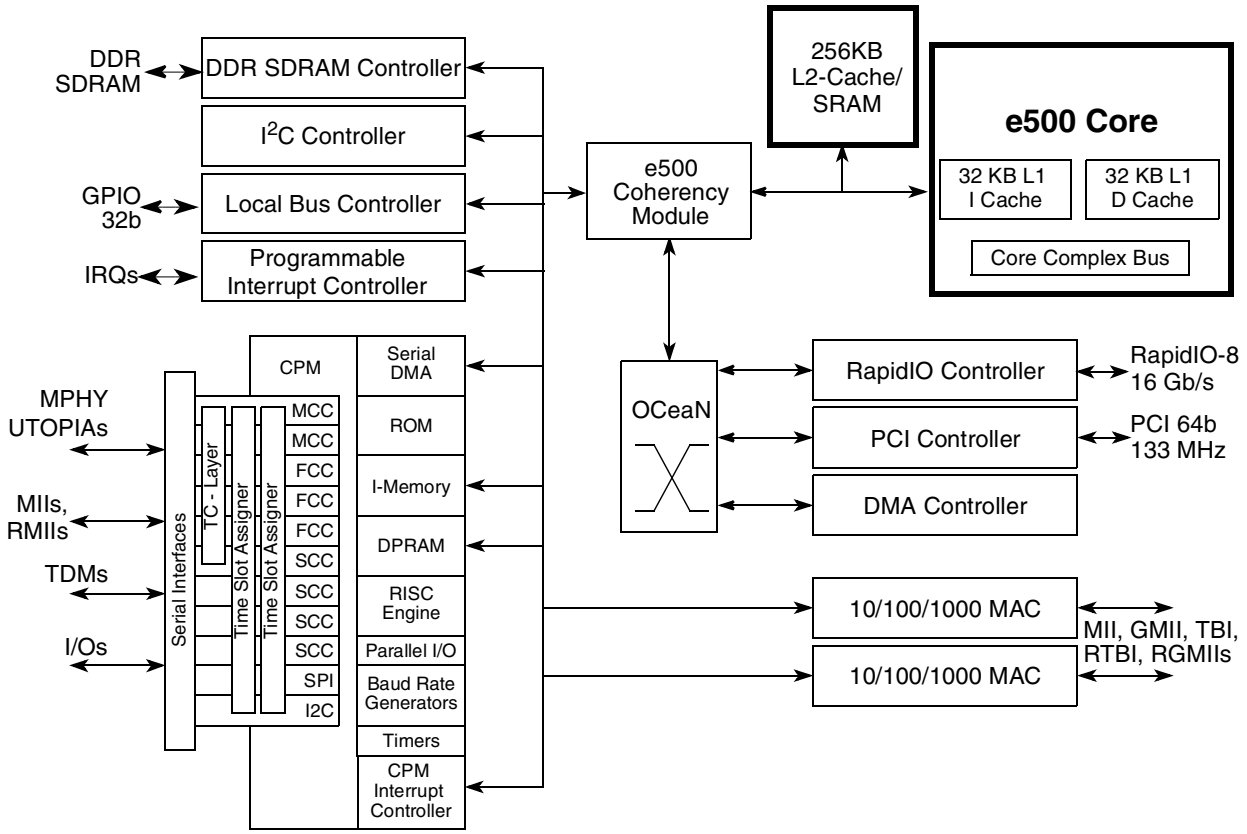

Figure 1. MPC8560 Block Diagram

1.1 Key Features

The following lists an overview of the MPC8560 feature set.

- High-performance, 32-bit Book E–enhanced core that implements the Power Architecture
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis. Separate locking for instructions and data
  - Memory management unit (MMU) especially designed for embedded applications
  - Enhanced hardware and software debug support
  - Performance monitor facility (similar to but different from the MPC8560 performance monitor described in Chapter 18, “Performance Monitor.”
- High-performance RISC CPM operating at up to 333 MHz
  - CPM software compatibility with previous PowerQUICC families
  - One instruction per clock

Table 6 provides estimated I/O power numbers for each block: DDR, PCI, Local Bus, RapidIO, TSEC, and CPM.

Table 6. Estimated Typical I/O Power Consumption

Interface	Parameter	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Units	Notes
DDR I/O	CCB = 200 MHz	0.46	—	—	—	W	1
	CCB = 266 MHz	0.59	—	—	—		
	CCB = 300 MHz	0.66	—	—	—		
	CCB = 333 MHz	0.73	—	—	—		
PCI/PCI-X I/O	32-bit, 33 MHz	—	0.04	—	—	W	2
	32-bit 66 MHz	—	0.07	—	—		
	64-bit, 66 MHz	—	0.14	—	—		
	64-bit, 133 MHz	—	0.25	—	—		
Local Bus I/O	32-bit, 33 MHz	—	0.07	—	—	W	3
	32-bit, 66 MHz	—	0.13	—	—		
	32-bit, 133 MHz	—	0.24	—	—		
	32-bit, 167 MHz	—	0.30	—	—		
RapidIO I/O	500 MHz data rate	—	0.96	—	—	W	4
TSEC I/O	MII	—	—	10	—	mW	5, 6
	GMII, TBI (2.5 V)	—	—	—	40		
	GMII, TBI (3.3 V)	—	—	70	—		
	RGMII, RTBI	—	—	—	40		
CPM-FCC	MII	—	15	—	—	mW	7
	RMII	—	13	—	—		
	HDLC 16 Mbps	—	9	—	—		
	UTOPIA-8 SPHY	—	60	—	—		
	UTOPIA-8 MPHY	—	100	—	—		
	UTOPIA-16 SPHY	—	94	—	—		
	UTOPIA-16 MPHY	—	135	—	—		
CPM-SCC	HDLC 16 Mbps	—	4	—	—	mW	7

Table 6. Estimated Typical I/O Power Consumption (continued)

Interface	Parameter	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Units	Notes
TDMA or TDMB	Nibble mode	—	10	—	—	mW	7
	Per channel	—	5	—	—		

Notes:

1. GV_{DD}=2.5, ECC enabled, 66% bus utilization, 33% write cycles, 10pF load on data, 10pF load on address/command, 10pF load on clock
2. OV_{DD}=3.3, 30pF load per pin, 54% bus utilization, 33% write cycles
3. OV_{DD}=3.3, 25pF load per pin, 5pF load on clock, 40% bus utilization, 33% write cycles
4. V_{DD}=1.2, OV_{DD}=3.3
5. LVDD=2.5/3.3, 15pF load per pin, 25% bus utilization
6. Power dissipation for one TSEC only
7. OV_{DD}=3.3, 10pF load per pin, 50% bus utilization

4 Clock Timing

4.1 System Clock Timing

Table 7 provides the system clock (SYSCLK) AC timing specifications for the MPC8560.

Table 7. SYSCLK AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	—	—	166	MHz	1
SYSCLK cycle time	t_{SYSCLK}	6.0	—	—	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KHKL}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	+/- 150	ps	4, 5

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, "Platform/System PLL Ratio," and Section 15.3, "e500 Core PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. For spread spectrum clocking, guidelines are +/-1% of the input frequency with a maximum of 60 kHz of modulation regardless of the input frequency.

7.2.2.2 MII Receive AC Timing Specifications

Table 24 provides the MII receive AC timing specifications.

Table 24. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX} [3]	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise and fall time	t_{MRXR}, t_{MRXF} [2,3]	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 11 shows the MII receive AC timing diagram.

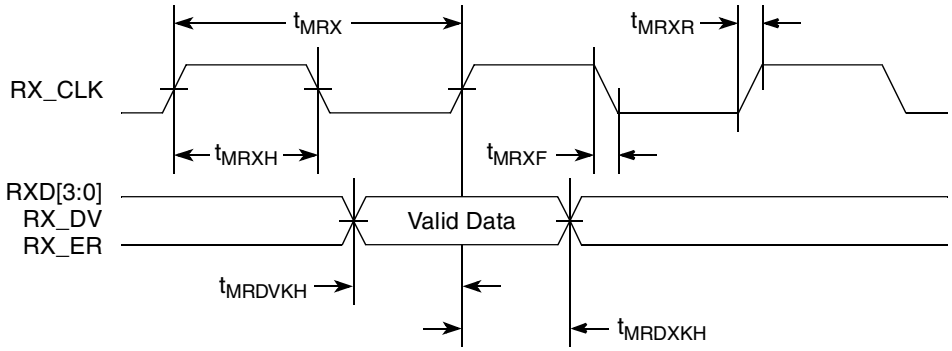

Figure 11. MII Receive AC Timing Diagram

Table 32. Local Bus General Timing Parameters—DLL Bypassed (continued)

Parameter	POR Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to data valid for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKLOV2}$	—	-0.1	ns	4
	TSEC2_TXD[6:5] = 11 (default)			1.4		
Local bus clock to address valid for LAD	TSEC2_TXD[6:5] = 00	$t_{LBKLOV3}$	—	0	ns	4
	TSEC2_TXD[6:5] = 11 (default)			1.5		
Local bus clock to LALE assertion		$t_{LBKHOV4}$	—	0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKLOX1}$	-3.2	—	ns	4
	TSEC2_TXD[6:5] = 11 (default)		-2.3			
Output hold from local bus clock for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKLOX2}$	-3.2	—	ns	4
	TSEC2_TXD[6:5] = 11 (default)		-2.3			
Local bus clock to output high Impedance (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKLOZ1}$	—	0.2	ns	7
	TSEC2_TXD[6:5] = 11 (default)			1.5		
Local bus clock to output high impedance for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKLOZ2}$	—	0.2	ns	7
	TSEC2_TXD[6:5] = 11 (default)			1.5		

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for DLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t_{LBKHKT}.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $OV_{DD}/2$.
4. All signals are measured from $OV_{DD}/2$ of the rising edge of local bus clock for DLL bypass mode to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins TSEC2_TXD[6:5].
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.
9. Guaranteed by design.

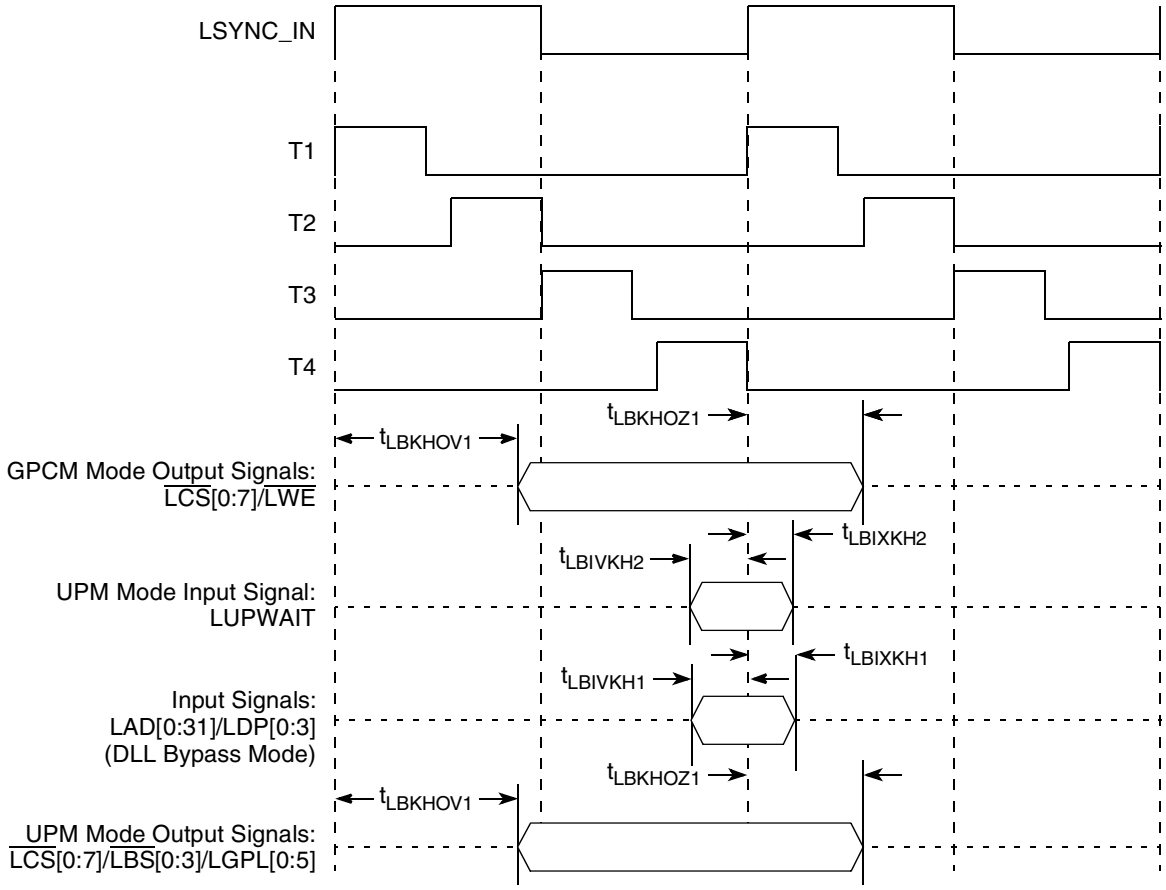

Figure 21. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Enabled)

13.3.2 RapidIO Receiver AC Timing Specifications

The RapidIO receiver AC timing specifications are provided in Table 51. A receiver shall comply with the specifications for each data rate/frequency for which operation of the receiver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The specifications apply over the receiver common mode and differential input voltage ranges.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7])

Table 51. RapidIO Receiver AC Timing Specifications—500 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1, 5
Data valid	DV	1080		ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}	—	380	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–300	300	ps	4

Notes:
1.Measured at V_{ID} = 0 V.
2.Measured using the RapidIO receive mask shown in Figure 46.
3.See Figure 49.
4.See Figure 48 and Figure 49.
5.Guaranteed by design.

Table 52. RapidIO Receiver AC Timing Specifications—750 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1, 5
Data valid	DV	600	—	ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}	—	400	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–267	267	ps	4

Notes:
1.Measured at V_{ID} = 0 V.
2.Measured using the RapidIO receive mask shown in Figure 46.
3.See Figure 49.
4.See Figure 48 and Figure 49.
5.Guaranteed by design.

Table 53. RapidIO Receiver AC Timing Specifications—1 Gbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1, 5
Data valid	DV	425	—	ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}	—	300	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–200	200	ps	4

Notes:

1.Measured at V_{ID} = 0 V.

2.Measured using the RapidIO receive mask shown in Figure 46.

3.See Figure 49.

4.See Figure 48 and Figure 49.

5.Guaranteed by design.

The compliance of receiver input signals RD[0:15] and RFRAME with their minimum data valid window (DV) specification shall be determined by generating an eye pattern for each of the data signals and comparing the eye pattern of each data signal with the RapidIO receive mask shown in Figure 46. The value of X2 used to construct the mask shall be $(1 – DV_{min})/2$. The ±100 mV minimum data valid and ±600 mV maximum input voltage values are from the DC specification. A signal is compliant with the data valid window specification if and only if the receive mask can be positioned on the signal's eye pattern such that the eye pattern falls entirely within the unshaded portion of the mask.

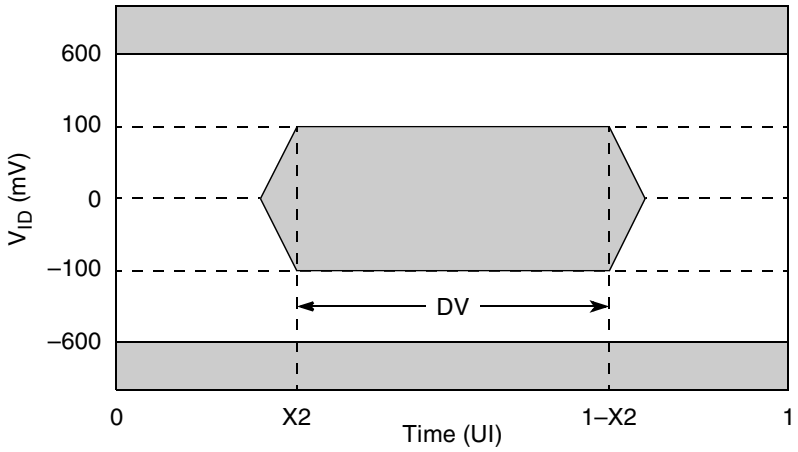

Figure 46. RapidIO Receive Mask

The eye pattern for a data signal is generated by making a large number of recordings of the signal and then overlaying the recordings. The number of recordings used to generate the eye shall be large enough that further increasing the number of recordings used does not cause the resulting eye pattern to change from one that complies with the RapidIO receive mask to one that does not. Each data signal in the interface shall be carrying random or pseudo-random data when the recordings are made. If pseudo-random data is used, the length of the pseudo-random sequence (repeat length) shall be long

Table 54. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface				
MDQ[0:63]	M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12	I/O	GV_{DD}	—
MECC[0:7]	N20, M20, L19, E19, C21, A21, G19, A19	I/O	GV_{DD}	—
MDM[0:8]	L24, H28, F24, L21, E18, E16, G14, B13, M19	O	GV_{DD}	—
MDQS[0:8]	L26, J25, D25, A22, H18, F16, F14, C13, C20	I/O	GV_{DD}	—
MBA[0:1]	B18, B19	O	GV_{DD}	—
MA[0:14]	N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13	O	GV_{DD}	—
$\overline{\text{MWE}}$	D17	O	GV_{DD}	—
$\overline{\text{MRAS}}$	F17	O	GV_{DD}	—
$\overline{\text{MCAS}}$	J16	O	GV_{DD}	—
$\overline{\text{MCS}}$[0:3]	H16, G16, J15, H15	O	GV_{DD}	—
MCKE[0:1]	E26, E28	O	GV_{DD}	11
MCK[0:5]	J20, H25, A15, D20, F28, K14	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	F20, G27, B15, E20, F27, L14	O	GV_{DD}	—
MSYNC_IN	M28	I	GV_{DD}	—
MSYNC_OUT	N28	O	GV_{DD}	—
Local Bus Controller Interface				
LA[27]	U18	O	OV_{DD}	5, 9
LA[28:31]	T18, T19, T20, T21	O	OV_{DD}	7, 9
LAD[0:31]	AD26, AD27, AD28, AC26, AC27, AC28, AA22, AA23, AA26, Y21, Y22, Y26, W20, W22, W26, V19, T22, R24, R23, R22, R21, R18, P26, P25, P20, P19, P18, N22, N23, N24, N25, N26	I/O	OV_{DD}	—
LALE	V21	O	OV_{DD}	8, 9
LBCTL	V20	O	OV_{DD}	9
LCKE	U23	O	OV_{DD}	—
LCLK[0:2]	U27, U28, V18	O	OV_{DD}	—
$\overline{\text{LCS}}$[0:4]	Y27, Y28, W27, W28, R27	O	OV_{DD}	18
$\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$	R28	I/O	OV_{DD}	1

Table 54. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LCS6/DMA_DACK2	P27	O	OV_{DD}	1
LCS7/DMA_DDONE2	P28	O	OV_{DD}	1
LDP[0:3]	AA27, AA28, T26, P21	I/O	OV_{DD}	
LGPL0/LSDA10	U19	O	OV_{DD}	5, 9
LGPL1/LSDWE	U22	O	OV_{DD}	5, 9
LGPL2/LOE/LSDRAS	V28	O	OV_{DD}	8, 9
LGPL3/LSDCAS	V27	O	OV_{DD}	5, 9
LGPL4/LGTA/LUPWAIT/ LPBSE	V23	I/O	OV_{DD}	22
LGPL5	V22	O	OV_{DD}	5, 9
LSYNC_IN	T27	I	OV_{DD}	—
LSYNC_OUT	T28	O	OV_{DD}	—
LWE[0:1]/LSDDQM[0:1]/LBS[0:1]	AB28, AB27	O	OV_{DD}	1, 5, 9
LWE[2:3]/LSDDQM[2:3]/LBS[2:3]	T23, P24	O	OV_{DD}	1, 5, 9
DMA				
DMA_DREQ[0:1]	H5, G4	I	OV_{DD}	—
DMA_DACK[0:1]	H6, G5	O	OV_{DD}	—
DMA_DDONE[0:1]	H7, G6	O	OV_{DD}	—
Programmable Interrupt Controller				
MCP	AG17	I	OV_{DD}	—
UDE	AG16	I	OV_{DD}	—
IRQ[0:7]	AA18, Y18, AB18, AG24, AA21, Y19, AA19, AG25	I	OV_{DD}	—
IRQ8	AB20	I	OV_{DD}	9
IRQ9/DMA_DREQ3	Y20	I	OV_{DD}	1
IRQ10/DMA_DACK3	AF26	I/O	OV_{DD}	1
IRQ11/DMA_DDONE3	AH24	I/O	OV_{DD}	1
IRQ_OUT	AB21	O	OV_{DD}	2, 4
Ethernet Management Interface				
EC_MDC	F1	O	OV_{DD}	5, 9
EC_MDIO	E1	I/O	OV_{DD}	—

Table 54. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Gigabit Reference Clock				
EC_GTX_CLK125	E2	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_TXD[7:4]	A6, F7, D7, C7	O	LV_{DD}	5, 9
TSEC1_TXD[3:0]	B7, A7, G8, E8	O	LV_{DD}	9, 19
TSEC1_TX_EN	C8	O	LV_{DD}	11
TSEC1_TX_ER	B8	O	LV_{DD}	—
TSEC1_TX_CLK	C6	I	LV_{DD}	—
TSEC1_GTX_CLK	B6	O	LV_{DD}	18
TSEC1_CRS	C3	I	LV_{DD}	—
TSEC1_COL	G7	I	LV_{DD}	—
TSEC1_RXD[7:0]	D4, B4, D3, D5, B5, A5, F6, E6	I	LV_{DD}	—
TSEC1_RX_DV	D2	I	LV_{DD}	—
TSEC1_RX_ER	E5	I	LV_{DD}	—
TSEC1_RX_CLK	D6	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_TXD[7:2]	B10, A10, J10, K11,J11, H11	O	LV_{DD}	5, 9
TSEC2_TXD[1:0]	G11, E11	O	LV_{DD}	—
TSEC2_TX_EN	B11	O	LV_{DD}	11
TSEC2_TX_ER	D11	O	LV_{DD}	—
TSEC2_TX_CLK	D10	I	LV_{DD}	—
TSEC2_GTX_CLK	C10	O	LV_{DD}	18
TSEC2_CRS	D9	I	LV_{DD}	—
TSEC2_COL	F8	I	LV_{DD}	—
TSEC2_RXD[7:0]	F9, E9, C9, B9, A9, H9, G10, F10	I	LV_{DD}	—
TSEC2_RX_DV	H8	I	LV_{DD}	—
TSEC2_RX_ER	A8	I	LV_{DD}	—
TSEC2_RX_CLK	E10	I	LV_{DD}	—
RapidIO Interface				
RIO_RCLK	Y25	I	OV_{DD}	—
$\overline{\text{RIO\_RCLK}}$	Y24	I	OV_{DD}	—

Table 54. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
RIO_RD[0:7]	T25, U25, V25, W25, AA25, AB25, AC25, AD25	I	OV_{DD}	—
$\overline{\text{RIO\_RD}}$[0:7]	T24, U24, V24, W24, AA24, AB24, AC24, AD24	I	OV_{DD}	—
RIO_RFRAME	AE27	I	OV_{DD}	—
$\overline{\text{RIO\_RFRAME}}$	AE26	I	OV_{DD}	—
RIO_TCLK	AC20	O	OV_{DD}	11
$\overline{\text{RIO\_TCLK}}$	AE21	O	OV_{DD}	11
RIO_TD[0:7]	AE18, AC18, AD19, AE20, AD21, AE22, AC22, AD23	O	OV_{DD}	—
$\overline{\text{RIO\_TD}}$[0:7]	AD18, AE19, AC19, AD20, AC21, AD22, AE23, AC23	O	OV_{DD}	—
RIO_TFRAME	AE24	O	OV_{DD}	—
$\overline{\text{RIO\_TFRAME}}$	AE25	O	OV_{DD}	—
RIO_TX_CLK_IN	AF24	I	OV_{DD}	—
$\overline{\text{RIO\_TX\_CLK\_IN}}$	AF25	I	OV_{DD}	—
I^2C interface				
IIC_SDA	AH22	I/O	OV_{DD}	4, 20
IIC_SCL	AH23	I/O	OV_{DD}	4, 20
System Control				
$\overline{\text{HRESET}}$	AH16	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	AG20	O	OV_{DD}	—
$\overline{\text{SRESET}}$	AF20	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN}}$	M11	I	OV_{DD}	—
$\overline{\text{CKSTP\_OUT}}$	G1	O	OV_{DD}	2, 4
Debug				
TRIG_IN	N12	I	OV_{DD}	—
TRIG_OUT/READY	G2	O	OV_{DD}	6, 9, 19
MSRCID[0:1]	J9, G3	O	OV_{DD}	5, 6, 9
MSRCID[2:4]	F3, F5, F2	O	OV_{DD}	6
MDVAL	F4	O	OV_{DD}	6
Clock				
SYSCLK	AH21	I	OV_{DD}	—
RTC	AB23	I	OV_{DD}	—
CLK_OUT	AF22	O	OV_{DD}	11

Table 54. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV_{DD}	A4, C5, E7, H10	Reference Voltage; Three-Speed Ethernet I/O (2.5 V, 3.3 V)	LV_{DD}	—
MV_{REF}	N27	Reference Voltage Signal; DDR	MV_{REF}	—
No Connects	AH26, AH27, AH28, AG28, AF28, AE28, AH1, AG1, AH2, B1, B2, A2, A3, AH25	—	—	16
OV_{DD}	D1, E4, H3, K4, K10, L7, M5, N3, P22, R19, R25, T2, T7, U5, U20, U26, V8, W4, W13, W19, W21, Y7, Y23, AA5, AA12, AA16, AA20, AB7, AB9, AB26, AC5, AC11, AC17, AD4, AE1, AE8, AE10, AE15, AF7, AF12, AG27, AH4	PCI/PCI-X, RapidIO, 10/100 Ethernet, and other Standard (3.3 V)	OV_{DD}	—
RESERVED	C1, T11, U11, AF1	—	—	15
SENSEVDD	L12	Power for Core (1.2 V)	V_{DD}	13
SENSEVSS	K12	—	—	13
V_{DD}	M13, M15, M17, N14, N16, P13, P15, P17, R12, R14, R16, T13, T15, T17, U12, U14	Power for Core (1.2 V)	V_{DD}	—
CPM				
PA[0:31]	H1, H2, J1, J2, J3, J4, J5, J6, J7, J8, K8, K7, K6, K3, K2, K1, L1, L2, L3, L4, L5, L8, L9, L10, L11, M10, M9, M8, M7, M6, M3, M2	I/0	OV_{DD}	—
PB[4:31]	M1, N1, N4, N5, N6, N7, N8, N9, N10, N11, P11, P10, P9, P8, P7, P6, P5, P4, P3, P2, P1, R1, R2, R3, R4, R5, R6, R7	I/0	OV_{DD}	—
PC[0:31]	R8, R9, R10, R11, T9, T6, T5, T4, T1, U1, U2, U3, U4, U7, U8, U9, U10, V9, V6, V5, V4, V3, V2, V1, W1, W2, W3, W6, W7, W8, W9, Y9	I/0	OV_{DD}	—

Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-millennium.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the MPC8560 to function in various environments.

16.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8560 thermal model is shown in Figure 52. Five cuboids are used to represent this device. To simplify the model, the solder balls and substrate are modeled as a single block 29x29x1.47 mm with the conductivity adjusted accordingly. For modeling, the planar dimensions of the die are rounded to the nearest mm, so the die is modeled as 10x12 mm at a thickness of 0.76 mm. The bump/underfill layer is modeled as a collapsed resistance between the die and substrate assuming a conductivity of 0.6 in-plane and 1.9 W/m•K in the thickness dimension of 0.76 mm. The lid attach adhesive is also modeled as a collapsed resistance with dimensions of 10x12x0.050 mm and the conductivity of 1 W/m•K. The nickel plated copper lid is modeled as 12x14x1 mm. Note that the die and lid are not centered on the substrate; there is a 1.5 mm offset documented in the case outline drawing in Figure 50.

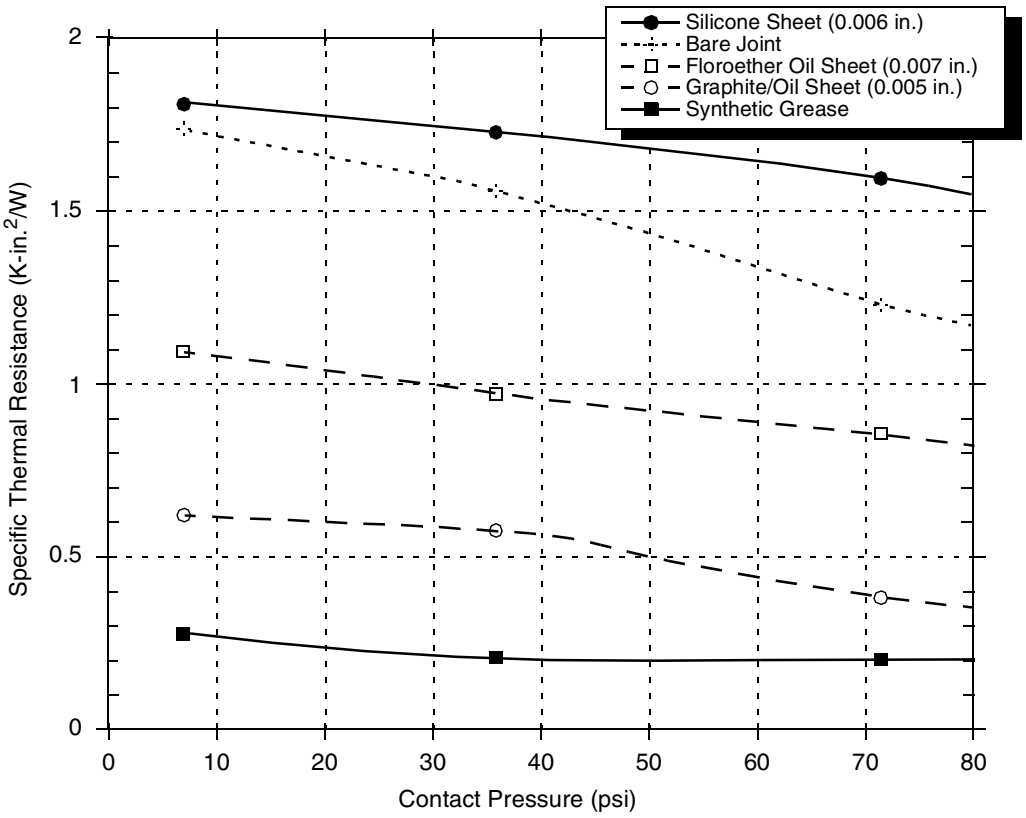

Figure 54. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

Thermagon Inc.
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

888-246-9050

16.2.4 Heat Sink Selection Examples

The following section provides a heat sink selection example using one of the commercially available heat sinks.

16.2.4.1 Case 1

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_I + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

where

T_J is the die-junction temperature

T_I is the inlet cabinet ambient temperature

T_R is the air temperature rise within the computer cabinet

θ_{JC} is the junction-to-case thermal resistance

θ_{INT} is the adhesive or interface material thermal resistance

θ_{SA} is the heat sink base-to-ambient thermal resistance

P_D is the power dissipated by the device

During operation the die-junction temperatures (T_J) should be maintained within the range specified in Table 2. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_A) may range from 30° to 40°C. The air temperature rise within a cabinet (T_R) may be in the range of 5° to 10°C. The thermal resistance of some thermal interface material (θ_{INT}) may be about 1°C/W. Assuming a T_I of 30°C, a T_R of 5°C, a FC-PBGA package θ_{JC} = 0.8, and a power consumption (P_D) of 7.0 W, the following expression for T_J is obtained:

$$\text{Die-junction temperature: } T_J = 30°C + 5°C + (0.8°C/W + 1.0°C/W + \theta_{SA}) \times 7.0\ W$$

The heat sink-to-ambient thermal resistance (θ_{SA}) versus airflow velocity for a Thermalloy heat sink #2328B is shown in Figure 55.

Assuming an air velocity of 2 m/s, we have an effective θ_{SA+} of about 3.3°C/W, thus

$$T_J = 30°C + 5°C + (0.8°C/W + 1.0°C/W + 3.3°C/W) \times 7.0\ W,$$

resulting in a die-junction temperature of approximately 71°C which is well within the maximum operating temperature of the component.

17 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8560.

17.1 System Clocking

The MPC8560 includes three PLLs.

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 15.2, “Platform/System PLL Ratio.”
2. The e500 Core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 15.3, “e500 Core PLL Ratio.”
3. The CPM PLL is slaved to the platform clock and is used to generate clocks used internally by the CPM block. The ratio between the CPM PLL and the platform clock is fixed and not under user control.

17.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$, and $AV_{DD}3$, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide three independent filter circuits as illustrated in Figure 58, one to each of the three AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias.

Table 62. Document Revision History (continued)

Rev. No.	Substantive Change(s)
1.2	Section 1.1.1—Updated feature list. Section 1.2.1.1—Updated notes for Table 1. Section 1.2.1.2—Removed 5-V PCI interface overshoot and undershoot figure. Section 1.2.1.3—Added this section to summarize impedance driver settings for various interfaces. Section 1.4—Updated rows in Reset Initialization timing specifications table. Added a table with DLL and PLL timing specifications. Section 1.5.2.2—Updated note 6 of DDR SDRAM Output AC Timing Specifications table. Section 1.7—Changed the minimum input low current from -600 to -15 μA for the RGMII DC electrical characteristics. Section 1.7.2—Changed LCS[3:4] to TSEC1_TXD[6:5]. Updated notes regarding LCS[3:4]. Section 1.13.2—Updated the mechanical dimensions diagram for the package. Section 1.13.3—Updated the notes for LBCTL, TRIG_OUT, and ASLEEP. Corrected pin assignments for IIC_SDA and IIC_SCL. Corrected reserved pin assignment of V11 to U11. V11 is actually $\overline{\text{PCI\_STOP}}$. Section 1.14.1—Updated the table for frequency options with respect to platform/CCB frequencies. Section 1.14.4—Edited Frequency options with respect to memory bus speeds.
1.1	Made updates throughout document. Section 1.6.1—Added symbols and note for the GTX_CLK125 timing parameters. Section 1.11.3—Updated pin list table: LGPL5/LSDAMUX to LGPL5, LA[27:29] and LA[30:31] to LA[27:31], TRST to $\overline{\text{TRST}}$, added GBE Clocking section and EC_GTX_CLK125 signal. Figure 50—Updated pin 2 connection information.
1	Original Customer Version.

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