E·XFL

NXP USA Inc. - MPC8560CPX667LB Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8560cpx667lb

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Overview

- General-purpose parallel ports—16 parallel I/O lines with interrupt capability
- Supports inverse muxing of ATM cells (IMA)
- 256 Kbyte L2 cache/SRAM
 - Can be configured as follows
 - Full cache mode (256-Kbyte cache).
 - Full memory-mapped SRAM mode (256-Kbyte SRAM mapped as a single 256-Kbyte block or two 128-Kbyte blocks)
 - Half SRAM and half cache mode (128-Kbyte cache and 128-Kbyte memory-mapped SRAM)
 - Full ECC support on 64-bit boundary in both cache and SRAM modes
 - Cache mode supports instruction caching, data caching, or both
 - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing)
 - Eight-way set-associative cache organization (1024 sets of 32-byte cache lines)
 - Supports locking the entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions
 - Global locking and flash clearing done through writes to L2 configuration registers
 - Instruction and data locks can be flash cleared separately
 - Read and write buffering for internal bus accesses
 - SRAM features include the following:
 - I/O devices access SRAM regions by marking transactions as snoopable (global)
 - Regions can reside at any aligned location in the memory map
 - Byte accessible ECC is protected using read-modify-write transactions accesses for smaller than cache-line accesses.
- Address translation and mapping unit (ATMU)
 - Eight local access windows define mapping within local 32-bit address space
 - Inbound and outbound ATMUs map to larger external address spaces
 - Three inbound windows plus a configuration window on PCI/PCI-X
 - Four inbound windows plus a default and configuration window on RapidIO
 - Four outbound windows plus default translation for PCI
 - Eight outbound windows plus default translation for RapidIO
- DDR memory controller
 - Programmable timing supporting DDR-1 SDRAM
 - 64-bit data interface, up to 333-MHz data rate
 - Four banks of memory supported, each up to 1 Gbyte
 - DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
 - Full ECC support
 - Page mode support (up to 16 simultaneous open pages)

Overview

- Interrupts can be routed to the e500 core's standard or critical interrupt inputs
- Interrupt summary registers allow fast identification of interrupt source
- I²C controller
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I²C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I²C addressing mode
 - Data integrity checked with preamble signature and CRC
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data operating at up to 166 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
 - Three protocol engines available on a per chip select basis:
 - General purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)
 - Dedicated single data rate SDRAM controller
 - Parity support
 - Default boot ROM chip select with configurable bus width (8-,16-, or 32-bit)
- Two three-speed (10/100/1Gb) Ethernet controllers (TSECs)
 - Dual IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab compliant controllers
 - Support for different Ethernet physical interfaces:
 - 10/100/1Gb Mbps IEEE 802.3 GMII
 - 10/100 Mbps IEEE 802.3 MII
 - 10 Mbps IEEE 802.3 MII
 - 1000 Mbps IEEE 802.3z TBI
 - 10/100/1Gb Mbps RGMII/RTBI
 - Full- and half-duplex support
 - Buffer descriptors are backward compatible with MPC8260 and MPC860T 10/100 programming models
 - 9.6-Kbyte jumbo frame support
 - RMON statistics support
 - 2-Kbyte internal transmit and receive FIFOs

NOTE

If the items on line 2 must precede items on line 1, please ensure that the delay will not exceed 500 ms and the power sequence is not done greater than once per day in production environment.

NOTE

From a system standpoint, if the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os on the MPC8560 may drive a logic one or zero during power-up.

2.1.3 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8560. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Characteristic			Recommended Value	Unit
Core supply voltage For e	devices rated at 667 and 833 MHz For devices rated at 1 GHz	V _{DD}	1.2 V ± 60 mV 1.3 V ± 50 mV	V
PLL supply voltage For devices rated at 667 and 833 MHz For devices rated at 1 GHz			1.2 V ± 60 mV 1.3 V ± 50 mV	V
DDR DRAM I/O voltage			2.5 V ± 125 mV	V
Three-speed Ethernet I/O voltage	LV _{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	
CPM, PCI/PCI-X, local bus, RapidIO, 10/100 DUART, system control and power managen	OV _{DD}	3.3 V ± 165 mV	V	
Input voltage	DDR DRAM signals	MV _{IN}	GND to GV _{DD}	V
	DDR DRAM reference	MV _{REF}	GND to GV _{DD/2}	V
	Three-speed Ethernet signals	LV _{IN}	GND to LV _{DD}	V
	CPM, PCI/PCI-X, local bus, RapidIO, 10/100 Ethernet, MII management, DUART, SYSCLK, system control and power management, I ² C, and JTAG signals	OV _{IN}	GND to OV _{DD}	V
Die-junction temperature		Тj	0 to 105	°C

Table 2. Recommended Operating Conditions

6 DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8560.

6.1 DDR SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8560.

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	GV _{DD}	2.375	2.625	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.18	GV _{DD} + 0.3	V	4
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.18	V	4
Output leakage current	I _{oz}	-10	10	μA	5
Output high current (V _{OUT} = 1.95 V)	I _{ОН}	-15.2	—	mA	—
Output low current (V _{OUT} = 0.35 V)	I _{OL}	15.2	—	mA	—
MV _{REF} input leakage current	I _{VREF}	_	100	μA	—

Table 13. DDR SDRAM DC Electrical Characteristics

Notes:

 $1.GV_{DD}$ is expected to be within 50 mV of the DRAM GV_{DD} at all times.

- $2.MV_{REF}$ is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
- $3.V_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail should track variations in the DC level of MV_{REF} .
- $4.V_{IH}$ can tolerate an overshoot of 1.2V over GV_{DD} for a pulse width of \leq 3 ns, and the pulse width cannot be greater than t_{MCK} . V_{IL} can tolerate an undershoot of 1.2V below GND for a pulse width of \leq 3 ns, and the pulse width cannot be greater than t_{MCK} .
- 5. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}

Table 14 provides the DDR capacitance.

Table 14. DDR SDRAM Capacitance

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, MSYNC_IN	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak to peak) = 0.2 V.

7.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

7.2.2.1 MII Transmit AC Timing Specifications

Table 23 provides the MII transmit AC timing specifications.

Table 23. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TX_CLK clock period 10 Mbps	t _{MTX} ²	—	400	—	ns
TX_CLK clock period 100 Mbps	t _{MTX}	—	40	—	ns
TX_CLK duty cycle	t _{MTXH} /t _{MTX}	35	_	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t _{MTKHDX}	1	5	15	ns
TX_CLK data clock rise and fall time	t _{MTXR} , t _{MTXF} ^{2,3}	1.0	_	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2.Signal timings are measured at 0.7 V and 1.9 V voltage levels.3.Guaranteed by design.

Figure 10 shows the MII transmit AC timing diagram.



Figure 10. MII Transmit AC Timing Diagram

Local Bus

Parameter	POR Configuration	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output high impedance	TSEC2_TXD[6:5] = 00	t _{LBKHOZ2}	_	2.5	ns	7, 9
for LAD/LDP	TSEC2_TXD[6:5] = 11 (default)			3.8		

 Table 31. Local Bus General Timing Parameters—DLL Enabled (continued)

Notes:

1.The symbols used for timing specifications herein follow the pattern of t_{(First two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(First two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the output (O) going invalid (X) or output hold time.}}

2.All timings are in reference to LSYNC_IN for DLL enabled mode.

3.Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at OV_{DD}/2.

4.All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for DLL enabled to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.

5.Input timings are measured at the pin.

- 6.The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins TSEC2_TXD[6:5].
- 7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

8. Guaranteed by characterization.

9.Guaranteed by design.

Table 32 describes the general timing parameters of the local bus interface of the MPC8560 with the DLL bypassed.

Table 32. Local Bus General Timing Parameters—DLL Bypassed

Parameter	POR Configuration	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	_	t _{LBK}	6.0	—	ns	2
Internal launch/capture clock to LCLK delay	—	t _{LBKHKT}	2.3	3.9	ns	8
LCLK[n] skew to LCLK[m] or LSYNC_OUT	—	t _{LBKSKEW}		150	ps	3, 9
Input setup to local bus clock (except LUPWAIT)	_	t _{LBIVKH1}	5.7	—	ns	4, 5
LUPWAIT input setup to local bus clock	_	t _{LBIVKH2}	5.6	—	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	_	t _{LBIXKH1}	-1.8	—	ns	4, 5
LUPWAIT input hold from local bus clock	_	t _{LBIXKH2}	-1.3	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	_	t _{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	t _{LBKLOV1}	_	-0.3	ns	4
	TSEC2_TXD[6:5] = 11 (default)			1.2		

Parameter	POR Configuration	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to data valid for LAD/LDP	TSEC2_TXD[6:5] = 00	t _{LBKLOV2}		-0.1	ns	4
	TSEC2_TXD[6:5] = 11 (default)			1.4		
Local bus clock to address valid for LAD	TSEC2_TXD[6:5] = 00	t _{LBKLOV3}		0	ns	4
	TSEC2_TXD[6:5] = 11 (default)			1.5		
Local bus clock to LALE assertion		t _{LBKHOV4}		0	ns	4
Output hold from local bus clock (except	TSEC2_TXD[6:5] = 00	t _{LBKLOX1}	-3.2	—	ns	4
LAD/LDP and LALE)	TSEC2_TXD[6:5] = 11 (default)		-2.3			
Output hold from local bus clock for	TSEC2_TXD[6:5] = 00	t _{LBKLOX2}	-3.2	—	ns	4
LAD/LDP	TSEC2_TXD[6:5] = 11 (default)		-2.3			
Local bus clock to output high Impedance	TSEC2_TXD[6:5] = 00	t _{LBKLOZ1}	_	0.2	ns	7
(except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 11 (default)			1.5		
Local bus clock to output high impedance	TSEC2_TXD[6:5] = 00	t _{LBKLOZ2}	_	0.2	ns	7
	TSEC2_TXD[6:5] = 11 (default)			1.5		

Table 32. Local Bus General	Timing Parameters—DLL B	vpassed (continued)
		,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,

Notes:

1. The symbols used for timing specifications herein follow the pattern of t_{(First two letters of functional block)(signal)(state) (reference)(state) for inputs and t_(First two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the output (O) going invalid (X) or output hold time.}

2.All timings are in reference to local bus clock for DLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by tLBKHKT.

3.Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at OV_{DD}/2.

4.All signals are measured from $OV_{DD}/2$ of the rising edge of local bus clock for DLL bypass mode to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.

5.Input timings are measured at the pin.

6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins TSEC2_TXD[6:5].

7.For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

8. Guaranteed by characterization.

9. Guaranteed by design.

PCI/PCI-X

12.2 PCI/PCI-X AC Electrical Specifications

This section describes the general AC timing parameters of the PCI/PCI-X bus of the MPC8560. Note that the SYSCLK signal is used as the PCI input clock. Table 43 provides the PCI AC timing specifications at 66 MHz.

Parameter	Symbol ¹	Min	Max	Unit	Notes
SYSCLK to output valid	^t PCKHOV	-	6.0	ns	2
Output hold from SYSCLK	t _{PCKHOX}	2.0	_	ns	2, 9
SYSCLK to output high impedance	t _{PCKHOZ}	-	14	ns	2, 3, 10
Input setup to SYSCLK	t _{PCIVKH}	3.0	_	ns	2, 4, 9
Input hold from SYSCLK	^t РСІХКН	0	_	ns	2, 4, 9
REQ64 to HRESET ⁹ setup time	t _{PCRVRH}	$10 imes t_{SYS}$	_	clocks	5, 6, 10
HRESET to REQ64 hold time	t _{PCRHRX}	0	50	ns	6, 10
HRESET high to first FRAME assertion	t _{PCRHFV}	10	_	clocks	7, 10

Table 43. PCI AC Timing Specifications at 66 MHz

Notes:

1.Note that the symbols used for timing specifications herein follow the pattern of t(first two letters of functional

block)(signal)(state) (reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{PCIVKH} symbolizes PCI/PCI-X timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI/PCI-X timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.

2.See the timing measurement conditions in the PCI 2.2 Local Bus Specifications.

3.For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

- 4.Input timings are measured at the pin.
- 5. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 15, "Clocking."

6.The setup and hold time is with respect to the rising edge of HRESET.

- 7. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
- 8. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 µs.
- 9. Guaranteed by characterization.

10.Guaranteed by design.

PCI/PCI-X

Figure 16 provides the AC test load for PCI and PCI-X.



Figure 38. PCI/PCI-X AC Test Load

Figure 39 shows the PCI/PCI-X input AC timing conditions.



Figure 39. PCI-PCI-X Input AC Timing Measurement Conditions

Figure 40 shows the PCI/PCI-X output AC timing conditions.



Figure 40. PCI-PCI-X Output AC Timing Measurement Condition

Table 44 provides the PCI-X AC timing specifications at 66 MHz.

Table 44. PCI-X AC Timing Specifications at 66 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	^t PCKHOV	_	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t _{PCKHOX}	0.7	_	ns	1, 10
SYSCLK to output high impedance	t _{PCKHOZ}	_	7	ns	1, 4, 8, 11
Input setup time to SYSCLK	t _{PCIVKH}	1.7	_	ns	3, 5
Input hold time from SYSCLK	t _{PCIXKH}	0.5	_	ns	10
REQ64 to HRESET setup time	t _{PCRVRH}	10	_	clocks	11
HRESET to REQ64 hold time	t _{PCRHRX}	0	50	ns	11
HRESET high to first FRAME assertion	t _{PCRHFV}	10	_	clocks	9, 11

Parameter	Symbol	Min	Max	Unit	Notes
PCI-X initialization pattern to HRESET setup time	^t PCIVRH	10		clocks	11
HRESET to PCI-X initialization pattern hold time	t _{PCRHIX}	0	50	ns	6, 11

Table 44. PCI-X AC Timing Specifications at 66 MHz (continued)

Notes:

1.See the timing measurement conditions in the PCI-X 1.0a Specification.

2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.

3.Setup time for point-to-point signals applies to REQ and GNT only. All other signals are bused.

4.For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.

6.Maximum value is also limited by delay to the first transaction (time for HRESET high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of HRESET must be negated no later than two clocks before the first FRAME and must be floated no later than one clock before FRAME is asserted.

7.A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.

8.Device must meet this specification independent of how many outputs switch simultaneously.

9. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification*. 10. Guaranteed by characterization.

11.Guaranteed by design.

Table 45 provides the PCI-X AC timing specifications at 133 MHz.

	ng Specifica	lions at 15	5 WIT12		
Parameter	Symbol	Min	Мах	Unit	Notes
SYSCLK to signal valid delay	^t PCKHOV	_	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t _{PCKHOX}	0.7	—	ns	1, 11
SYSCLK to output high impedance	t _{PCKHOZ}	_	7	ns	1, 4, 8, 12
Input setup time to SYSCLK	^t РСІVКН	1.4	—	ns	3, 5, 9, 11
Input hold time from SYSCLK	t _{PCIXKH}	0.5	—	ns	11
REQ64 to HRESET setup time	t _{PCRVRH}	10	—	clocks	12
HRESET to REQ64 hold time	t _{PCRHRX}	0	50	ns	12
HRESET high to first FRAME assertion	t _{PCRHFV}	10	—	clocks	10, 12
PCI-X initialization pattern to HRESET setup time	^t PCIVRH	10	—	clocks	12

Table 45. PCI-X AC Timing Specifications at 133 MHz

Table 45. PCI-X A	C Timing Specifications a	at 133 MHz (continued)
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Parameter	Symbol	Min	Max	Unit	Notes
HRESET to PCI-X initialization pattern hold time	t _{PCRHIX}	0	50	ns	6, 12

Notes:

1.See the timing measurement conditions in the PCI-X 1.0a Specification.

- 2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
- 3.Setup time for point-to-point signals applies to REQ and GNT only. All other signals are bused.
- 4.For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
- 6.Maximum value is also limited by delay to the first transaction (time for HRESET high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of HRESET must be negated no later than two clocks before the first FRAME and must be floated no later than one clock before FRAME is asserted.
- 7.A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
- 8. Device must meet this specification independent of how many outputs switch simultaneously.
- 9. The timing parameter t_{PCIVKH} is a minimum of 1.4 ns rather than the minimum of 1.2 ns in the *PCI-X* 1.0a *Specification.*
- 10. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*
- 11. Guaranteed by characterization.
- 12.Guaranteed by design.

13 RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8560.

13.1 RapidIO DC Electrical Characteristics

RapidIO driver and receiver DC electrical characteristics are provided in Table 46 and Table 47, respectively.

Table 46. RapidIO 8/16 LP-LVDS Driver DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Characteristic	Symbol	Min	Мах	Unit	Notes
Differential output high voltage	V _{OHD}	247	454	mV	1, 2
Differential output low voltage	V _{OLD}	-454	-247	mV	1, 2
Differential offset voltage	ΔV_{OSD}	—	50	mV	1,3
Output high common mode voltage	V _{OHCM}	1.125	1.375	V	1, 4
Output low common mode voltage	V _{OLCM}	1.125	1.375	V	1, 5

MPC8560 Integrated Processor Hardware Specifications, Rev. 4.2

Characteristic	Symbol	Rai	nge	Unit	Notes
Characteristic	Symbol	Min	Мах	Onit	NOLES
Differential output high voltage	V _{OHD}	200	540	mV	1
Differential output low voltage	V _{OLD}	-540	-200	mV	1
Duty cycle	DC	48	52	%	2, 6
V _{OD} rise time, 20%–80% of peak to peak differential signal swing	t _{FALL}	100	_	ps	3, 6
V _{OD} fall time, 20%–80% of peak to peak differential signal swing	t _{RISE}	100	_	ps	6
Data valid	DV	575	_	ps	6
Skew of any two data outputs	t _{DPAIR}	_	100	ps	4, 6
Skew of single data outputs to associated clock	t _{SKEW,PAIR}	-100	100	ps	5, 6

Table 50. RapidIO Driver AC Timing Specifications—1 Gbps Data Rate

Notes:

1.See Figure 44.

2.Requires ±100 ppm long term frequency stability.

3.Measured at $V_{OD} = 0$ V.

4.Measured using the RapidIO transmit mask shown in Figure 44.

5.See Figure 49.

6.Guaranteed by design.

The compliance of driver output signals TD[0:15] and TFRAME with their minimum data valid window (DV) specification shall be determined by generating an eye pattern for each of the data signals and comparing the eye pattern of each data signal with the RapidIO transmit mask shown in Figure 44. The value of X2 used to construct the mask shall be $(1 - DV_{min})/2$. A signal is compliant with the data valid window specification if the transmit mask can be positioned on the signal's eye pattern such that the eye pattern falls entirely within the unshaded portion of the mask.



Figure 44. RapidIO Transmit Mask

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Package and Pin Listings

Signal	Signal Package Pin Number		Power Supply	Notes		
JTAG						
тск	AF21	I	OV _{DD}	_		
TDI	AG21	I	OV _{DD}	12		
TDO	AF19	0	OV _{DD}	11		
TMS	AF23	I	OV _{DD}	12		
TRST	AG23	I	OV _{DD}	12		
	DFT					
LSSD_MODE	AG19	I	OV _{DD}	21		
L1_TSTCLK	AB22	I	OV _{DD}	21		
L2_TSTCLK	AG22	I	OV _{DD}	21		
TEST_SEL	AH20	I	OV _{DD}	3		
	Thermal Management					
THERM0	AG2	I	—	14		
THERM1	AH3	I	—	14		
	Power Management					
ASLEEP	AG18	I/O		9, 19		
	Power and Ground Signals					
AV _{DD} 1	AH19	Power for e500 PLL (1.2 V)	AV _{DD} 1	_		
AV _{DD} 2	AH18	Power for CCB PLL (1.2 V)	AV _{DD} 2	_		
AV _{DD} 3	AH17	Power for CPM PLL (1.2 V)	AV _{DD} 3	_		
GND	 A12, A17, B3, B14, B20, B26, B27, C2, C4, C11,C17, C19, C22, C27, D8, E3, E12, E24, F11, F18, F23, G9, G12, G25, H4, H12, H14, H17, H20, H22, H27, J19, J24, K5, K9, K18, K23, K28, L6, L20, L25, M4, M12, M14, M16, M22, M27, N2, N13, N15, N17, P12, P14, P16, P23, R13, R15, R17, R20, R26, T3, T8, T10, T12, T14, T16, U6, U13, U15, U16, U17, U21, V7, V10, V26, W5, W18, W23, Y8, Y16, AA6, AA13, AB4, AB11, AB19, AC6, AC9, AD3, AD8, AD17, AF2, AF4, AF10, AF13, AF15, AF27, AG3, AG7, AG26 	_	—	_		
GV _{DD}	A14, A20, A25, A26, A27, A28, B17, B22, B28, C12, C28, D16, D19, D21, D24, D28, E17, E22, F12, F15, F19, F25, G13, G18, G20, G23, G28, H19, H24, J12, J17, J22, J27, K15, K20, K25, L13, L23, L28, M25, N21	Power for DDR DRAM I/O Voltage (2.5 V)	GV _{DD}	_		

MPC8560 Integrated Processor Hardware Specifications, Rev. 4.2

Package and Pin Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PD[4:31]	Y1, Y2, Y3, Y4, Y5, Y6, AA8, AA7, AA4, AA3, AA2, AA1, AB1, AB2, AB3, AB5, AB6, AC7, AC4, AC3, AC2, AC1, AD1, AD2, AD5, AD6, AE3, AE2	Ι/Ο	OV _{DD}	

Notes:

- 1.All multiplexed signals are listed only once and do not re-occur. For example, LCS5/DMA_REQ2 is listed only once in the Local Bus Controller Interface section, and is not mentioned in the DMA section even though the pin also functions as DMA_REQ2.
- 2.Recommend a weak pull-up resistor (2–10 k Ω) be placed on this pin to OV_{DD}.
- 3. This pin must always be pulled up to $\ensuremath{\text{OV}_{\text{DD}}}$.
- 4. This pin is an open drain signal.
- 5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the MPC8560 is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. If an external device connected to this pin might pull it down during reset, then a pull-up or active driver is needed if the signal is intended to be high during reset.
- 6. Treat these pins as no connects (NC) unless using debug address functionality.
- 7. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 15.2, "Platform/System PLL Ratio."
- 8. The value of LALE and LGPL2 at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 15.3, "e500 Core PLL Ratio."
- 9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
- 10. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. Refer to the *PCI Specification*.
- 11. This output is actively driven during reset rather than being three-stated during reset.
- 12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 13. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
- 14.Internal thermally sensitive resistor.
- 15.No connections should be made to these pins.
- 16. These pins are not connected for any functional use.
- 17.PCI specifications recommend that a weak pull-up resistor (2–10 k Ω) be placed on the higher order pins to OV_{DD} when using 64-bit buffer mode (pins PCI_AD[63:32] and PCI_C_BE[7:4]).
- 18.Note that these signals are POR configurations for Rev. 1.x and notes 5 and 9 apply to these signals in Rev. 1.x but not in later revisions.
- 19 If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a logic -1 state during reset.
- 20.Recommend a pull-up resistor (~1 K Ω) b placed on this pin to OV_{DD}.
- 21. These are test signals for factory use only and must be pulled up (100 Ω 1 k Ω) to OVDD for normal machine operation.
- 22. If this signal is used as both an input and an output, a weak pull-up (~10 k Ω) is required on this pin.

Thermal

Alpha Novatech	408-749-7601
473 Sapena Ct #15	+00-7+7-7001
Santa Clara, CA 95054	
Internet: www.alphanovatech.com	
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502	818-842-7277
Internet: www.ctscorp.com	
Millennium Electronics (MEI)	408-436-8770
Loroco Sites	
671 East Brokaw Road	
San Jose, CA 95112	
Internet: www.mei-millennium.com	
Tyco Electronics	800-522-6752
Chip Coolers TM	
P.O. Box 3668	
Harrisburg, PA 17105-3668	
Internet: www.chipcoolers.com	
Wakefield Engineering	603-635-5102
33 Bridge St.	
Pelham, NH 03076	
Internet: www.wakefield.com	

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the MPC8560 to function in various environments.

16.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8560 thermal model is shown in Figure 52. Five cuboids are used to represent this device. To simplify the model, the solder balls and substrate are modeled as a single block 29x29x1.47 mm with the conductivity adjusted accordingly. For modeling, the planar dimensions of the die are rounded to the nearest mm, so the die is modeled as 10x12 mm at a thickness of 0.76 mm. The bump/underfill layer is modeled as a collapsed resistance between the die and substrate assuming a conductivity of 0.6 in-plane and 1.9 W/m•K in the thickness dimension of 0.76 mm. The lid attach adhesive is also modeled as a collapsed resistance with dimensions of 10x12x0.050 mm and the conductivity of 1 W/m•K. The nickel plated copper lid is modeled as 12x14x1 mm. Note that the die and lid are not centered on the substrate; there is a 1.5 mm offset documented in the case outline drawing in Figure 50.

Thermal

Figure 53 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 53. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

16.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 54 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 51). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink, the heat sink should be slowly removed. Heating the heat sink to 40-50°C with an air gun can soften the interface material and make the removal easier. The use of an adhesive for heat sink attach is not recommended.

17 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8560.

17.1 System Clocking

The MPC8560 includes three PLLs.

- 1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 15.2, "Platform/System PLL Ratio."
- 2. The e500 Core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 15.3, "e500 Core PLL Ratio."
- 3. The CPM PLL is slaved to the platform clock and is used to generate clocks used internally by the CPM block. The ratio between the CPM PLL and the platform clock is fixed and not under user control.

17.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD}1, AV_{DD}2, and AV_{DD}3, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide three independent filter circuits as illustrated in Figure 58, one to each of the three AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias.

System Design Information

When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.



Figure 59. Driver Impedance Measurement

The output impedance of the RapidIO port drivers targets 200- Ω differential resistance. The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term} . The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 61 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD} , nominal OV_{DD} , 105°C.

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI/PCI-X	DDR DRAM	RapidIO	Symbol	Unit
R _N	43 Target	25 Target	20 Target	NA	Z ₀	W
R _P	43 Target	25 Target	20 Target	NA	Z ₀	W
Differential	NA	NA	NA	200 Target	Z _{DIFF}	W

Table 61. Impedance Characteristics

Note: Nominal supply voltages. See Table 1, $T_i = 105^{\circ}C$.

Device Nomenclature

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