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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

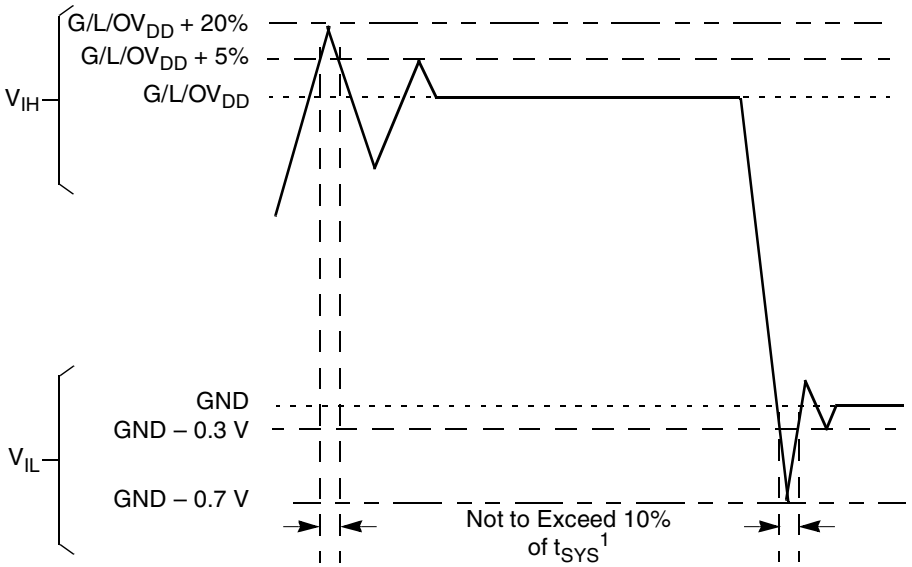
Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8560cvt667jb

  - General-purpose parallel ports—16 parallel I/O lines with interrupt capability
  - Supports inverse muxing of ATM cells (IMA)
- 256 Kbyte L2 cache/SRAM
  - Can be configured as follows
    - Full cache mode (256-Kbyte cache).
    - Full memory-mapped SRAM mode (256-Kbyte SRAM mapped as a single 256-Kbyte block or two 128-Kbyte blocks)
    - Half SRAM and half cache mode (128-Kbyte cache and 128-Kbyte memory-mapped SRAM)
  - Full ECC support on 64-bit boundary in both cache and SRAM modes
  - Cache mode supports instruction caching, data caching, or both
  - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing)
  - Eight-way set-associative cache organization (1024 sets of 32-byte cache lines)
  - Supports locking the entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions
  - Global locking and flash clearing done through writes to L2 configuration registers
  - Instruction and data locks can be flash cleared separately
  - Read and write buffering for internal bus accesses
  - SRAM features include the following:
    - I/O devices access SRAM regions by marking transactions as snoopable (global)
    - Regions can reside at any aligned location in the memory map
    - Byte accessible ECC is protected using read-modify-write transactions accesses for smaller than cache-line accesses.
- Address translation and mapping unit (ATMU)
  - Eight local access windows define mapping within local 32-bit address space
  - Inbound and outbound ATMUs map to larger external address spaces
    - Three inbound windows plus a configuration window on PCI/PCI-X
    - Four inbound windows plus a default and configuration window on RapidIO
    - Four outbound windows plus default translation for PCI
    - Eight outbound windows plus default translation for RapidIO
- DDR memory controller
  - Programmable timing supporting DDR-1 SDRAM
  - 64-bit data interface, up to 333-MHz data rate
  - Four banks of memory supported, each up to 1 Gbyte
  - DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
  - Full ECC support
  - Page mode support (up to 16 simultaneous open pages)

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8560.



Note:
t_{SYS} refers to the clock period associated with the SYSCLK signal.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

The MPC8560 core voltage must always be provided at nominal 1.2 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

3 Power Characteristics

The estimated power dissipation on the V_{DD} supply for the MPC8560 is shown in Table 4.

Table 4. MPC8560 V_{DD} Power Dissipation [1,2]

CCB Frequency (MHz)	Core Frequency (MHz)	Typical Power[3,4]	Maximum Power[5]	Unit
200	400	5.1	7.7	W
	500	5.4	8.0	
	600	5.8	8.4	
267	533	6.0	8.7	W
	667	6.4	9.2	
	800	6.9	10.7	
333	667	6.8	9.8	W
	833	7.4	11.4	
	1000 [6]	11.9	16.5	

Notes:

1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}.
2. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, air flow, power dissipation of other components on the board, and board thermal resistance. Any customer design must take these considerations into account to ensure the maximum 105 °C junction temperature is not exceeded on this device.
3. Typical Power is based on a nominal voltage of V_{DD} = 1.2 V, a nominal process, a junction temperature of T_j = 105 °C, and a Dhrystone 2.1 benchmark application.
4. Thermal solutions will likely need to design to a number higher than Typical Power based on the end application, T_A target, and I/O power.
5. Maximum power is based on a nominal voltage of V_{DD} = 1.2 V, worst case process, a junction temperature of T_j = 105 °C, and an artificial smoke test.
6. The nominal recommended V_{DD} is 1.3 V for this speed grade.

The estimated power dissipation on the AV_{DD} supplies for the MPC8560 PLLs is shown in Table 5.

Table 5. MPC8560 AV_{DD} Power Dissipation

$AV_{DD}n$	Typical[1]	Unit
$AV_{DD}1$	0.007	W
$AV_{DD}2$	0.014	W
$AV_{DD}3$	0.004	W

Notes:

1. V_{DD} = 1.2 V(1.3 V for 1.0 GHz device), T_J = 105°C

6.2.2 DDR SDRAM Output AC Timing Specifications

For chip selects $\overline{\text{MCS1}}$ and $\overline{\text{MCS2}}$, there will always be at least 200 DDR memory clocks coming out of self-refresh after an $\overline{\text{HRESET}}$ before a precharge occurs. This will not necessarily be the case for chip selects $\overline{\text{MCS0}}$ and $\overline{\text{MCS3}}$.

6.2.2.1 DLL Enabled Mode

Table 16 and Table 17 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface with the DDR DLL enabled.

Table 16. DDR SDRAM Output AC Timing Specifications–DLL Mode

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing)	t_{MCK}	6	10	ns	2
On chip Clock Skew	$t_{MCKSKEW}$	—	150	ps	3, 8
MCK[n] duty cycle	t_{MCKH}/t_{MCK}	45	55	%	8
ADDR/CMD output valid	t_{DDKHOV}	—	3	ns	4, 9
ADDR/CMD output invalid	t_{DDKHOX}	1	—	ns	4, 9
Write CMD to first MDQS capture edge	t_{DDSHMH}	t_{MCK} + 1.5	t_{MCK} + 4.0	ns	5
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 900 1100 1200	—	ps	6, 9
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 900 1100 1200	—	ps	6, 9
MDQS preamble start	t_{DDSHMP}	0.75 × t_{MCK} + 1.5	0.75 × t_{MCK} + 4.0	ns	7, 8

Table 16. DDR SDRAM Output AC Timing Specifications–DLL Mode (continued)

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDSHME}	1.5	4.0	ns	7, 8

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (OX or DX). For example, t_{DDKHOV} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (O) are valid (V) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. Maximum possible clock skew between a clock MCK[n] and its relative inverse clock $\overline{\text{MCK}}$[n], or between a clock MCK[n] and a relative clock MCK[m] or MSYNC_OUT. Skew measured between complementary signals at $GV_{DD}/2$.
4. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$ and MDQ/MECC/MDM/MDQS.
5. Note that t_{DDSHMH} follows the symbol conventions described in note 1. For example, t_{DDSHMH} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) until the MDQS signal is valid (MH). t_{DDSHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. These controls allow the relationship between the synchronous clock control timing and the source-synchronous DQS domain to be modified by the user. For best turnaround times, these may need to be set to delay t_{DDSHMH} an additional $0.25t_{MCK}$. This will also affect t_{DDSHMP} and t_{DDSHME} accordingly. See the *MPC8560 PowerQUICC III Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8560.
7. All outputs are referenced to the rising edge of MSYNC_IN (S) at the pins of the MPC8560. Note that t_{DDSHMP} follows the symbol conventions described in note 1. For example, t_{DDSHMP} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) for the duration of the MDQS signal precharge period (MP).
8. Guaranteed by design.
9. Guaranteed by characterization.

Figure 5 provides the AC test load for the DDR bus.

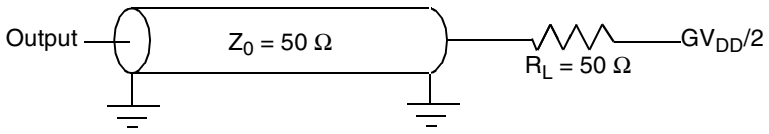


Figure 5. DDR AC Test Load

Table 17. DDR SDRAM Measurement Conditions

Symbol	DDR	Unit	Notes
V_{TH}	MV_{REF} ± 0.31 V	V	1
V_{OUT}	0.5 × GV_{DD}	V	2

Notes:

1. Data input threshold measurement point.
2. Data output measurement point.

Figure 6 shows the DDR SDRAM output timing diagram.

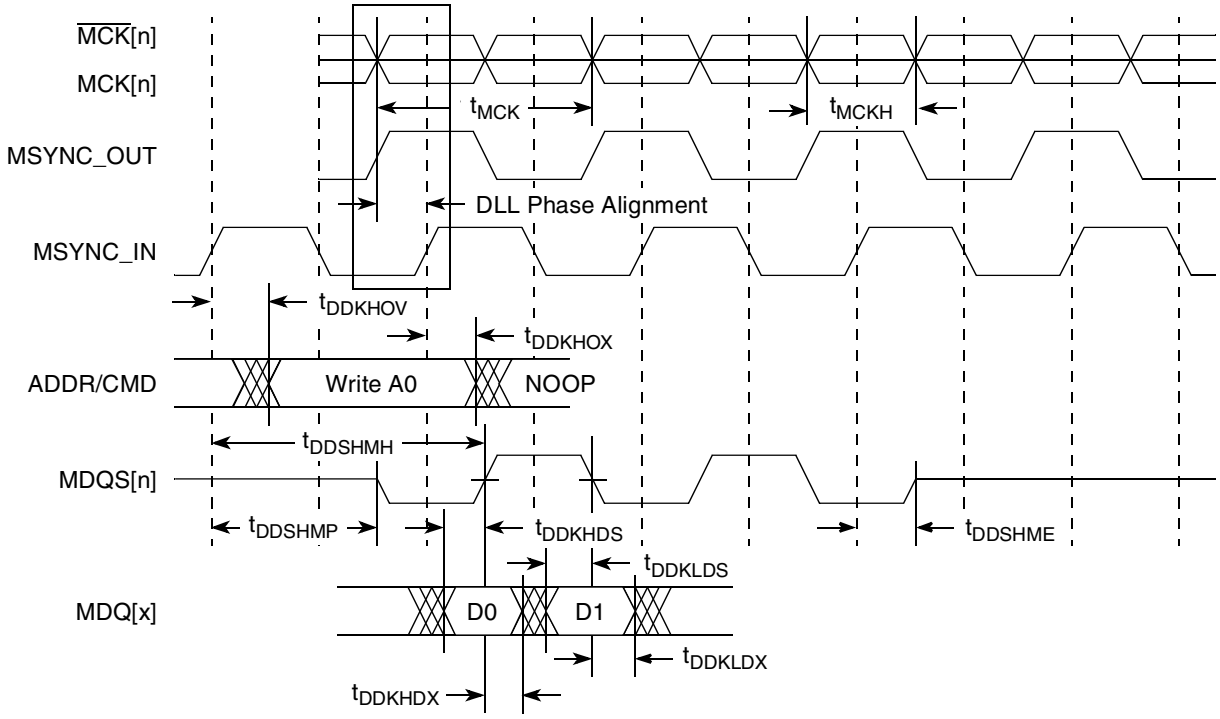


Figure 6. DDR SDRAM Output Timing Diagram

6.2.2.2 Load Effects on Address/Command Bus

Table 18 provides approximate delay information that can be expected for the address and command signals of the DDR controller for various loadings. These numbers are the result of simulations for one topology. The delay numbers will strongly depend on the topology used. These delay numbers show the total delay for the address and command to arrive at the DRAM devices. The actual delay could be different than the delays seen in simulation, depending on the system topology. If a heavily loaded system is used, the DLL loop may need to be adjusted to meet setup requirements at the DRAM.

Table 18. Expected Delays for Address/Command

Load	Delay	Unit
4 devices (12 pF)	3.0	ns
9 devices (27 pF)	3.6	ns
36 devices (108 pF) + 40 pF compensation capacitor	5.0	ns
36 devices (108 pF) + 80 pF compensation capacitor	5.2	ns

Table 22. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock rise and fall time	t_{GRXR}, t_{GRXF} [2,3]	—	—	1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 8 provides the AC test load for TSEC.

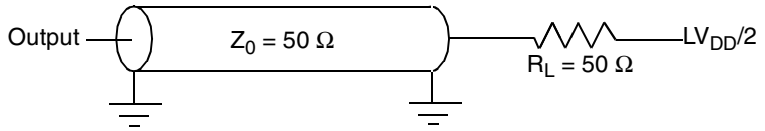


Figure 8. TSEC AC Test Load

Figure 9 shows the GMII receive AC timing diagram.

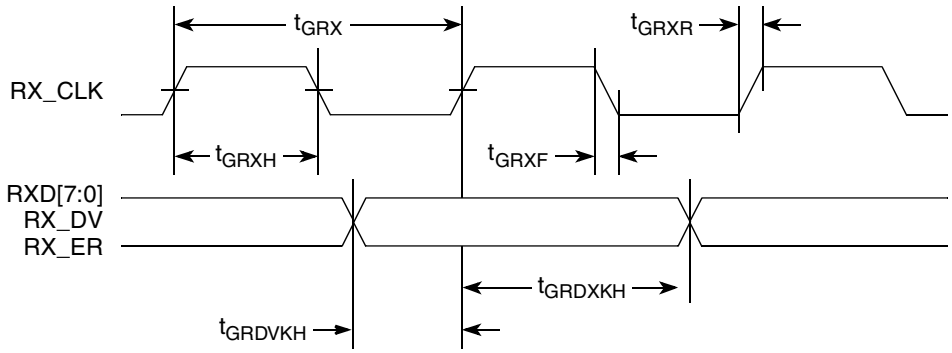


Figure 9. GMII Receive AC Timing Diagram

7.2.3.2 TBI Receive AC Timing Specifications

Table 26 provides the TBI receive AC timing specifications.

Table 26. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRX}		16.0		ns
RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising RX_CLK	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising RX_CLK	t_{TRDXKH}	1.5	—	—	ns
RX_CLK clock rise time and fall time	t_{TRXR}, t_{TRXF} [2,3]	0.7	—	2.4	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 13 shows the TBI receive AC timing diagram.

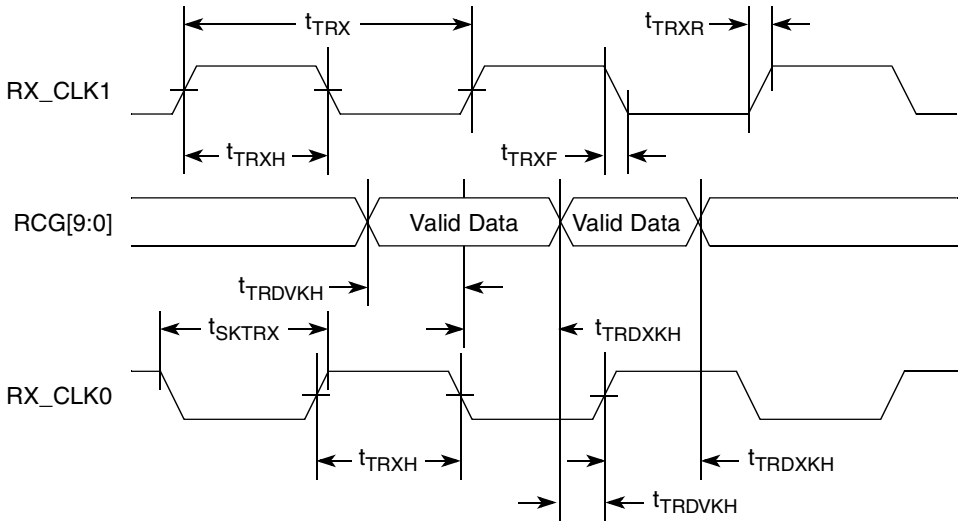


Figure 13. TBI Receive AC Timing Diagram

Table 31. Local Bus General Timing Parameters—DLL Enabled (continued)

Parameter	POR Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKHOZ2}$	—	2.5	ns	7, 9
	TSEC2_TXD[6:5] = 11 (default)			3.8		

Notes:

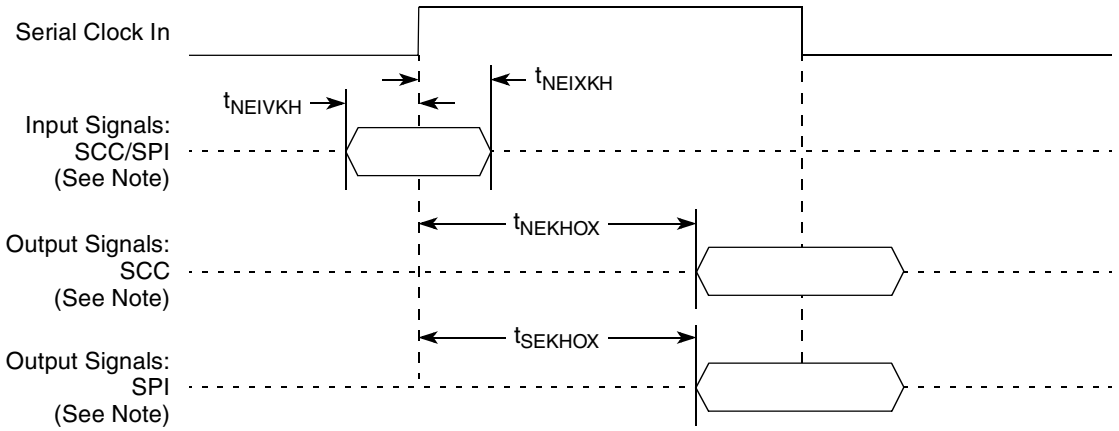
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for DLL enabled mode.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $OV_{DD}/2$.
4. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for DLL enabled to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins TSEC2_TXD[6:5].
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.
9. Guaranteed by design.

Table 32 describes the general timing parameters of the local bus interface of the MPC8560 with the DLL bypassed.

Table 32. Local Bus General Timing Parameters—DLL Bypassed

Parameter	POR Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	—	t_{LBK}	6.0	—	ns	2
Internal launch/capture clock to LCLK delay	—	t_{LBKHKT}	2.3	3.9	ns	8
LCLK[n] skew to LCLK[m] or LSYNC_OUT	—	$t_{LBKSKEW}$	—	150	ps	3, 9
Input setup to local bus clock (except LUPWAIT)	—	$t_{LBIVKH1}$	5.7	—	ns	4, 5
LUPWAIT input setup to local bus clock	—	$t_{LBIVKH2}$	5.6	—	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	—	$t_{LBIXKH1}$	-1.8	—	ns	4, 5
LUPWAIT input hold from local bus clock	—	$t_{LBIXKH2}$	-1.3	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	—	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKLOV1}$	—	-0.3	ns	4
	TSEC2_TXD[6:5] = 11 (default)			1.2		

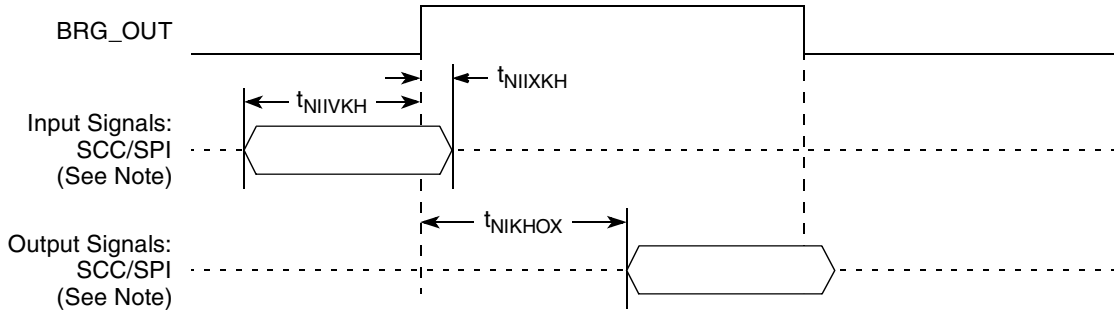
Figure 27 shows the SCC/SPI external clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 27. SCC/SPI AC Timing External Clock Diagram

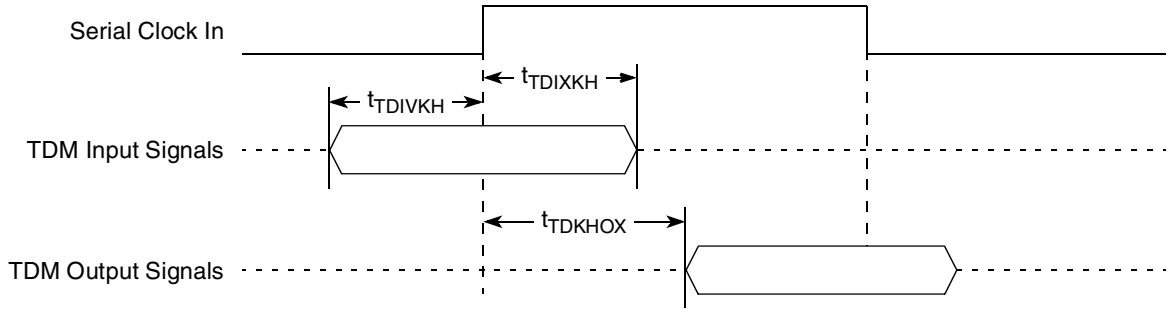
Figure 28 shows the SCC/SPI internal clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 28. SCC/SPI AC Timing Internal Clock Diagram

Figure 29 shows TDM input and output signals.



Note: There are 4 possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 29. TDM Signal AC Timing Diagram

12.2 PCI/PCI-X AC Electrical Specifications

This section describes the general AC timing parameters of the PCI/PCI-X bus of the MPC8560. Note that the SYSCLK signal is used as the PCI input clock. Table 43 provides the PCI AC timing specifications at 66 MHz.

Table 43. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol [1]	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from SYSCLK	t_{PCKHOX}	2.0	—	ns	2, 9
SYSCLK to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3, 10
Input setup to SYSCLK	t_{PCIVKH}	3.0	—	ns	2, 4, 9
Input hold from SYSCLK	t_{PCIXKH}	0	—	ns	2, 4, 9
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ [9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	5, 6, 10
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	6, 10
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	7, 10

Notes:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI/PCI-X timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI/PCI-X timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 15, "Clocking."
6. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
7. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
8. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 µs.
9. Guaranteed by characterization.
10. Guaranteed by design.

Table 44. PCI-X AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	—	clocks	11
$\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time	t_{PCRHIX}	0	50	ns	6, 11

Notes:

1.See the timing measurement conditions in the *PCI-X 1.0a Specification*.

2.Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.

3.Setup time for point-to-point signals applies to $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ only. All other signals are bused.

4.For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

5.Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.

6.Maximum value is also limited by delay to the first transaction (time for $\overline{\text{HRESET}}$ high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of $\overline{\text{HRESET}}$ must be negated no later than two clocks before the first $\overline{\text{FRAME}}$ and must be floated no later than one clock before $\overline{\text{FRAME}}$ is asserted.

7.A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.

8.Device must meet this specification independent of how many outputs switch simultaneously.

9.The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*

10.Guaranteed by characterization.

11.Guaranteed by design.

Table 45 provides the PCI-X AC timing specifications at 133 MHz.

Table 45. PCI-X AC Timing Specifications at 133 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	—	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t_{PCKHOX}	0.7	—	ns	1, 11
SYSCLK to output high impedance	t_{PCKHOZ}	—	7	ns	1, 4, 8, 12
Input setup time to SYSCLK	t_{PCIVKH}	1.4	—	ns	3, 5, 9, 11
Input hold time from SYSCLK	t_{PCIXKH}	0.5	—	ns	11
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time	t_{PCRVRH}	10	—	clocks	12
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	12
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	10, 12
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	—	clocks	12

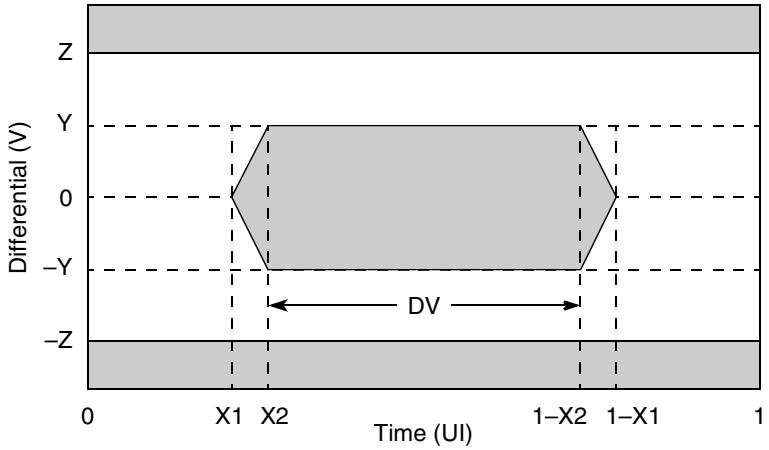


Figure 43. Example Compliance Mask

Y = minimum data valid amplitude

Z = maximum amplitude

1 UI = 1 unit interval = 1/baud rate

X1 = end of zero crossing region

X2 = beginning of data valid window

DV = data valid window = $1 - 2 \times X2$

The waveform of the signal under test must fall within the unshaded area of the mask to be compliant. Different masks are used for the driver output and the receiver input allowing each to be separately specified.

13.3.1 RapidIO Driver AC Timing Specifications

Driver AC timing specifications are provided in Table 48, Table 49, and Table 50. A driver shall comply with the specifications for each data rate/frequency for which operation of the driver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The output of a driver shall be connected to a 100 Ω, ±1%, differential (bridged) resistive load.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7]).

Table 48. RapidIO Driver AC Timing Specifications—500 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential output high voltage	V_{OHD}	200	540	mV	1
Differential output low voltage	V_{OLD}	–540	–200	mV	1

Figure 48 shows the definitions of the data to clock static skew parameter $t_{SKEW,PAIR}$ and the data valid window parameter DV. The data and frame bits are those that are associated with the clock. The figure applies for all zero-crossings of the clock. All of the signals are differential signals. V_D represents V_{OD} for the transmitter and V_{ID} for the receiver. The center of the eye is defined as the midpoint of the region in which the magnitude of the signal voltage is greater than or equal to the minimum DV voltage.

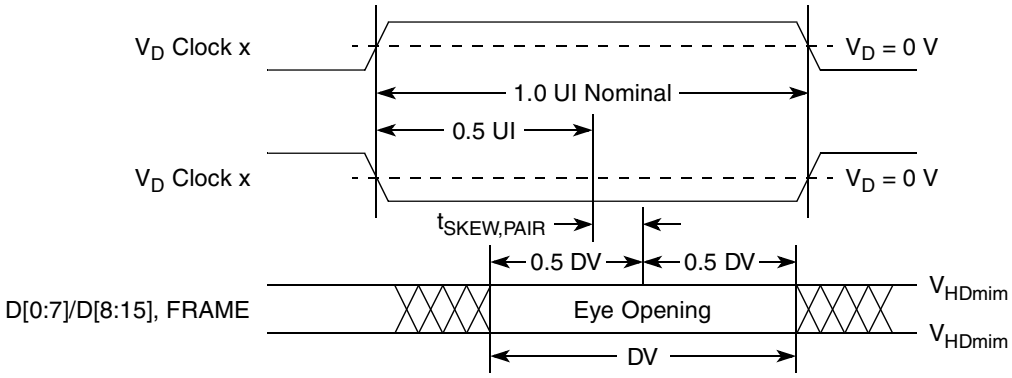


Figure 48. Data to Clock Skew

Figure 49 shows the definition of the data to data static skew parameter t_{DPAIR} and how the skew parameters are applied.

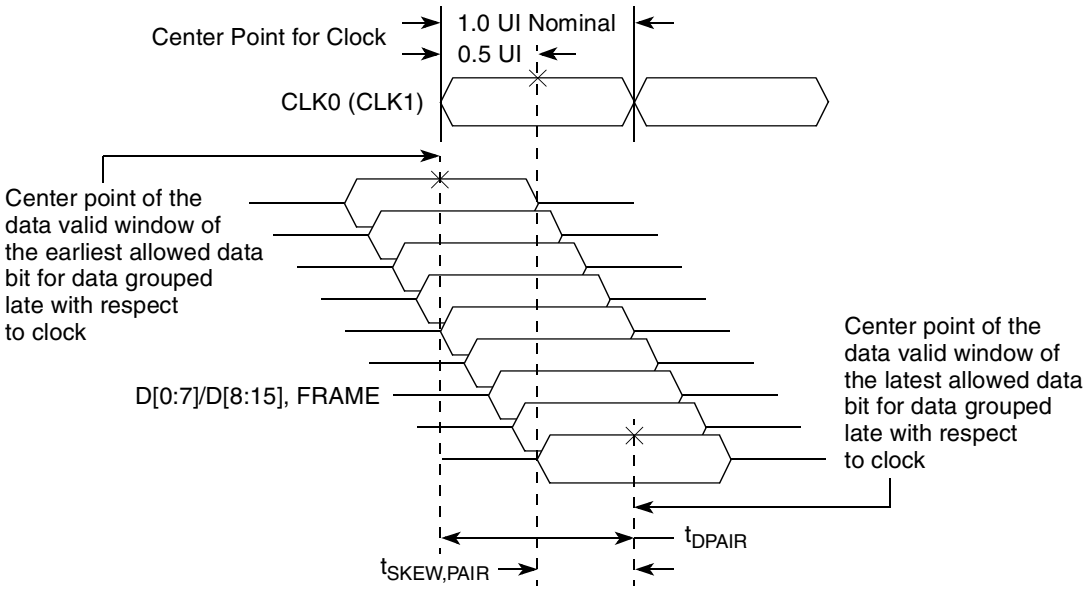


Figure 49. Static Skew Diagram

3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
7. The socket lid must always be oriented to A1.

14.3 Pinout Listings

Table 54 provides the pin-out listing for the MPC8560, 783 FC-PBGA package.

Table 54. MPC8560 Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI/PCI-X				
PCI_AD[63:0]	AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14, V15, W15, Y15, AA15, AB15, AC15, AD15, AG15, AH15, V16, W16, AB16, AC16, AD16, AE16, AF16, V17, W17, Y17, AA17, AB17, AE17, AF17, AF18, AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9, AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11, AG11, AH11, V12, W12, Y12, AB12, AD12, AE12, AG12, AH12, V13, Y13, AB13, AC13	I/O	OV_{DD}	17
PCI_C_$\overline{BE}$[7:0]	AG13, AH13, V14, W14, AH8, AB10, AD11, AC12	I/O	OV_{DD}	17
PCI_PAR	AA11	I/O	OV_{DD}	—
PCI_PAR64	Y14	I/O	OV_{DD}	—
$\overline{\text{PCI\_FRAME}}$	AC10	I/O	OV_{DD}	2
$\overline{\text{PCI\_TRDY}}$	AG10	I/O	OV_{DD}	2
$\overline{\text{PCI\_IRDY}}$	AD10	I/O	OV_{DD}	2
$\overline{\text{PCI\_STOP}}$	V11	I/O	OV_{DD}	2
$\overline{\text{PCI\_DEVSEL}}$	AH10	I/O	OV_{DD}	2
PCI_IDSEL	AA9	I	OV_{DD}	—
$\overline{\text{PCI\_REQ64}}$	AE13	I/O	OV_{DD}	5, 10
$\overline{\text{PCI\_ACK64}}$	AD13	I/O	OV_{DD}	2
$\overline{\text{PCI\_PERR}}$	W11	I/O	OV_{DD}	2
$\overline{\text{PCI\_SERR}}$	Y11	I/O	OV_{DD}	2, 4
$\overline{\text{PCI\_REQ0}}$	AF5	I/O	OV_{DD}	—
$\overline{\text{PCI\_REQ}}$[1:4]	AF3, AE4, AG4, AE5	I	OV_{DD}	—
$\overline{\text{PCI\_GNT}}$[0]	AE6	I/O	OV_{DD}	—
$\overline{\text{PCI\_GNT}}$[1:4]	AG5, AH5, AF6, AG6	O	OV_{DD}	5, 9

Table 54. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface				
MDQ[0:63]	M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12	I/O	GV_{DD}	—
MECC[0:7]	N20, M20, L19, E19, C21, A21, G19, A19	I/O	GV_{DD}	—
MDM[0:8]	L24, H28, F24, L21, E18, E16, G14, B13, M19	O	GV_{DD}	—
MDQS[0:8]	L26, J25, D25, A22, H18, F16, F14, C13, C20	I/O	GV_{DD}	—
MBA[0:1]	B18, B19	O	GV_{DD}	—
MA[0:14]	N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13	O	GV_{DD}	—
$\overline{\text{MWE}}$	D17	O	GV_{DD}	—
$\overline{\text{MRAS}}$	F17	O	GV_{DD}	—
$\overline{\text{MCAS}}$	J16	O	GV_{DD}	—
$\overline{\text{MCS}}$[0:3]	H16, G16, J15, H15	O	GV_{DD}	—
MCKE[0:1]	E26, E28	O	GV_{DD}	11
MCK[0:5]	J20, H25, A15, D20, F28, K14	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	F20, G27, B15, E20, F27, L14	O	GV_{DD}	—
MSYNC_IN	M28	I	GV_{DD}	—
MSYNC_OUT	N28	O	GV_{DD}	—
Local Bus Controller Interface				
LA[27]	U18	O	OV_{DD}	5, 9
LA[28:31]	T18, T19, T20, T21	O	OV_{DD}	7, 9
LAD[0:31]	AD26, AD27, AD28, AC26, AC27, AC28, AA22, AA23, AA26, Y21, Y22, Y26, W20, W22, W26, V19, T22, R24, R23, R22, R21, R18, P26, P25, P20, P19, P18, N22, N23, N24, N25, N26	I/O	OV_{DD}	—
LALE	V21	O	OV_{DD}	8, 9
LBCTL	V20	O	OV_{DD}	9
LCKE	U23	O	OV_{DD}	—
LCLK[0:2]	U27, U28, V18	O	OV_{DD}	—
$\overline{\text{LCS}}$[0:4]	Y27, Y28, W27, W28, R27	O	OV_{DD}	18
$\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$	R28	I/O	OV_{DD}	1

18 Document Revision History

Table 62 provides a revision history for this hardware specification.

Table 62. Document Revision History

Rev. No.	Substantive Change(s)
4.2	Added “Note: Rise/Fall Time on CPM Input Pins” and following note text to Section 9.2, “CPM AC Timing Specifications.”
4.1	Inserted Figure 3 and paragraph above it. Added PCI/PCI-X row to Input Voltage characteristic and added footnote 6 to Table 1.
4	Updated Section 2.1.2, “Power Sequencing.” Updated back page information.
3.5	Updated Section 2.1.2, “Power Sequencing.”
3.4	Updated MV_{REF} Max Value in Table 1. Updated MV_{REF} Max Value in Table 2. Added new revision level information to Table 63
3.3	Updated MV_{REF} Max Value in Table 1. Removed Figure 3. In Table 4, replaced TBD with power numbers and added footnote. Updated specs and footnotes in Table 8. Corrected max number for MV_{REF} in Table 13. Changed parameter “Clock cycle duration” to “Clock period” in Table 27. Added note 4 to $t_{LBKHOV1}$ and removed LALE reference from $t_{LBKHOV3}$ in Table 31 and Table 32. Updated LALE signal in Figure 17 and Figure 18. Modified Figure 21. Modified Figure 61.

Table 62. Document Revision History (continued)

Rev. No.	Substantive Change(s)
3.2	Updated Table 1 and Table 2 with 1.0 GHz device parameter requirements. Added Section 2.1.2, “Power Sequencing”. Added CPM port signal drive strength to Table 3. Updated Table 4 with Maximum power data. Updated Table 4 and Table 5 with 1 GHz speed grade information. Updated Table 6 with corrected typical I/O power numbers. Updated Table 7 Note 2 lower voltage measurement point. Replaced Table 7 Note 5 with spread spectrum clocking guidelines. Added to Table 8 rise and fall time information. Added Section 4.4, “Real Time Clock Timing”. Added precharge information to Section 6.2.2, “DDR SDRAM Output AC Timing Specifications”. Removed V_{IL} and V_{IH} references from Table 21, Table 22, Table 23, and Table 24. Added reference level note to Table 21, Table 22, Table 23, Table 24, Table 25, Table 26, and Table 27. Updated TXD references to TCG in Section 7.2.3.1, “TBI Transmit AC Timing Specifications”. Updated t_{TTKHDX} value in Table 25. Updated PMA_RX_CLK references to RX_CLK in Section 7.2.3.2, “TBI Receive AC Timing Specifications”. Updated RXD references to RCG in Section 7.2.3.2, “TBI Receive AC Timing Specifications”. Updated Table 27 Note 2. Corrected Table 29 f_{MDC} and t_{MDC} to reflect the correct minimum operating frequency. Updated Table 29 t_{MDKHDV} and t_{MDKHDX} values for clarification. Added t_{LBKHKT} and updated Note 2 in Table 32. Corrected $\overline{\text{LGTA}}$ timing references in Figure 17. Updated Figure 18, Figure 20, and Figure 22. Corrected FCC output timing reference labels in Figure 24 and Figure 25. Updated Figure 50. Clarified Table 54 Note 5. Updated Table 55 and Table 56 with 1 GHz information. Added heat sink removal discussion to Section 16.2.3, “Thermal Interface Materials”. Corrected and added 1 GHz part number to Table 63.
3.1	Updated Table 4 and Table 5. Added Table 6. Added MCK duty cycle to Table 16. Updated f_{MDC}, t_{MDC}, t_{MDKHDV}, and t_{MDKHDX} parameters in Table 29. Added LALE to $t_{LBKHOV3}$ parameter in Table 31 and Table 32, and updated Figure 17. Corrected active level designations of some of the pins in Table 54. Updated Table 63.

Table 62. Document Revision History (continued)

Rev. No.	Substantive Change(s)
3.0	Table 1—Corrected MII management voltage reference Section 2.1.3—New Table 2—Corrected MII management voltage reference Table 5—Removed 'minimum' column Table 5—Added AV_{DD} power table Table 8—New Table 9—New Table 9—New Table 13—Added overshoot/undershoot note. Figure 4—New Table 16—Restated $t_{MCKSKEW1}$ as $t_{MCKSKEW}$, removed $t_{MCKSKEW2}$; added speed-specific minimum values for 333, 266, and 200 MHz; updated t_{DDSHME} values. Updated chapter to reflect that GMII, MII and TBI can be run with 2.5V signalling. Table 29—Added MDIO output valid timing Table 31—Updated $t_{LBIVKH1}$, $t_{LBIXKH1}$, and t_{LBOTOT}. Table 32—New Figure 20, Figure 22—Updated clock reference Table 34—Updated t_{TDIVKH} Table 35—Updated t_{TDKHOX} Added tables and figures for CPM I^2C Table 45—Updated t_{PCIVKH} Section 14.1— Changed minimum height from 2.22 to 3.07 and maximum from 2.76 to 3.75 Table 54.—Updated MII management voltage reference and added note 20. Section 16.2.4.1—Changed θ_{JC} from 0.3 to 0.8; changed die-junction temperature from 67° to 71° Section 17.7—Added paragraph that begins "TSEC1_TXD[3:0]..."
2.1	Section 2.1.3—New Table 16—Added speed-specific minimum values for 333, 266, and 200 MHz Table 31—Replaced all references to TSEC1_TXD[6:5] to TSEC2_TXD[6:5] Table 31—Added t_{LBSKEW} and note 3 Table 31—Added comment about rev. 2.x devices to note 5 Section 14.1— Changed minimum height from 2.22 to 3.07 and maximum from 2.76 to 3.75 Section 16.2.4.1—Changed θ_{JC} from 0.3 to 0.8; changed die-junction temperature from 67° to 71° Section 17.7—Added paragraph that begins "TSEC1_TXD[3:0]..."

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