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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	-
Number of Cores/Bus Width	-
Speed	-
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8560cvt667jc

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic		Symbol	Max Value	Unit	Notes
DDR DRAM I/O voltage		GV_{DD}	–0.3 to 3.63	V	—
Three-speed Ethernet I/O voltage		LV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	—
CPM, PCI/PCI-X, local bus, RapidIO, 10/100 Ethernet,MII management, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	3
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	4, 5
	CPM, Local bus, RapidIO, 10/100 Ethernet, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	5
	PCI/PCI-X	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

2.1.2 Power Sequencing

The MPC8560 requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD}, AV_{DD}
2. GV_{DD}, LV_{DD}, OV_{DD} (I/O supplies)

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90 percent of their value before the voltage rails on the current step reach 10 percent of theirs.

Table 22. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock rise and fall time	t_{GRXR}, t_{GRXF} [2,3]	—	—	1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 8 provides the AC test load for TSEC.

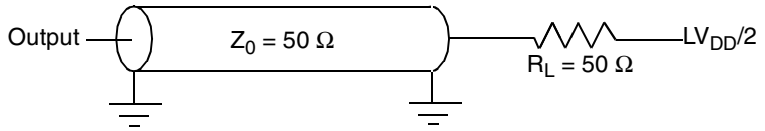


Figure 8. TSEC AC Test Load

Figure 9 shows the GMII receive AC timing diagram.

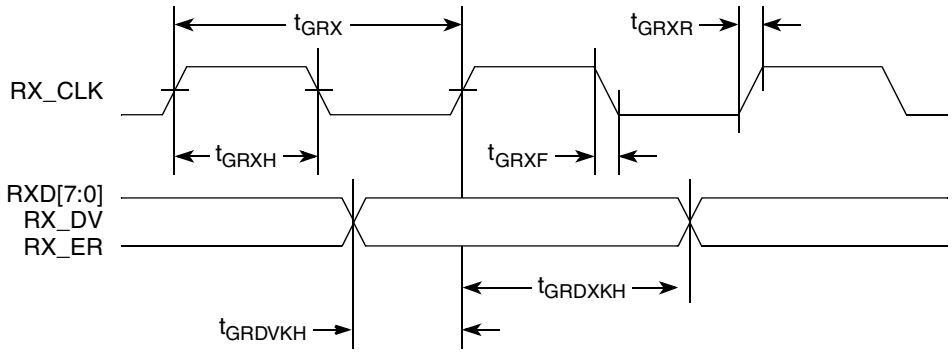


Figure 9. GMII Receive AC Timing Diagram

Table 28. MII Management DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit
Input high current (OV_{DD} = Max, V_{IN} [1] = 2.1 V)	I_{IH}	—	40	μA
Input low current (OV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA

Note:

1.Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.3.2 MII Management AC Electrical Specifications

Table 29 provides the MII management AC timing specifications.

Table 29. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	0.893	—	10.4	MHz	2, 4
MDC period	t_{MDC}	96	—	1120	ns	
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	
MDC to MDIO valid	t_{MDKHDV}			$2*[1/(f_{ccb\_clk}/8)]$	ns	3
MDC to MDIO delay	t_{MDKHDX}	10	—	$2*[1/(f_{ccb\_clk}/8)]$	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	
MDC rise time	t_{MDCR}	—	—	10	ns	4
MDC fall time	t_{MDHF}	—	—	10	ns	4

Notes:

1.The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2.This parameter is dependent on the CCB clock speed (that is, for a CCB clock of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a CCB clock of 333 MHz, the maximum frequency is 10.4 MHz and the minimum frequency is 1.5 MHz).

3.This parameter is dependent on the CCB clock speed (that is, for a CCB clock of 267 MHz, the delay is 60 ns and for a CCB clock of 333 MHz, the delay is 48 ns).

4.Guaranteed by design.

Figure 16 provides the AC test load for the local bus.

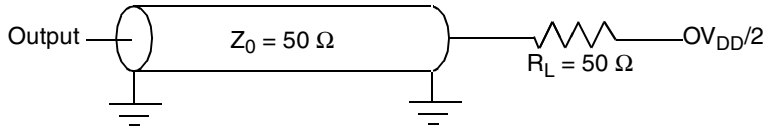


Figure 16. Local Bus AC Test Load

Figure 17 through Figure 22 show the local bus signals.

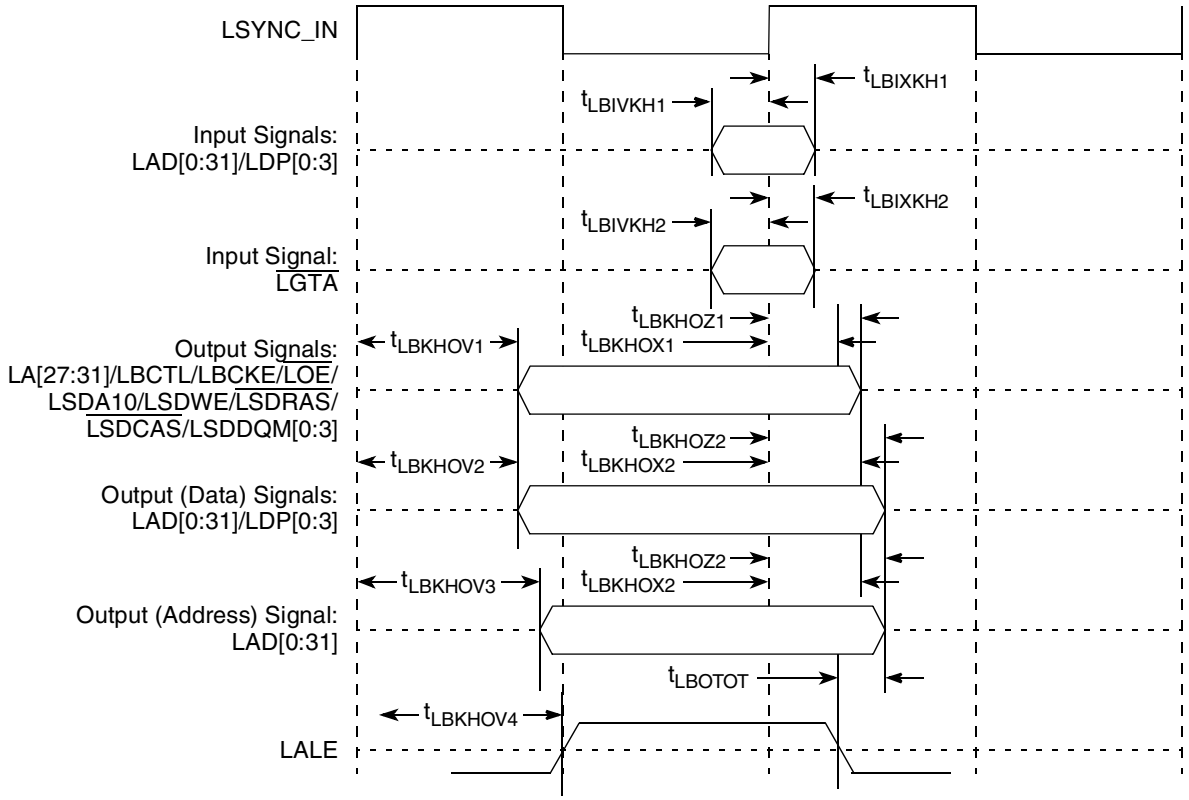


Figure 17. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

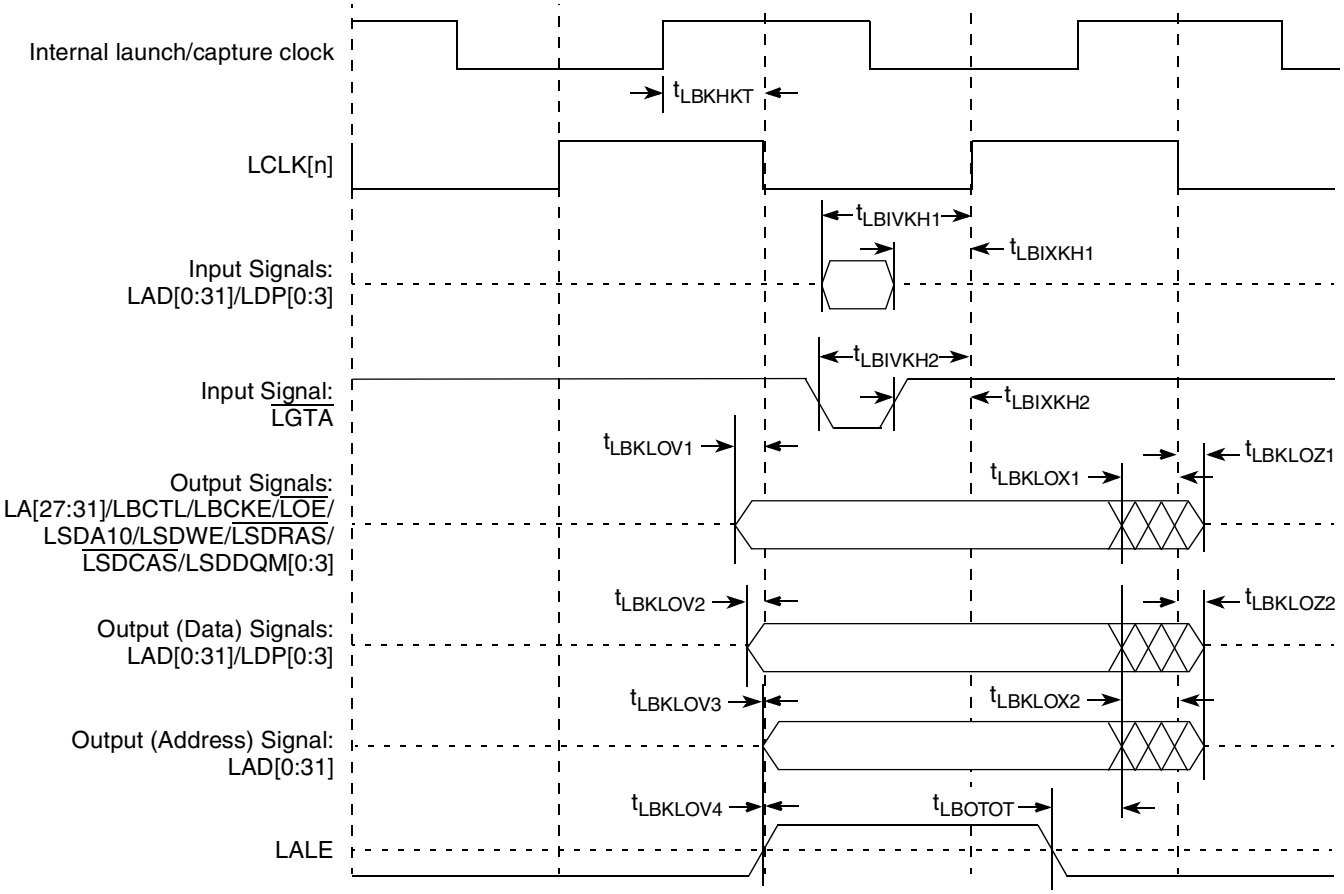


Figure 18. Local Bus Signals (DLL Bypass Mode)

Table 33. CPM DC Electrical Characteristics (continued)

Characteristic	Symbol	Min	Max	Unit	Notes
Output high voltage (I_{OH} = –2.0 mA)	V_{OH}	2.4	—	V	1
Output low voltage (I_{OL} = 3.2 mA)	V_{OL}	—	0.4	V	1

Note:
1. This specification applies to the following pins: PA[0–31], PB[4–31], PC[0–31], and PD[4–31].
2. V_{IL}(max) for the IIC interface is 0.8 V rather than the 1.5 V specified in the IIC standard

9.2 CPM AC Timing Specifications

Table 34 and Table 35 provide the CPM input and output AC timing specifications, respectively.

NOTE: Rise/Fall Time on CPM Input Pins

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

Table 34. CPM Input AC Timing Specifications [1]

Characteristic	Symbol [2]	Min [3]	Unit
FCC inputs—internal clock (NMSI) input setup time	t_{FIIVKH}	6	ns
FCC inputs—internal clock (NMSI) hold time	t_{FIIXKH}	0	ns
FCC inputs—external clock (NMSI) input setup time	t_{FEIVKH}	2.5	ns
FCC inputs—external clock (NMSI) hold time	t_{FEIXKH}b	2	ns
SCC/SPI inputs—internal clock (NMSI) input setup time	t_{NIIVKH}	6	ns
SCC/SPI inputs—internal clock (NMSI) input hold time	t_{NIIXKH}	0	ns
SCC/SPI inputs—external clock (NMSI) input setup time	t_{NEIVKH}	4	ns
SCC/SPI inputs—external clock (NMSI) input hold time	t_{NEIXKH}	2	ns
TDM inputs/SI—input setup time	t_{TDIVKH}	4	ns
TDM inputs/SI—hold time	t_{TDIXKH}	3	ns

Table 36 shows CPM I^{2}C AC Timing.

Table 36. CPM I^{2}C AC Timing

Characteristic	Symbol	Min	Max	Unit
SCL clock frequency (slave)	f_{SCL}	0	F_{MAX}[1]	Hz
SCL clock frequency (master)	f_{SCL}	BRGCLK/16512	BRGCLK/48	Hz
Bus free time between transmissions	t_{SDHDL}	1/(2.2 * f_{SCL})	—	s
Low period of SCL	t_{SCLCH}	1/(2.2 * f_{SCL})	—	s
High period of SCL	t_{SCHCL}	1/(2.2 * f_{SCL})	—	s
Start condition setup time [2]	t_{SCHDL}	2/(divider * f_{SCL})	—	s
Start condition hold time [2]	t_{SDLCL}	3/(divider * f_{SCL})	—	s
Data hold time [2]	t_{SCLDX}	2/(divider * f_{SCL})	—	s
Data setup time [2]	t_{SDVCH}	3/(divider * f_{SCL})	—	s
SDA/SCL rise time	t_{SRISE}	—	1/(10 * f_{SCL})	s
SDA/SCL fall time	t_{SFALL}	—	1/(33 * f_{SCL})	s
Stop condition setup time	t_{SCHDH}	2/(divider * f_{SCL})	—	s

Notes:

1. F_{MAX} = BRGCLK/(min_divider*prescaler). Where prescaler=25-I2MODE[PDIV]; and min_divider=12 if digital filter disabled and 18 if enabled.
   Example #1: if I2MODE[PDIV]=11 (prescaler=4) and I2MODE[FLT]=0 (digital filter disabled) then FMAX=BRGCLK/48
   Example #2: if I2MODE[PDIV]=00 (prescaler=32) and I2MODE[FLT]=1 (digital filter enabled) then FMAX=BRGCLK/576
2. divider = f_{SCL}/prescaler.
   In master mode: divider = BRGCLK/(f_{SCL}*prescaler) = 2*(I2BRG[DIV]+3)
   In slave mode: divider = BRGCLK/(f_{SCL}*prescaler)

Figure 30 is a a diagram of CPM I^{2}C Bus Timing.

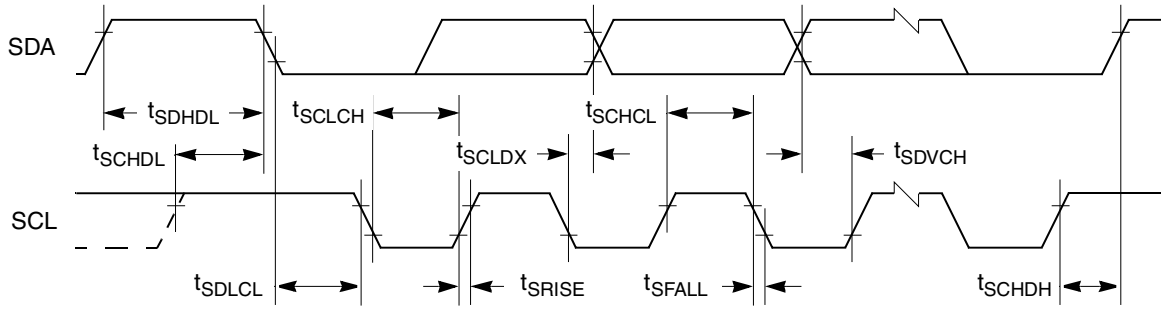


Figure 30. CPM I^{2}C Bus Timing Diagram

Figure 31 provides the AC test load for TDO and the boundary-scan outputs of the MPC8560.

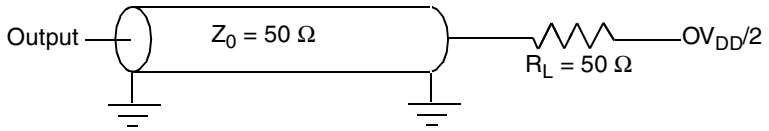


Figure 31. AC Test Load for the JTAG Interface

Figure 32 provides the JTAG clock input timing diagram.

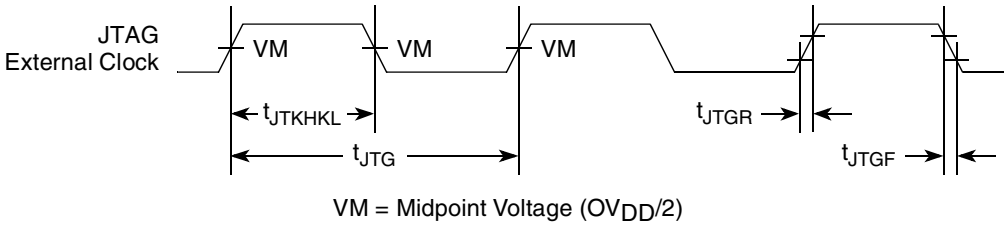


Figure 32. JTAG Clock Input Timing Diagram

Figure 33 provides the $\overline{\text{TRST}}$ timing diagram.

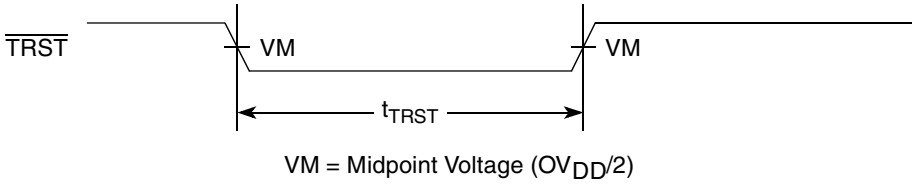


Figure 33. $\overline{\text{TRST}}$ Timing Diagram

Figure 34 provides the boundary-scan timing diagram.

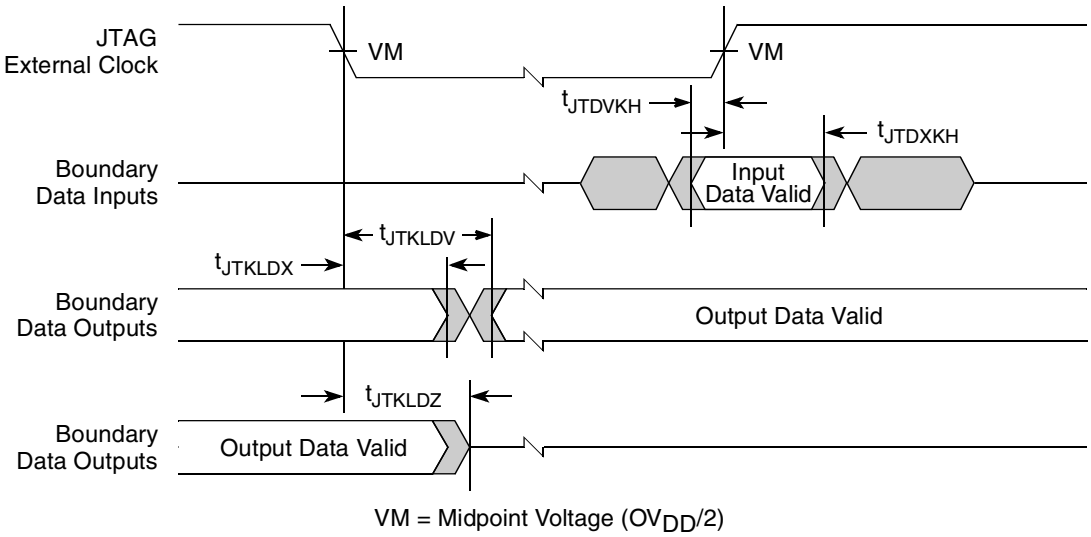


Figure 34. Boundary-Scan Timing Diagram

11.2 I²C AC Electrical Specifications

Table 41 provides the AC timing parameters for the I²C interface of the MPC8560.

Table 41. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 40).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} [6]	1.3	—	μs
High period of the SCL clock	t_{I2CH} [6]	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH} [6]	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} [6]	0.6	—	μs
Data setup time	t_{I2DVKH} [6]	100	—	ns
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	— 0 [2]	— 0.9 [3]	μs
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8560 provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
6. Guaranteed by design.

Figure 16 provides the AC test load for the I²C.

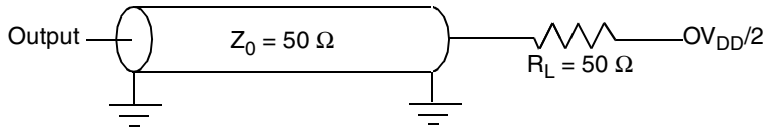


Figure 36. I²C AC Test Load

- The peak differential signal of the transmitter output or receiver input, is A – B volts.
- The peak-to-peak differential signal of the transmitter output or receiver input, is 2 × (A – B) volts.

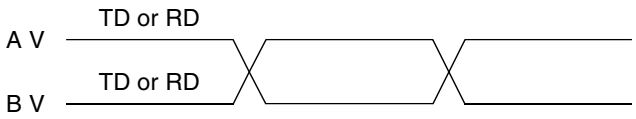


Figure 42. Differential Peak-to-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using numerical values, consider the case where a LVDS transmitter has a common mode voltage of 1.2 V and each signal has a swing that goes between 1.4 and 1.0 V. Using these values, the peak-to-peak voltage swing of the signals TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ is 400 mV. The differential signal ranges between 400 and –400 mV. The peak differential signal is 400 mV, and the peak-to-peak differential signal is 800 mV.

A timing edge is the zero-crossing of a differential signal. Each skew timing parameter on a parallel bus is synchronously measured on two signals relative to each other in the same cycle, such as data to data, data to clock, or clock to clock. A skew timing parameter may be relative to the edge of a signal or to the middle of two sequential edges.

Static skew represents the timing difference between signals that does not vary over time regardless of system activity or data pattern. Path length differences are a primary source of static skew.

Dynamic skew represents the amount of timing difference between signals that is dependent on the activity of other signals and varies over time. Crosstalk between signals is a source of dynamic skew.

Eye diagrams and compliance masks are a useful way to visualize and specify driver and receiver performance. This technique is used in several serial bus specifications. An example compliance mask is shown in Figure 43. The key difference in the application of this technique for a parallel bus is that the data is source synchronous to its bus clock while serial data is referenced to its embedded clock. Eye diagrams reveal the quality (cleanness, openness, goodness) of a driver output or receiver input. An advantage of using an eye diagram and a compliance mask is that it allows specifying the quality of a signal without requiring separate specifications for effects such as rise time, duty cycle distortion, data dependent dynamic skew, random dynamic skew, etc. This allows the individual semiconductor manufacturer maximum flexibility to trade off various performance criteria while keeping the system performance constant.

In using the eye pattern and compliance mask approach, the quality of the signal is specified by the compliance mask. The mask specifies the maximum permissible magnitude of the signal and the minimum permissible eye opening. The eye diagram for the signal under test is generated according to the specification. Compliance is determined by whether the compliance mask can be positioned over the eye diagram such that the eye pattern falls entirely within the unshaded portion of the mask.

Serial specifications have clock encoded with the data, but the LP-LVDS physical layer defined by RapidIO is a source synchronous parallel port so additional specifications to include effects that are not found in serial links are required. Specifications for the effect of bit to bit timing differences caused by static skew have been added and the eye diagrams specified are measured relative to the associated clock in order to include clock to data effects. With the transmit output (or receiver input) eye diagram, the user can determine if the transmitter output (or receiver input) is compliant with an oscilloscope with the appropriate software.

Table 53. RapidIO Receiver AC Timing Specifications—1 Gbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1, 5
Data valid	DV	425	—	ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}	—	300	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–200	200	ps	4

Notes:

1.Measured at V_{ID} = 0 V.

2.Measured using the RapidIO receive mask shown in Figure 46.

3.See Figure 49.

4.See Figure 48 and Figure 49.

5.Guaranteed by design.

The compliance of receiver input signals RD[0:15] and RFRAME with their minimum data valid window (DV) specification shall be determined by generating an eye pattern for each of the data signals and comparing the eye pattern of each data signal with the RapidIO receive mask shown in Figure 46. The value of X2 used to construct the mask shall be $(1 – DV_{min})/2$. The ±100 mV minimum data valid and ±600 mV maximum input voltage values are from the DC specification. A signal is compliant with the data valid window specification if and only if the receive mask can be positioned on the signal's eye pattern such that the eye pattern falls entirely within the unshaded portion of the mask.

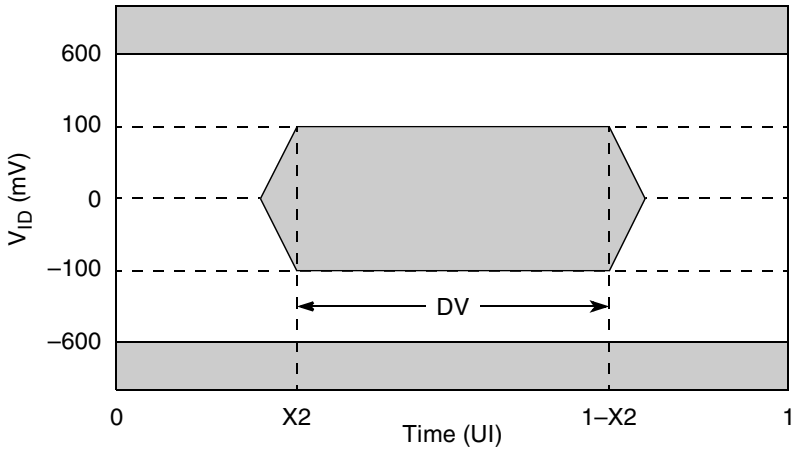


Figure 46. RapidIO Receive Mask

The eye pattern for a data signal is generated by making a large number of recordings of the signal and then overlaying the recordings. The number of recordings used to generate the eye shall be large enough that further increasing the number of recordings used does not cause the resulting eye pattern to change from one that complies with the RapidIO receive mask to one that does not. Each data signal in the interface shall be carrying random or pseudo-random data when the recordings are made. If pseudo-random data is used, the length of the pseudo-random sequence (repeat length) shall be long

enough that increasing the length of the sequence does not cause the resulting eye pattern to change from one that complies with the RapidIO receive mask to one that does not comply with the mask. The data carried by any given data signal in the interface may not be correlated with the data carried by any other data signal in the interface. The zero-crossings of the clock associated with a data signal shall be used as the timing reference for aligning the multiple recordings of the data signal when the recordings are overlaid.

While the method used to make the recordings and overlay them to form the eye pattern is not specified, the method used shall be demonstrably equivalent to the following method. The signal under test is repeatedly recorded with a digital oscilloscope in infinite persistence mode. Each recording is triggered by a zero-crossing of the clock associated with the data signal under test. Roughly half of the recordings are triggered by positive-going clock zero-crossings and roughly half are triggered by negative-going clock zero-crossings. Each recording is at least 1.9 UI in length (to ensure that at least one complete eye is formed) and begins 0.5 UI before the trigger point (0.5 UI before the associated clock zero-crossing). Depending on the length of the individual recordings used to generate the eye pattern, one or more complete eyes will be formed. Regardless of the number of eyes, the eye whose center is immediately to the right of the trigger point is the eye used for compliance testing.

An example of an eye pattern generated using the above method with recordings 3 UI in length is shown in Figure 47. In this example, there is no skew between the signal under test and the associated clock used to trigger the recordings. If skew was present, the eye pattern would be shifted to the left or right relative to the oscilloscope trigger point.

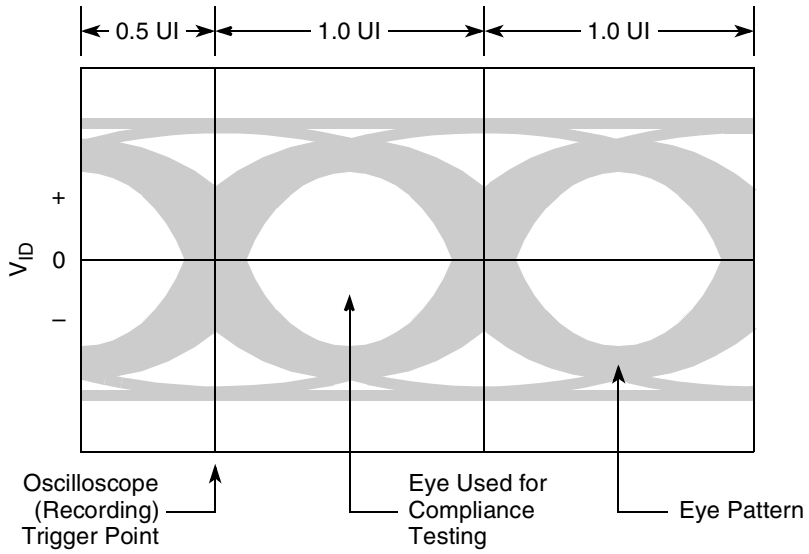


Figure 47. Example Receiver Input Eye Pattern

14.2 Mechanical Dimensions of the MPC8560 FC-PBGA

Figure 50 the mechanical dimensions and bottom surface nomenclature of the MPC8560, 783 FC-PBGA package.

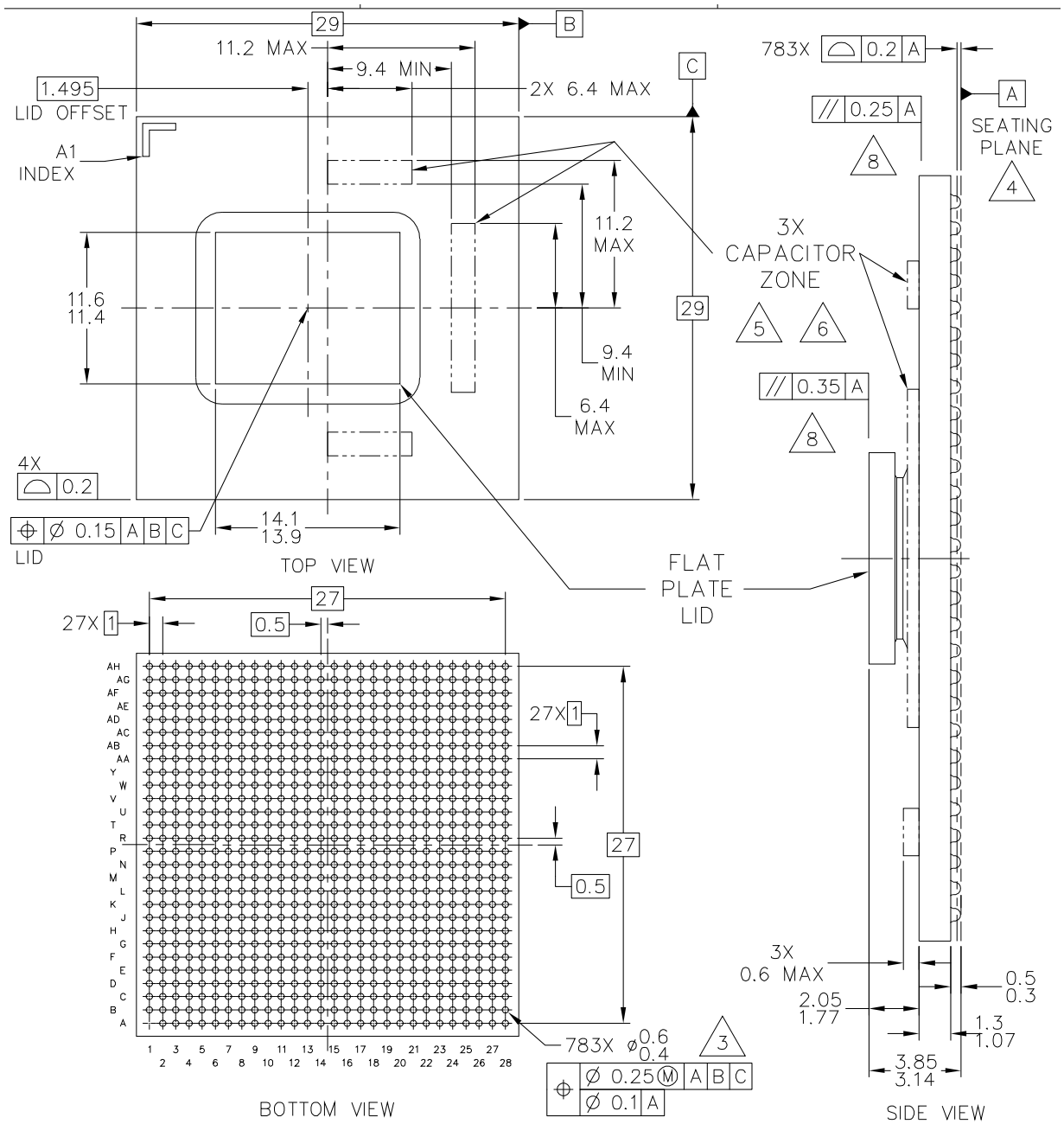


Figure 50. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8560 FC-PBGA

NOTES

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.

Table 54. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV_{DD}	A4, C5, E7, H10	Reference Voltage; Three-Speed Ethernet I/O (2.5 V, 3.3 V)	LV_{DD}	—
MV_{REF}	N27	Reference Voltage Signal; DDR	MV_{REF}	—
No Connects	AH26, AH27, AH28, AG28, AF28, AE28, AH1, AG1, AH2, B1, B2, A2, A3, AH25	—	—	16
OV_{DD}	D1, E4, H3, K4, K10, L7, M5, N3, P22, R19, R25, T2, T7, U5, U20, U26, V8, W4, W13, W19, W21, Y7, Y23, AA5, AA12, AA16, AA20, AB7, AB9, AB26, AC5, AC11, AC17, AD4, AE1, AE8, AE10, AE15, AF7, AF12, AG27, AH4	PCI/PCI-X, RapidIO, 10/100 Ethernet, and other Standard (3.3 V)	OV_{DD}	—
RESERVED	C1, T11, U11, AF1	—	—	15
SENSEVDD	L12	Power for Core (1.2 V)	V_{DD}	13
SENSEVSS	K12	—	—	13
V_{DD}	M13, M15, M17, N14, N16, P13, P15, P17, R12, R14, R16, T13, T15, T17, U12, U14	Power for Core (1.2 V)	V_{DD}	—
CPM				
PA[0:31]	H1, H2, J1, J2, J3, J4, J5, J6, J7, J8, K8, K7, K6, K3, K2, K1, L1, L2, L3, L4, L5, L8, L9, L10, L11, M10, M9, M8, M7, M6, M3, M2	I/0	OV_{DD}	—
PB[4:31]	M1, N1, N4, N5, N6, N7, N8, N9, N10, N11, P11, P10, P9, P8, P7, P6, P5, P4, P3, P2, P1, R1, R2, R3, R4, R5, R6, R7	I/0	OV_{DD}	—
PC[0:31]	R8, R9, R10, R11, T9, T6, T5, T4, T1, U1, U2, U3, U4, U7, U8, U9, U10, V9, V6, V5, V4, V3, V2, V1, W1, W2, W3, W6, W7, W8, W9, Y9	I/0	OV_{DD}	—

15.2 Platform/System PLL Ratio

The platform clock is the clock that drives the L2 cache, the DDR SDRAM data rate, and the e500 core complex bus (CCB), and is also called the CCB clock. The values are determined by the binary value on LA[28:31] at power up, as shown in Table 57.

There is no default for this PLL ratio; these signals must be pulled to the desired values.

Table 57. CCB Clock Ratio

Binary Value of LA[28:31] Signals	Ratio Description
0000	16:1 ratio CCB clock: SYSCLK (PCI bus)
0001	Reserved
0010	2:1 ratio CCB clock: SYSCLK (PCI bus)
0011	3:1 ratio CCB clock: SYSCLK (PCI bus)
0100	4:1 ratio CCB clock: SYSCLK (PCI bus)
0101	5:1 ratio CCB clock: SYSCLK (PCI bus)
0110	6:1 ratio CCB clock: SYSCLK (PCI bus)
0111	Reserved
1000	8:1 ratio CCB clock: SYSCLK (PCI bus)
1001	9:1 ratio CCB clock: SYSCLK (PCI bus)
1010	10:1 ratio CCB clock: SYSCLK (PCI bus)
1011	Reserved
1100	12:1 ratio CCB clock: SYSCLK (PCI bus)
1101	Reserved
1110	Reserved
1111	Reserved

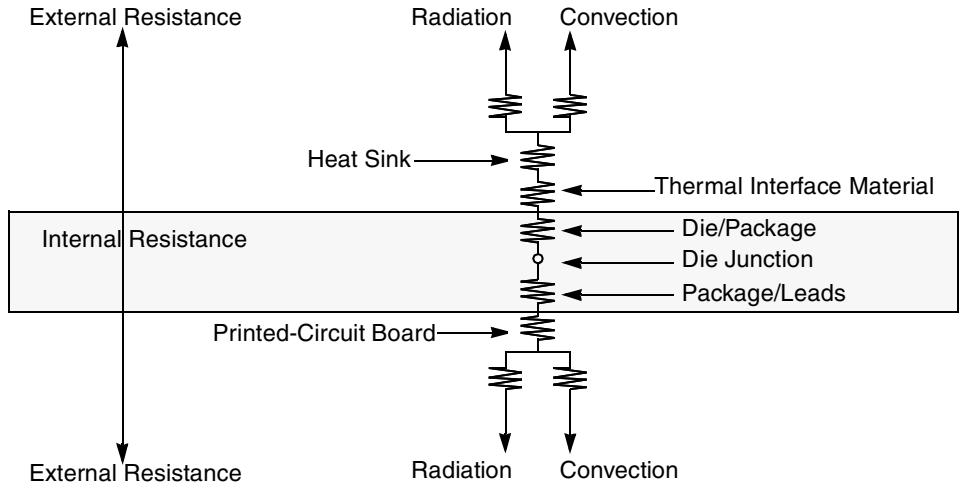
15.3 e500 Core PLL Ratio

Table 58 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LALE and LGPL2 at power up, as shown in Table 58.

Table 58. e500 Core to CCB Ratio

Binary Value of LALE, LGPL2 Signals	Ratio Description
00	2:1 e500 core:CCB
01	5:2 e500 core:CCB
10	3:1 e500 core:CCB
11	7:2 e500 core:CCB

Figure 53 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 53. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

16.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 54 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 51). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink, the heat sink should be slowly removed. Heating the heat sink to 40-50°C with an air gun can soften the interface material and make the removal easier. The use of an adhesive for heat sink attach is not recommended.

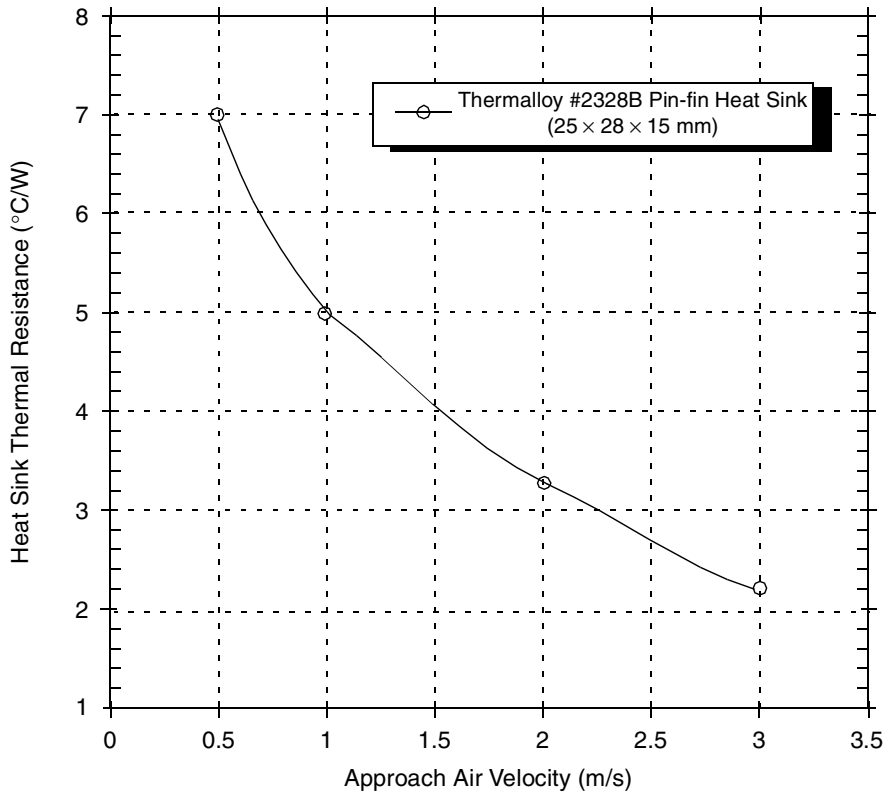


Figure 55. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

16.2.4.2 Case 2

Every system application has different conditions that the thermal management solution must solve. As an alternate example, assume that the air reaching the component is 85 °C with an approach velocity of 1 m/sec. For a maximum junction temperature of 105 °C at 7 W, the total thermal resistance of junction to case thermal resistance plus thermal interface material plus heat sink thermal resistance must be less than 2.8 °C/W. The value of the junction to case thermal resistance in Table 60 includes the thermal interface resistance of a thin layer of thermal grease as documented in footnote 4 of the table. Assuming that the heat sink is flat enough to allow a thin layer of grease or phase change material, then the heat sink must be less than 2 °C/W.

Millennium Electronics (MEI) has tooled a heat sink MTHERM-1051 for this requirement assuming a compactPCI environment at 1 m/sec and a heat sink height of 12 mm. The MEI solution is illustrated in Figure 56 and Figure 57. This design has several significant advantages:

- The heat sink is clipped to a plastic frame attached to the application board with screws or plastic inserts at the corners away from the primary signal routing areas.
- The heat sink clip is designed to apply the force holding the heat sink in place directly above the die at a maximum force of less than 10 lbs.
- For applications with significant vibration requirements, silicone damping material can be applied between the heat sink and plastic frame.

When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

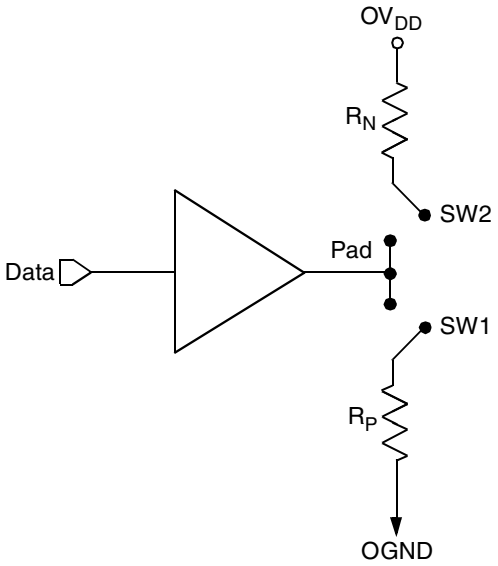


Figure 59. Driver Impedance Measurement

The output impedance of the RapidIO port drivers targets 200-Ω differential resistance. The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 61 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 61. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI/PCI-X	DDR DRAM	RapidIO	Symbol	Unit
R_N	43 Target	25 Target	20 Target	NA	Z_0	W
R_P	43 Target	25 Target	20 Target	NA	Z_0	W
Differential	NA	NA	NA	200 Target	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

Table 62. Document Revision History (continued)

Rev. No.	Substantive Change(s)
3.0	Table 1—Corrected MII management voltage reference Section 2.1.3—New Table 2—Corrected MII management voltage reference Table 5—Removed 'minimum' column Table 5—Added AV_{DD} power table Table 8—New Table 9—New Table 9—New Table 13—Added overshoot/undershoot note. Figure 4—New Table 16—Restated $t_{MCKSKEW1}$ as $t_{MCKSKEW}$, removed $t_{MCKSKEW2}$; added speed-specific minimum values for 333, 266, and 200 MHz; updated t_{DDSHME} values. Updated chapter to reflect that GMII, MII and TBI can be run with 2.5V signalling. Table 29—Added MDIO output valid timing Table 31—Updated $t_{LBIVKH1}$, $t_{LBIXKH1}$, and t_{LBOTOT}. Table 32—New Figure 20, Figure 22—Updated clock reference Table 34—Updated t_{TDIVKH} Table 35—Updated t_{TDKHOX} Added tables and figures for CPM I^2C Table 45—Updated t_{PCIVKH} Section 14.1— Changed minimum height from 2.22 to 3.07 and maximum from 2.76 to 3.75 Table 54.—Updated MII management voltage reference and added note 20. Section 16.2.4.1—Changed θ_{JC} from 0.3 to 0.8; changed die-junction temperature from 67° to 71° Section 17.7—Added paragraph that begins "TSEC1_TXD[3:0]..."
2.1	Section 2.1.3—New Table 16—Added speed-specific minimum values for 333, 266, and 200 MHz Table 31—Replaced all references to TSEC1_TXD[6:5] to TSEC2_TXD[6:5] Table 31—Added t_{LBSKEW} and note 3 Table 31—Added comment about rev. 2.x devices to note 5 Section 14.1— Changed minimum height from 2.22 to 3.07 and maximum from 2.76 to 3.75 Section 16.2.4.1—Changed θ_{JC} from 0.3 to 0.8; changed die-junction temperature from 67° to 71° Section 17.7—Added paragraph that begins "TSEC1_TXD[3:0]..."

19 Device Nomenclature

Ordering information for the parts fully covered by this specification document is provided in Section 19.1, "Part Numbers Fully Addressed by this Document."

19.1 Part Numbers Fully Addressed by this Document

Table 63 provides the Freescale part numbering nomenclature for the MPC8560. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 63. Part Numbering Nomenclature

MPC	nnnn	t	pp	ff(f)	c	r
Product Code	**Part Identifier**	**Temperature Range [1]**	**Package [2]**	**Processor Frequency [3, 4]**	**Platform Frequency**	**Revision Level**
MPC	8560	Blank = 0 to 105°C C= -40 to 105°C	PX = FC-PBGA VT = FC-PBGA (Pb-free)	833 = 833 MHz 667 = 667 MHz	L = 333 MHz J= 266 MHz	B = Rev. 2.0 (SVR = 0x80700020) C = Rev. 2.1 (SVR = 0x80700021)
MPC	8560	Blank = 0 to 105°C C = –40 to 105°C	PX = FC-PBGA VT = FC-PBGA (Pb-free)	AQ = 1.0 GHz	F = 333 MHz	B = Rev. 2.0 (SVR = 0x80700020) C = Rev. 2.1 (SVR = 0x80700021)

Notes:

1. For Temperature Range=C, Processor Frequency is limited to 667 MHz.
2. See Section 14, "Package and Pin Listings" for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. The core must be clocked at a minimum frequency of 400 MHz. A device must not be used beyond the core frequency or platform frequency indicated on the device.
4. Designers should use the maximum power value corresponding to the core and platform frequency grades indicated on the device. A lower maximum power value should not be assumed for design purposes even when running at a lower frequency.