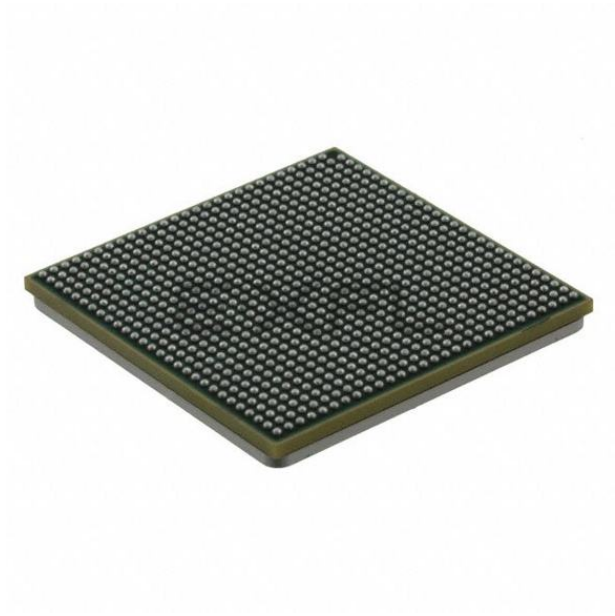

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 667MHz |
| Co-Processors/DSP | Communications; CPM |
| RAM Controllers | DDR, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | - |
| Voltage - I/O | 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8560cvt667lb |

  - Interrupts can be routed to the e500 core's standard or critical interrupt inputs
  - Interrupt summary registers allow fast identification of interrupt source
- $I^2C$ controller
  - Two-wire interface
  - Multiple master support
  - Master or slave $I^2C$ mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the $I^2C$ interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended $I^2C$ addressing mode
  - Data integrity checked with preamble signature and CRC
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 166 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
  - Three protocol engines available on a per chip select basis:
    - General purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-,16-, or 32-bit)
- Two three-speed (10/100/1Gb) Ethernet controllers (TSECs)
  - Dual IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab compliant controllers
  - Support for different Ethernet physical interfaces:
    - 10/100/1Gb Mbps IEEE 802.3 GMII
    - 10/100 Mbps IEEE 802.3 MII
    - 10 Mbps IEEE 802.3 MII
    - 1000 Mbps IEEE 802.3z TBI
    - 10/100/1Gb Mbps RGMII/RTBI
  - Full- and half-duplex support
  - Buffer descriptors are backward compatible with MPC8260 and MPC860T 10/100 programming models
  - 9.6-Kbyte jumbo frame support
  - RMON statistics support
  - 2-Kbyte internal transmit and receive FIFOs

**Table 6. Estimated Typical I/O Power Consumption (continued)**

| Interface | Parameter | $GV_{DD}$ (2.5 V) | $OV_{DD}$ (3.3 V) | $LV_{DD}$ (3.3 V) | $LV_{DD}$ (2.5 V) | Units | Notes |
|---|---|---|---|---|---|---|---|
| TDMA or TDMB | Nibble mode | — | 10 | — | — | mW | 7 |
| | Per channel | — | 5 | — | — | | |

**Notes:**

1. $GV_{DD}$=2.5, ECC enabled, 66% bus utilization, 33% write cycles, 10pF load on data, 10pF load on address/command, 10pF load on clock
2. $OV_{DD}$=3.3, 30pF load per pin, 54% bus utilization, 33% write cycles
3. $OV_{DD}$=3.3, 25pF load per pin, 5pF load on clock, 40% bus utilization, 33% write cycles
4. $V_{DD}$=1.2, $OV_{DD}$=3.3
5. LVDD=2.5/3.3, 15pF load per pin, 25% bus utilization
6. Power dissipation for one TSEC only
7. $OV_{DD}$=3.3, 10pF load per pin, 50% bus utilization

# 4 Clock Timing

## 4.1 System Clock Timing

Table 7 provides the system clock (SYSCLK) AC timing specifications for the MPC8560.

**Table 7. SYSCLK AC Timing Specifications**

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| SYSCLK frequency | $f_{SYSCLK}$ | — | — | 166 | MHz | 1 |
| SYSCLK cycle time | $t_{SYSCLK}$ | 6.0 | — | — | ns | — |
| SYSCLK rise and fall time | $t_{KH}$, $t_{KL}$ | 0.6 | 1.0 | 1.2 | ns | 2 |
| SYSCLK duty cycle | $t_{KHKL}/t_{SYSCLK}$ | 40 | — | 60 | % | 3 |
| SYSCLK jitter | — | — | — | +/- 150 | ps | 4, 5 |

**Notes:**

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, "Platform/System PLL Ratio," and Section 15.3, "e500 Core PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. For spread spectrum clocking, guidelines are +/-1% of the input frequency with a maximum of 60 kHz of modulation regardless of the input frequency.

### 7.2.3.2 TBI Receive AC Timing Specifications

Table 26 provides the TBI receive AC timing specifications.

**Table 26. TBI Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ of 3.3 V ± 5%, or $LV_{DD}$=2.5V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period | $t_{TRX}$ | | 16.0 | | ns |
| RX_CLK skew | $t_{SKTRX}$ | 7.5 | — | 8.5 | ns |
| RX_CLK duty cycle | $t_{TRXH}/t_{TRX}$ | 40 | — | 60 | % |
| RCG[9:0] setup time to rising RX_CLK | $t_{TRDVKH}$ | 2.5 | — | — | ns |
| RCG[9:0] hold time to rising RX_CLK | $t_{TRDXKH}$ | 1.5 | — | — | ns |
| RX_CLK clock rise time and fall time | $t_{TRXR}$, $t_{TRXF}$ [2,3] | 0.7 | — | 2.4 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{TRDVKH}$ symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{TRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{TRDXKH}$ symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{TRX}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{TRX}$ represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 13 shows the TBI receive AC timing diagram.

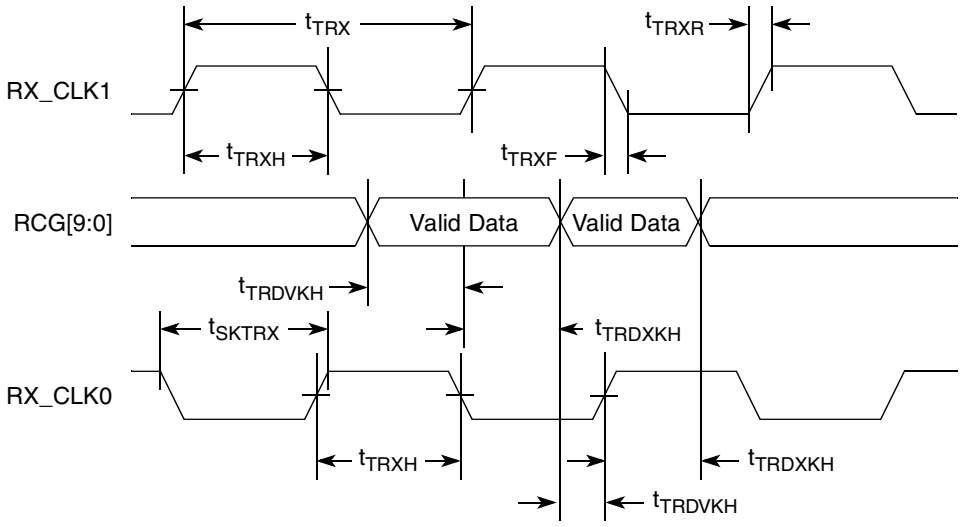


**Figure 13. TBI Receive AC Timing Diagram**

Figure 15 shows the MII management AC timing diagram.

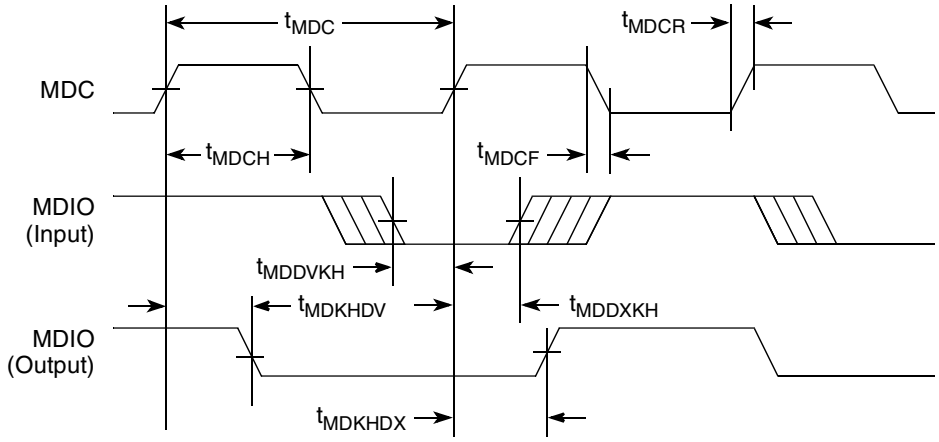


**Figure 15. MII Management Interface Timing Diagram**

# 8 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8560.

## 8.1 Local Bus DC Electrical Characteristics

Table 30 provides the DC electrical characteristics for the local bus interface.

**Table 30. Local Bus DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($V_{IN}$ [1] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | $OV_{DD}$ - 0.2 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.2 | V |

**Note:**

1.Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 8.2 Local Bus AC Electrical Specifications

Table 31 describes the general timing parameters of the local bus interface of the MPC8560 with the DLL enabled.

**Table 31. Local Bus General Timing Parameters—DLL Enabled**

| Parameter | POR Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Local bus cycle time | — | $t_{LBK}$ | 6.0 | — | ns | 2 |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | — | $t_{LBKSKEW}$ | — | 150 | ps | 3, 9 |

**Table 31. Local Bus General Timing Parameters—DLL Enabled (continued)**

| Parameter | POR Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Input setup to local bus clock (except LUPWAIT) | — | $t_{LBIVKH1}$ | 1.8 | — | ns | 4, 5, 8 |
| LUPWAIT input setup to local bus clock | — | $t_{LBIVKH2}$ | 1.7 | — | ns | 4, 5 |
| Input hold from local bus clock (except LUPWAIT) | — | $t_{LBIXKH1}$ | 0.5 | — | ns | 4, 5, 8 |
| LUPWAIT input hold from local bus clock | — | $t_{LBIXKH2}$ | 1.0 | — | ns | 4, 5 |
| LALE output transition to LAD/LDP output transition (LATCH hold time) | — | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | TSEC2_TXD[6:5] = 00 | $t_{LBKHOV1}$ | — | 2.0 | ns | 4, 8 |
| | TSEC2_TXD[6:5] = 11 (default) | | | 3.5 | | |
| Local bus clock to data valid for LAD/LDP | TSEC2_TXD[6:5] = 00 | $t_{LBKHOV2}$ | — | 2.2 | ns | 4, 8 |
| | TSEC2_TXD[6:5] = 11 (default) | | | 3.7 | | |
| Local bus clock to address valid for LAD | TSEC2_TXD[6:5] = 00 | $t_{LBKHOV3}$ | — | 2.3 | ns | 4, 8 |
| | TSEC2_TXD[6:5] = 11 (default) | | | 3.8 | | |
| Local bus clock to LALE assertion | | $t_{LBKHOV4}$ | — | 2.3 | ns | 4, 8 |
| Output hold from local bus clock (except LAD/LDP and LALE) | TSEC2_TXD[6:5] = 00 | $t_{LBKHOX1}$ | 0.7 | — | ns | 4, 8 |
| | TSEC2_TXD[6:5] = 11 (default) | | 1.6 | | | |
| Output hold from local bus clock for LAD/LDP | TSEC2_TXD[6:5] = 00 | $t_{LBKHOX2}$ | 0.7 | — | ns | 4, 8 |
| | TSEC2_TXD[6:5] = 11 (default) | | 1.6 | | | |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | TSEC2_TXD[6:5] = 00 | $t_{LBKHOZ1}$ | — | 2.5 | ns | 7, 9 |
| | TSEC2_TXD[6:5] = 11 (default) | | | 3.8 | | |

**Table 31. Local Bus General Timing Parameters—DLL Enabled (continued)**

| Parameter | POR Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Local bus clock to output high impedance for LAD/LDP | TSEC2_TXD[6:5] = 00 | $t_{LBKHOZ2}$ | — | 2.5 | ns | 7, 9 |
| | TSEC2_TXD[6:5] = 11 (default) | | | 3.8 | | |

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for DLL enabled mode.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $OV_{DD}/2$.
4. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for DLL enabled to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of $t_{LBOTOT}$ is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins TSEC2_TXD[6:5].
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.
9. Guaranteed by design.

Table 32 describes the general timing parameters of the local bus interface of the MPC8560 with the DLL bypassed.

**Table 32. Local Bus General Timing Parameters—DLL Bypassed**

| Parameter | POR Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Local bus cycle time | — | $t_{LBK}$ | 6.0 | — | ns | 2 |
| Internal launch/capture clock to LCLK delay | — | $t_{LBKHKT}$ | 2.3 | 3.9 | ns | 8 |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | — | $t_{LBKSKEW}$ | — | 150 | ps | 3, 9 |
| Input setup to local bus clock (except LUPWAIT) | — | $t_{LBIVKH1}$ | 5.7 | — | ns | 4, 5 |
| LUPWAIT input setup to local bus clock | — | $t_{LBIVKH2}$ | 5.6 | — | ns | 4, 5 |
| Input hold from local bus clock (except LUPWAIT) | — | $t_{LBIXKH1}$ | -1.8 | — | ns | 4, 5 |
| LUPWAIT input hold from local bus clock | — | $t_{LBIXKH2}$ | -1.3 | — | ns | 4, 5 |
| LALE output transition to LAD/LDP output transition (LATCH hold time) | — | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | TSEC2_TXD[6:5] = 00 | $t_{LBKLOV1}$ | — | -0.3 | ns | 4 |
| | TSEC2_TXD[6:5] = 11 (default) | | | 1.2 | | |

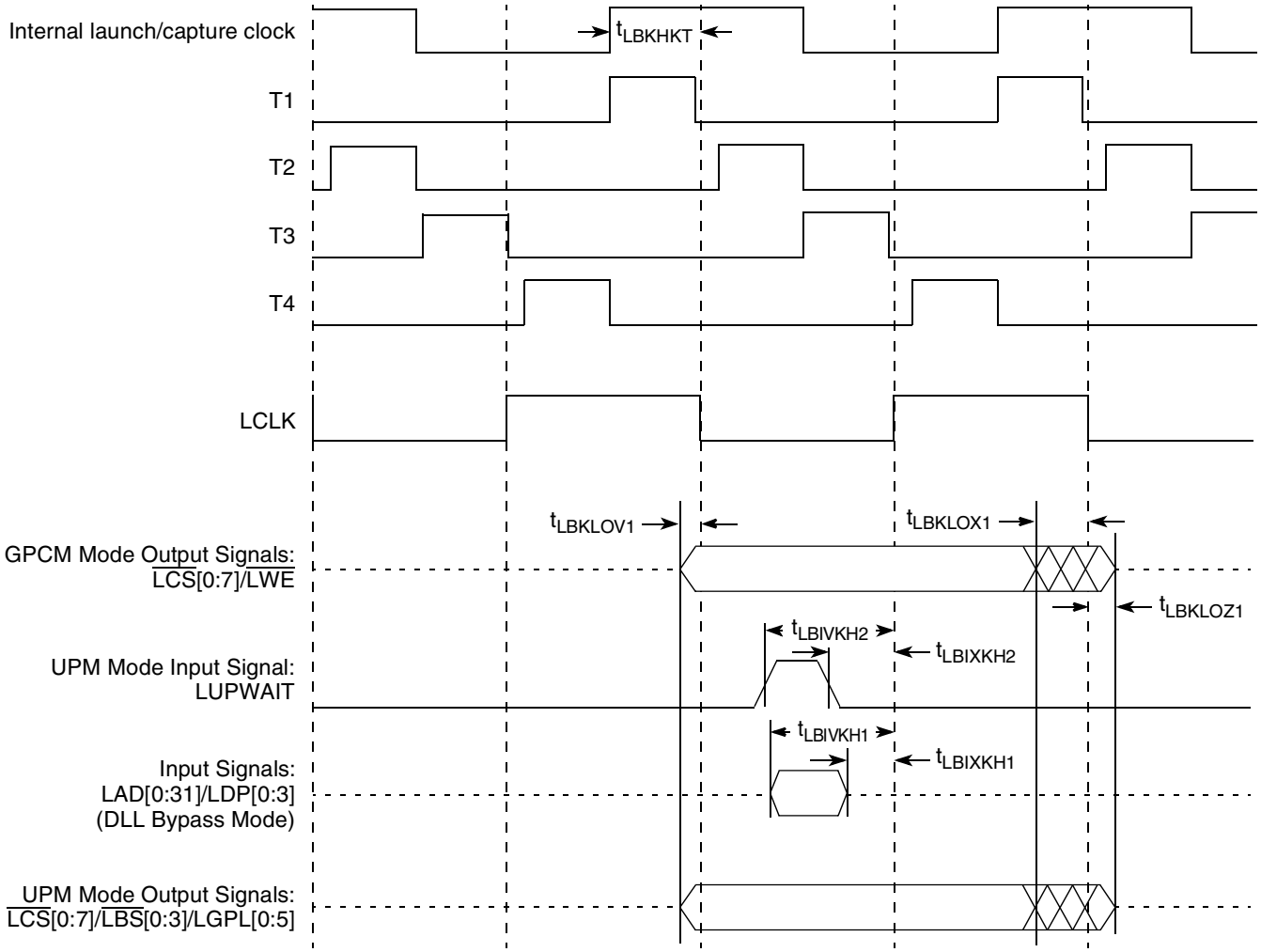


**Figure 22. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Bypass Mode)**

# 9 CPM

This section describes the DC and AC electrical specifications for the CPM of the MPC8560.

## 9.1 CPM DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the MPC8560 CPM.

**Table 33. CPM DC Electrical Characteristics**

| Characteristic | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 2.0 | 3.465 | V | 1 |
| Input low voltage | $V_{IL}$ | GND | 0.8 | V | 1, 2 |
| Output high voltage ($I_{OH}$ = –8.0 mA) | $V_{OH}$ | 2.4 | — | V | 1 |
| Output low voltage ($I_{OL}$ = 8.0 mA) | $V_{OL}$ | — | 0.5 | V | 1 |

Figure 24 shows the FCC internal clock.

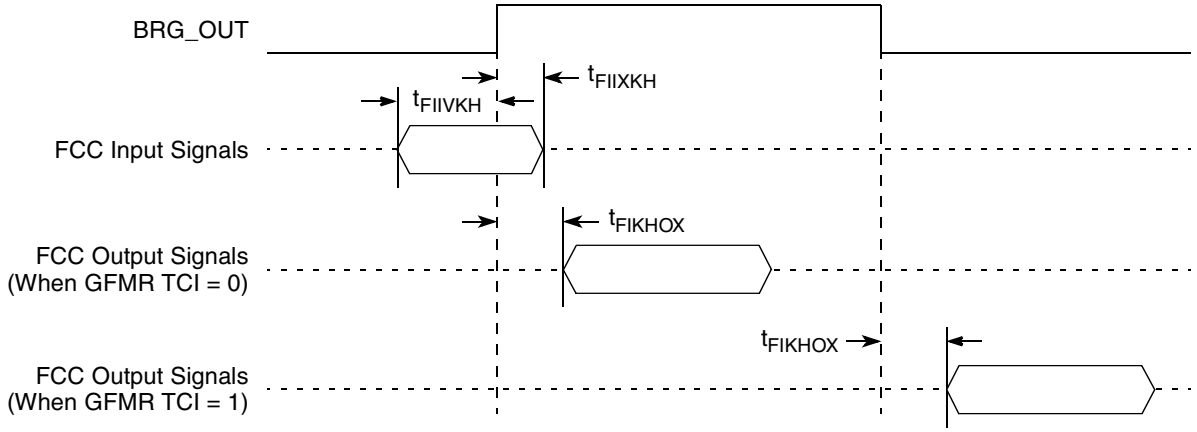


**Figure 24. FCC Internal AC Timing Clock Diagram**

Figure 25 shows the FCC external clock.

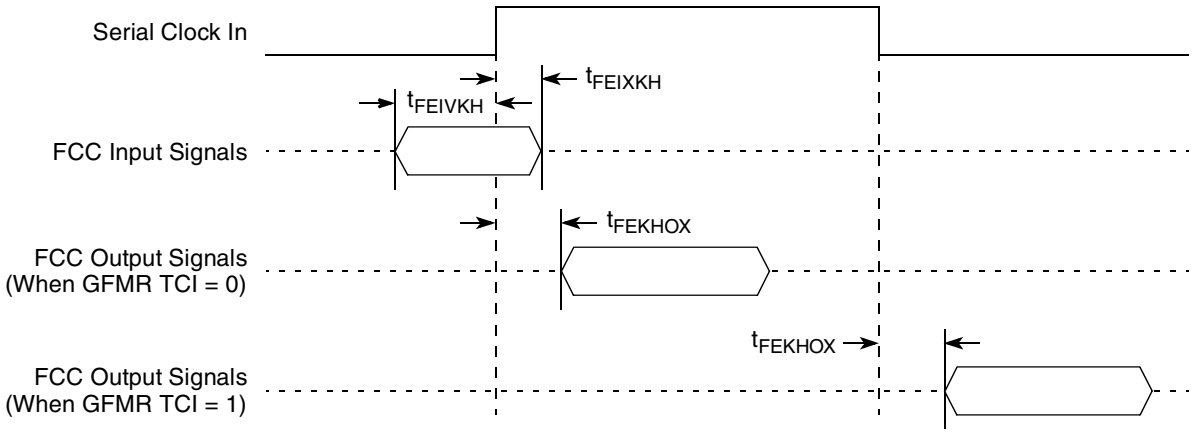


**Figure 25. FCC External AC Timing Clock Diagram**

Figure 26 shows Ethernet collision timing on FCCs.

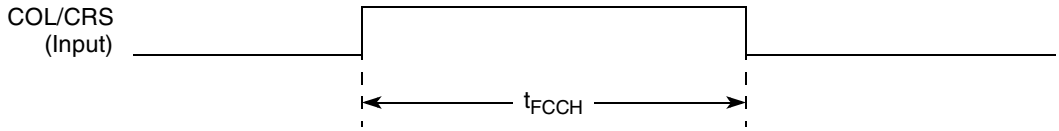


**Figure 26. Ethernet Collision AC Timing Diagram (FCC)**

Table 37 and Table 38 are examples of $I^2C$ AC parameters at $I^2C$ clock value of 100 kHz and 400 kHz respectively.

**Table 37. CPM $I^2C$ AC Timing ($f_{SCL}$ = 100 kHz)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| SCL clock frequency (slave) | $f_{SCL}$ | — | 100 | KHz |
| SCL clock frequency (master) | $f_{SCL}$ | — | 100 | KHz |
| Bus free time between transmissions | $t_{SDHDL}$ | 4.7 | — | µs |
| Low period of SCL | $t_{SCLCH}$ | 4.7 | — | µs |
| High period of SCL | $t_{SCHCL}$ | 4 | — | µs |
| Start condition setup time [2] | $t_{SCHDL}$ | 2 | — | µs |
| Start condition hold time [2] | $t_{SDLCL}$ | 3 | — | µs |
| Data hold time [2] | $t_{SCLDX}$ | 2 | — | µs |
| Data setup time [2] | $t_{SDVCH}$ | 3 | — | µs |
| SDA/SCL rise time | $t_{SRISE}$ | — | 1 | µs |
| SDA/SCL fall time | $t_{SFALL}$ | — | 303 | ns |
| Stop condition setup time | $t_{SCHDH}$ | 2 | — | µs |

**Table 38. CPM $I^2C$ AC Timing ($f_{SCL}$ = 400 kHz)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| SCL clock frequency (slave) | $f_{SCL}$ | — | 400 | KHz |
| SCL clock frequency (master) | $f_{SCL}$ | — | 400 | KHz |
| Bus free time between transmissions | $t_{SDHDL}$ | 1.2 | — | µs |
| Low period of SCL | $t_{SCLCH}$ | 1.2 | — | µs |
| High period of SCL | $t_{SCHCL}$ | 1 | — | µs |
| Start condition setup time [2] | $t_{SCHDL}$ | 420 | — | ns |
| Start condition hold time [2] | $t_{SDLCL}$ | 630 | — | ns |
| Data hold time [2] | $t_{SCLDX}$ | 420 | — | ns |
| Data setup time [2] | $t_{SDVCH}$ | 630 | — | ns |
| SDA/SCL rise time | $t_{SRISE}$ | — | 250 | ns |
| SDA/SCL fall time | $t_{SFALL}$ | — | 75 | ns |
| Stop condition setup time | $t_{SCHDH}$ | 420 | — | ns |

# 10 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8560.

Table 39 provides the JTAG AC timing specifications as defined in Figure 32 through Figure 35.

**Table 39. JTAG AC Timing Specifications (Independent of SYSCLK) [1]**

At recommended operating conditions (see Table 2).

| Parameter | Symbol [2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | — |
| JTAG external clock pulse width measured at 1.4 V | $t_{JTKHKL}$ | 15 | — | ns | — |
| JTAG external clock rise and fall times | $t_{JTGR}$ & $t_{JTGF}$ | 0 | 2 | ns | 6 |
| $\overline{\text{TRST}}$ assert time | $t_{TRST}$ | 25 | — | ns | 3 |
| Input setup times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDVKH}$<br>$t_{JTIVKH}$ | <br>4<br>0 | <br>—<br>— | ns | 4 |
| Input hold times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDXKH}$<br>$t_{JTIXKH}$ | <br>20<br>25 | <br>—<br>— | ns | 4 |
| Valid times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDV}$<br>$t_{JTKLOV}$ | <br>4<br>4 | <br>20<br>25 | ns | 5 |
| Output hold times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDX}$<br>$t_{JTKLOX}$ | | — | ns | 5 |
| JTAG external clock to output high impedance:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDZ}$<br>$t_{JTKLOZ}$ | <br>3<br>3 | <br>19<br>9 | ns | 5, 6 |

**Notes:**

1. All outputs are measured from the midpoint voltage of the falling/rising edge of $t_{TCLK}$ to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 31). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to $t_{TCLK}$.
5. Non-JTAG signal output timing with respect to $t_{TCLK}$.
6. Guaranteed by design.

Figure 37 shows the AC timing diagram for the $I^2C$ bus.

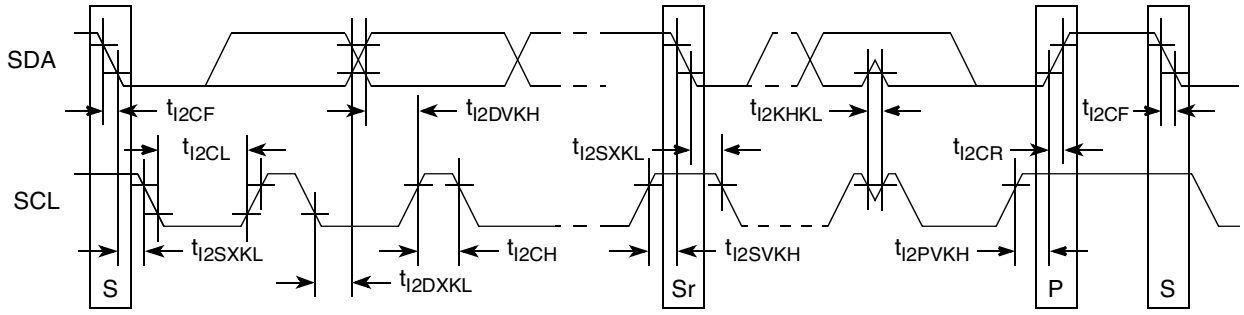


**Figure 37. $I^2C$ Bus AC Timing Diagram**

# 12 PCI/PCI-X

This section describes the DC and AC electrical specifications for the PCI/PCI-X bus of the MPC8560.

## 12.1 PCI/PCI-X DC Electrical Characteristics

Table 42 provides the DC electrical characteristics for the PCI/PCI-X interface of the MPC8560.

**Table 42. PCI/PCI-X DC Electrical Characteristics [1]**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($V_{IN}$ [2] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –100 μA) | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 100 μA) | $V_{OL}$ | — | 0.2 | V |

**Notes:**

1.Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.

2.Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

- The peak differential signal of the transmitter output or receiver input, is A – B volts.
- The peak-to-peak differential signal of the transmitter output or receiver input, is 2 × (A – B) volts.

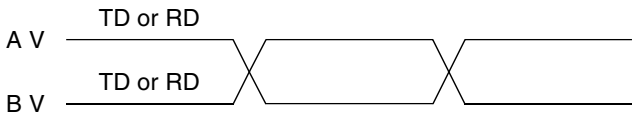


**Figure 42. Differential Peak-to-Peak Voltage of Transmitter or Receiver**

To illustrate these definitions using numerical values, consider the case where a LVDS transmitter has a common mode voltage of 1.2 V and each signal has a swing that goes between 1.4 and 1.0 V. Using these values, the peak-to-peak voltage swing of the signals TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ is 400 mV. The differential signal ranges between 400 and –400 mV. The peak differential signal is 400 mV, and the peak-to-peak differential signal is 800 mV.

A timing edge is the zero-crossing of a differential signal. Each skew timing parameter on a parallel bus is synchronously measured on two signals relative to each other in the same cycle, such as data to data, data to clock, or clock to clock. A skew timing parameter may be relative to the edge of a signal or to the middle of two sequential edges.

Static skew represents the timing difference between signals that does not vary over time regardless of system activity or data pattern. Path length differences are a primary source of static skew.

Dynamic skew represents the amount of timing difference between signals that is dependent on the activity of other signals and varies over time. Crosstalk between signals is a source of dynamic skew.

Eye diagrams and compliance masks are a useful way to visualize and specify driver and receiver performance. This technique is used in several serial bus specifications. An example compliance mask is shown in Figure 43. The key difference in the application of this technique for a parallel bus is that the data is source synchronous to its bus clock while serial data is referenced to its embedded clock. Eye diagrams reveal the quality (cleanness, openness, goodness) of a driver output or receiver input. An advantage of using an eye diagram and a compliance mask is that it allows specifying the quality of a signal without requiring separate specifications for effects such as rise time, duty cycle distortion, data dependent dynamic skew, random dynamic skew, etc. This allows the individual semiconductor manufacturer maximum flexibility to trade off various performance criteria while keeping the system performance constant.

In using the eye pattern and compliance mask approach, the quality of the signal is specified by the compliance mask. The mask specifies the maximum permissible magnitude of the signal and the minimum permissible eye opening. The eye diagram for the signal under test is generated according to the specification. Compliance is determined by whether the compliance mask can be positioned over the eye diagram such that the eye pattern falls entirely within the unshaded portion of the mask.

Serial specifications have clock encoded with the data, but the LP-LVDS physical layer defined by RapidIO is a source synchronous parallel port so additional specifications to include effects that are not found in serial links are required. Specifications for the effect of bit to bit timing differences caused by static skew have been added and the eye diagrams specified are measured relative to the associated clock in order to include clock to data effects. With the transmit output (or receiver input) eye diagram, the user can determine if the transmitter output (or receiver input) is compliant with an oscilloscope with the appropriate software.

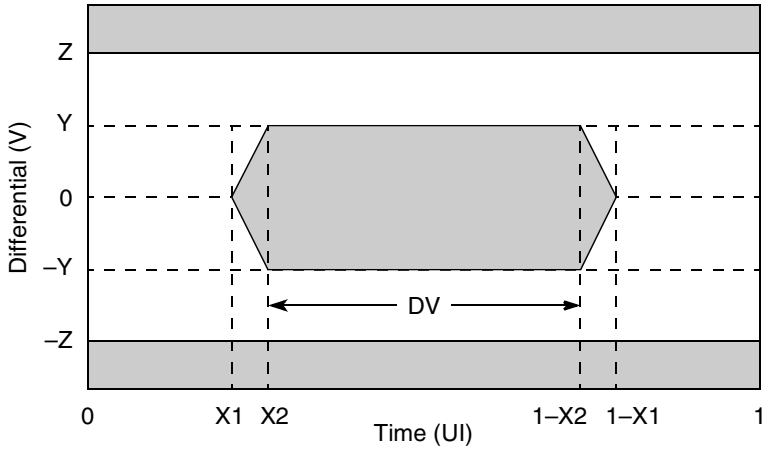


**Figure 43. Example Compliance Mask**

Y = minimum data valid amplitude

Z = maximum amplitude

1 UI = 1 unit interval = 1/baud rate

X1 = end of zero crossing region

X2 = beginning of data valid window

DV = data valid window = $1 - 2 \times X2$

The waveform of the signal under test must fall within the unshaded area of the mask to be compliant. Different masks are used for the driver output and the receiver input allowing each to be separately specified.

## 13.3.1 RapidIO Driver AC Timing Specifications

Driver AC timing specifications are provided in Table 48, Table 49, and Table 50. A driver shall comply with the specifications for each data rate/frequency for which operation of the driver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The output of a driver shall be connected to a 100 Ω, ±1%, differential (bridged) resistive load.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7]).

**Table 48. RapidIO Driver AC Timing Specifications—500 Mbps Data Rate**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Differential output high voltage | $V_{OHD}$ | 200 | 540 | mV | 1 |
| Differential output low voltage | $V_{OLD}$ | –540 | –200 | mV | 1 |

3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
7. The socket lid must always be oriented to A1.

## 14.3 Pinout Listings

Table 54 provides the pin-out listing for the MPC8560, 783 FC-PBGA package.

**Table 54. MPC8560 Pinout Listing**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **PCI/PCI-X** | | | | |
| PCI_AD[63:0] | AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14, V15, W15, Y15, AA15, AB15, AC15, AD15, AG15, AH15, V16, W16, AB16, AC16, AD16, AE16, AF16, V17, W17, Y17, AA17, AB17, AE17, AF17, AF18, AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9, AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11, AG11, AH11, V12, W12, Y12, AB12, AD12, AE12, AG12, AH12, V13, Y13, AB13, AC13 | I/O | $OV_{DD}$ | 17 |
| PCI_C_$\overline{BE}$[7:0] | AG13, AH13, V14, W14, AH8, AB10, AD11, AC12 | I/O | $OV_{DD}$ | 17 |
| PCI_PAR | AA11 | I/O | $OV_{DD}$ | — |
| PCI_PAR64 | Y14 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI\_FRAME}}$ | AC10 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI\_TRDY}}$ | AG10 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI\_IRDY}}$ | AD10 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI\_STOP}}$ | V11 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI\_DEVSEL}}$ | AH10 | I/O | $OV_{DD}$ | 2 |
| PCI_IDSEL | AA9 | I | $OV_{DD}$ | — |
| $\overline{\text{PCI\_REQ64}}$ | AE13 | I/O | $OV_{DD}$ | 5, 10 |
| $\overline{\text{PCI\_ACK64}}$ | AD13 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI\_PERR}}$ | W11 | I/O | $OV_{DD}$ | 2 |
| $\overline{\text{PCI\_SERR}}$ | Y11 | I/O | $OV_{DD}$ | 2, 4 |
| $\overline{\text{PCI\_REQ0}}$ | AF5 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI\_REQ}}$[1:4] | AF3, AE4, AG4, AE5 | I | $OV_{DD}$ | — |
| $\overline{\text{PCI\_GNT}}$[0] | AE6 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI\_GNT}}$[1:4] | AG5, AH5, AF6, AG6 | O | $OV_{DD}$ | 5, 9 |

**Table 54. MPC8560 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **JTAG** | | | | |
| TCK | AF21 | I | $OV_{DD}$ | — |
| TDI | AG21 | I | $OV_{DD}$ | 12 |
| TDO | AF19 | O | $OV_{DD}$ | 11 |
| TMS | AF23 | I | $OV_{DD}$ | 12 |
| $\overline{\text{TRST}}$ | AG23 | I | $OV_{DD}$ | 12 |
| **DFT** | | | | |
| $\overline{\text{LSSD\_MODE}}$ | AG19 | I | $OV_{DD}$ | 21 |
| L1_TSTCLK | AB22 | I | $OV_{DD}$ | 21 |
| L2_TSTCLK | AG22 | I | $OV_{DD}$ | 21 |
| $\overline{\text{TEST\_SEL}}$ | AH20 | I | $OV_{DD}$ | 3 |
| **Thermal Management** | | | | |
| THERM0 | AG2 | I | — | 14 |
| THERM1 | AH3 | I | — | 14 |
| **Power Management** | | | | |
| ASLEEP | AG18 | I/O | | 9, 19 |
| **Power and Ground Signals** | | | | |
| $AV_{DD}1$ | AH19 | Power for e500 PLL (1.2 V) | $AV_{DD}1$ | — |
| $AV_{DD}2$ | AH18 | Power for CCB PLL (1.2 V) | $AV_{DD}2$ | — |
| $AV_{DD}3$ | AH17 | Power for CPM PLL (1.2 V) | $AV_{DD}3$ | — |
| GND | A12, A17, B3, B14, B20, B26, B27, C2, C4, C11,C17, C19, C22, C27, D8, E3, E12, E24, F11, F18, F23, G9, G12, G25, H4, H12, H14, H17, H20, H22, H27, J19, J24, K5, K9, K18, K23, K28, L6, L20, L25, M4, M12, M14, M16, M22, M27, N2, N13, N15, N17, P12, P14, P16, P23, R13, R15, R17, R20, R26, T3, T8, T10, T12, T14, T16, U6, U13, U15, U16, U17, U21, V7, V10, V26, W5, W18, W23, Y8, Y16, AA6, AA13, AB4, AB11, AB19, AC6, AC9, AD3, AD8, AD17, AF2, AF4, AF10, AF13, AF15, AF27, AG3, AG7, AG26 | — | — | — |
| $GV_{DD}$ | A14, A20, A25, A26, A27, A28, B17, B22, B28, C12, C28, D16, D19, D21, D24, D28, E17, E22, F12, F15, F19, F25, G13, G18, G20, G23, G28, H19, H24, J12, J17, J22, J27, K15, K20, K25, L13, L23, L28, M25, N21 | Power for DDR DRAM I/O Voltage (2.5 V) | $GV_{DD}$ | — |

**Table 54. MPC8560 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| PD[4:31] | Y1, Y2, Y3, Y4, Y5, Y6, AA8, AA7, AA4, AA3, AA2, AA1, AB1, AB2, AB3, AB5, AB6, AC7, AC4, AC3, AC2, AC1, AD1, AD2, AD5, AD6, AE3, AE2 | I/0 | $OV_{DD}$ | — |

**Notes:**

1.All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5}}$/$\overline{\text{DMA\_REQ2}}$ is listed only once in the Local Bus Controller Interface section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA\_REQ2}}$.

2.Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to $OV_{DD}$.

3.This pin must always be pulled up to $OV_{DD}$.

4.This pin is an open drain signal.

5.This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the MPC8560 is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. If an external device connected to this pin might pull it down during reset, then a pull-up or active driver is needed if the signal is intended to be high during reset.

6.Treat these pins as no connects (NC) unless using debug address functionality.

7.The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 15.2, “Platform/System PLL Ratio.”

8.The value of LALE and LGPL2 at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 15.3, “e500 Core PLL Ratio.”

9.Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.

10.This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. Refer to the *PCI Specification*.

11.This output is actively driven during reset rather than being three-stated during reset.

12.These JTAG pins have weak internal pull-up P-FETs that are always enabled.

13.These pins are connected to the $V_{DD}$/GND planes internally and may be used by the core power supply to improve tracking and regulation.

14.Internal thermally sensitive resistor.

15.No connections should be made to these pins.

16.These pins are not connected for any functional use.

17.PCI specifications recommend that a weak pull-up resistor (2–10 kΩ) be placed on the higher order pins to $OV_{DD}$ when using 64-bit buffer mode (pins PCI_AD[63:32] and PCI_C_BE[7:4]).

18.Note that these signals are POR configurations for Rev. 1.x and notes 5 and 9 apply to these signals in Rev. 1.x but not in later revisions.

19 If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a logic –1 state during reset.

20.Recommend a pull-up resistor (~1 KΩ) b placed on this pin to $OV_{DD}$.

21.These are test signals for factory use only and must be pulled up (100 Ω - 1 kΩ) to OVDD for normal machine operation.

22.If this signal is used as both an input and an output, a weak pull-up (~10 kΩ) is required on this pin.

# 17 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8560.

## 17.1 System Clocking

The MPC8560 includes three PLLs.

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 15.2, “Platform/System PLL Ratio.”
2. The e500 Core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 15.3, “e500 Core PLL Ratio.”
3. The CPM PLL is slaved to the platform clock and is used to generate clocks used internally by the CPM block. The ratio between the CPM PLL and the platform clock is fixed and not under user control.

## 17.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$, and $AV_{DD}3$, respectively). The $AV_{DD}$ level should always be equivalent to $V_{DD}$, and preferably these voltages will be derived directly from $V_{DD}$ through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide three independent filter circuits as illustrated in Figure 58, one to each of the three $AV_{DD}$ pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific $AV_{DD}$ pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the $AV_{DD}$ pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias.

Figure 58 shows the PLL power supply filter circuit.

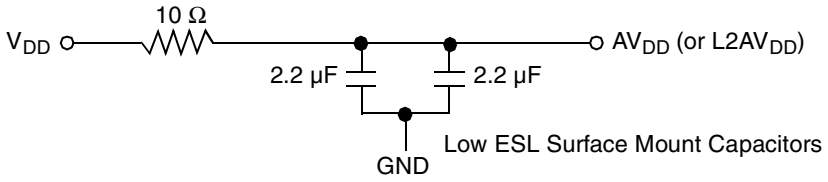


**Figure 58. PLL Power Supply Filter Circuit**

## 17.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8560 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8560 system, and the MPC8560 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each $V_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$ pins of the MPC8560. These decoupling capacitors should receive their power from separate $V_{DD}$, $OV_{DD}$, $GV_{DD}$, $LV_{DD}$, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the $V_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$ planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

## 17.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to $OV_{DD}$, $GV_{DD}$, or $LV_{DD}$ as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external $V_{DD}$, $GV_{DD}$, $LV_{DD}$, $OV_{DD}$, and GND pins of the MPC8560.

## 17.5 Output Buffer DC Impedance

The MPC8560 drivers are characterized over process, voltage, and temperature. There are two driver types: a push-pull single-ended driver (open drain for $I^2C$) for all buses except RapidIO, and a current-steering differential driver for the RapidIO port.

To measure $Z_0$ for the single-ended drivers, an external resistor is connected from the chip pad to $OV_{DD}$ or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 59). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices.

When data is held high, SW1 is closed (SW2 is open) and $R_P$ is trimmed until the voltage at the pad equals $OV_{DD}/2$. $R_P$ then becomes the resistance of the pull-up devices. $R_P$ and $R_N$ are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

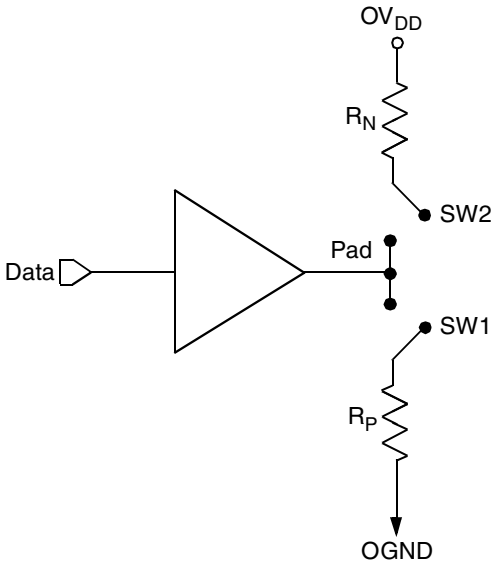


**Figure 59. Driver Impedance Measurement**

The output impedance of the RapidIO port drivers targets 200-Ω differential resistance. The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value $R_{term}$. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 61 summarizes the signal impedance targets. The driver impedance are targeted at minimum $V_{DD}$, nominal $OV_{DD}$, 105°C.

**Table 61. Impedance Characteristics**

| Impedance | Local Bus, Ethernet, DUART, Control, Configuration, Power Management | PCI/PCI-X | DDR DRAM | RapidIO | Symbol | Unit |
|---|---|---|---|---|---|---|
| $R_N$ | 43 Target | 25 Target | 20 Target | NA | $Z_0$ | W |
| $R_P$ | 43 Target | 25 Target | 20 Target | NA | $Z_0$ | W |
| Differential | NA | NA | NA | 200 Target | $Z_{DIFF}$ | W |

**Note:** Nominal supply voltages. See Table 1, $T_j$ = 105°C.

**Table 62. Document Revision History (continued)**

| Rev. No. | Substantive Change(s) |
|---|---|
| 3.2 | Updated Table 1 and Table 2 with 1.0 GHz device parameter requirements.<br>Added Section 2.1.2, “Power Sequencing”.<br>Added CPM port signal drive strength to Table 3.<br>Updated Table 4 with Maximum power data.<br>Updated Table 4 and Table 5 with 1 GHz speed grade information.<br>Updated Table 6 with corrected typical I/O power numbers.<br>Updated Table 7 Note 2 lower voltage measurement point.<br>Replaced Table 7 Note 5 with spread spectrum clocking guidelines.<br>Added to Table 8 rise and fall time information.<br>Added Section 4.4, “Real Time Clock Timing”.<br>Added precharge information to Section 6.2.2, “DDR SDRAM Output AC Timing Specifications”.<br>Removed $V_{IL}$ and $V_{IH}$ references from Table 21, Table 22, Table 23, and Table 24.<br>Added reference level note to Table 21, Table 22, Table 23, Table 24, Table 25, Table 26, and Table 27.<br>Updated TXD references to TCG in Section 7.2.3.1, “TBI Transmit AC Timing Specifications”.<br>Updated $t_{TTKHDX}$ value in Table 25.<br>Updated PMA_RX_CLK references to RX_CLK in Section 7.2.3.2, “TBI Receive AC Timing Specifications”.<br>Updated RXD references to RCG in Section 7.2.3.2, “TBI Receive AC Timing Specifications”.<br>Updated Table 27 Note 2.<br>Corrected Table 29 $f_{MDC}$ and $t_{MDC}$ to reflect the correct minimum operating frequency.<br>Updated Table 29 $t_{MDKHDV}$ and $t_{MDKHDX}$ values for clarification.<br>Added $t_{LBKHKT}$ and updated Note 2 in Table 32.<br>Corrected $\overline{\text{LGTA}}$ timing references in Figure 17.<br>Updated Figure 18, Figure 20, and Figure 22.<br>Corrected FCC output timing reference labels in Figure 24 and Figure 25.<br>Updated Figure 50.<br>Clarified Table 54 Note 5.<br>Updated Table 55 and Table 56 with 1 GHz information.<br>Added heat sink removal discussion to Section 16.2.3, “Thermal Interface Materials”.<br>Corrected and added 1 GHz part number to Table 63. |
| 3.1 | Updated Table 4 and Table 5.<br>Added Table 6.<br>Added MCK duty cycle to Table 16.<br>Updated $f_{MDC}$, $t_{MDC}$, $t_{MDKHDV}$, and $t_{MDKHDX}$ parameters in Table 29.<br>Added LALE to $t_{LBKHOV3}$ parameter in Table 31 and Table 32, and updated Figure 17.<br>Corrected active level designations of some of the pins in Table 54.<br>Updated Table 63. |