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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8560px667lb

  - Contiguous or discontiguous memory mapping
  - Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
  - Sleep mode support for self refresh SDRAM
  - Supports auto refreshing
  - On-the-fly power management using CKE signal
  - Registered DIMM support
  - Fast memory access via JTAG port
  - 2.5-V SSTL2 compatible I/O
- RapidIO interface unit
  - 8-bit RapidIO I/O and messaging protocols
  - Source-synchronous double data rate (DDR) interfaces
  - Supports small type systems (small domain, 8-bit device ID)
  - Supports four priority levels (ordering within a level)
  - Reordering across priority levels
  - Maximum data payload of 256 bytes per packet
  - Packet pacing support at the physical layer
  - CRC protection for packets
  - Supports atomic operations increment, decrement, set, and clear
  - LVDS signaling
- RapidIO–compliant message unit
  - One inbound data message structure (inbox)
  - One outbound data message structure (outbox)
  - Supports chaining and direct modes in the outbox
  - Support of up to 16 packets per message
  - Support of up to 256 bytes per packet and up to 4 Kbytes of data per message
  - Supports one inbound doorbell message structure
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts with 32-bit messages
  - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
  - Four global high resolution timers/counters that can generate interrupts
  - Supports 22 other internal interrupt sources
  - Supports fully nested interrupt delivery
  - Interrupts can be routed to external pin for external processing

Table 6 provides estimated I/O power numbers for each block: DDR, PCI, Local Bus, RapidIO, TSEC, and CPM.

Table 6. Estimated Typical I/O Power Consumption

Interface	Parameter	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Units	Notes
DDR I/O	CCB = 200 MHz	0.46	—	—	—	W	1
	CCB = 266 MHz	0.59	—	—	—		
	CCB = 300 MHz	0.66	—	—	—		
	CCB = 333 MHz	0.73	—	—	—		
PCI/PCI-X I/O	32-bit, 33 MHz	—	0.04	—	—	W	2
	32-bit 66 MHz	—	0.07	—	—		
	64-bit, 66 MHz	—	0.14	—	—		
	64-bit, 133 MHz	—	0.25	—	—		
Local Bus I/O	32-bit, 33 MHz	—	0.07	—	—	W	3
	32-bit, 66 MHz	—	0.13	—	—		
	32-bit, 133 MHz	—	0.24	—	—		
	32-bit, 167 MHz	—	0.30	—	—		
RapidIO I/O	500 MHz data rate	—	0.96	—	—	W	4
TSEC I/O	MII	—	—	10	—	mW	5, 6
	GMII, TBI (2.5 V)	—	—	—	40		
	GMII, TBI (3.3 V)	—	—	70	—		
	RGMII, RTBI	—	—	—	40		
CPM-FCC	MII	—	15	—	—	mW	7
	RMII	—	13	—	—		
	HDLC 16 Mbps	—	9	—	—		
	UTOPIA-8 SPHY	—	60	—	—		
	UTOPIA-8 MPHY	—	100	—	—		
	UTOPIA-16 SPHY	—	94	—	—		
	UTOPIA-16 MPHY	—	135	—	—		
CPM-SCC	HDLC 16 Mbps	—	4	—	—	mW	7

Table 22. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock rise and fall time	t_{GRXR}, t_{GRXF} [2,3]	—	—	1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 8 provides the AC test load for TSEC.

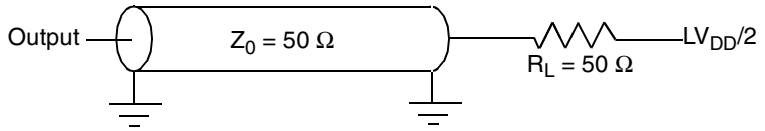

Figure 8. TSEC AC Test Load

Figure 9 shows the GMII receive AC timing diagram.

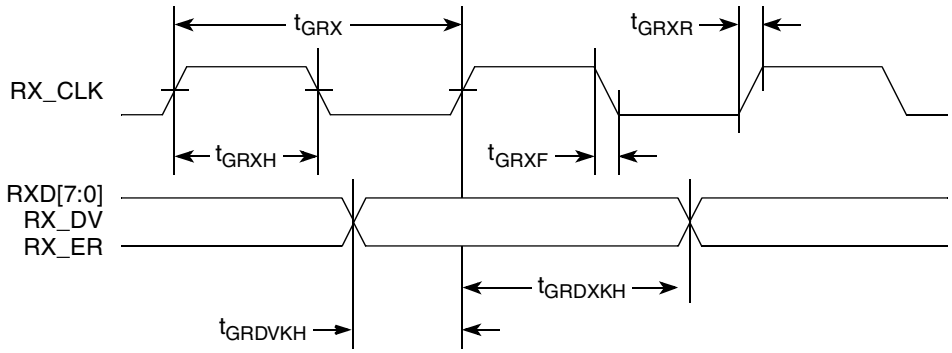

Figure 9. GMII Receive AC Timing Diagram

Figure 14 shows the RGMII and RTBI AC timing and multiplexing diagrams.

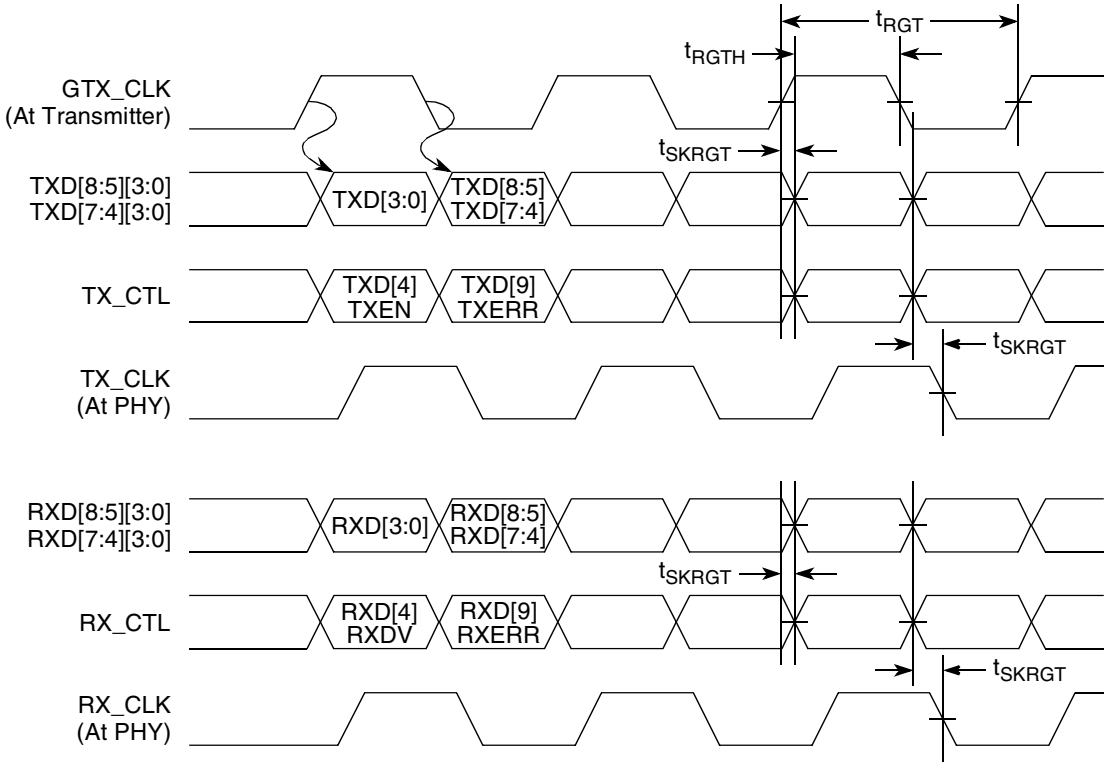

Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

7.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 7.1, "Three-Speed Ethernet Controller (TSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics."

7.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 28.

Table 28. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.13	3.47	V
Output high voltage (OV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	1.70	—	V
Input low voltage	V_{IL}	—	0.90	V

Figure 24 shows the FCC internal clock.

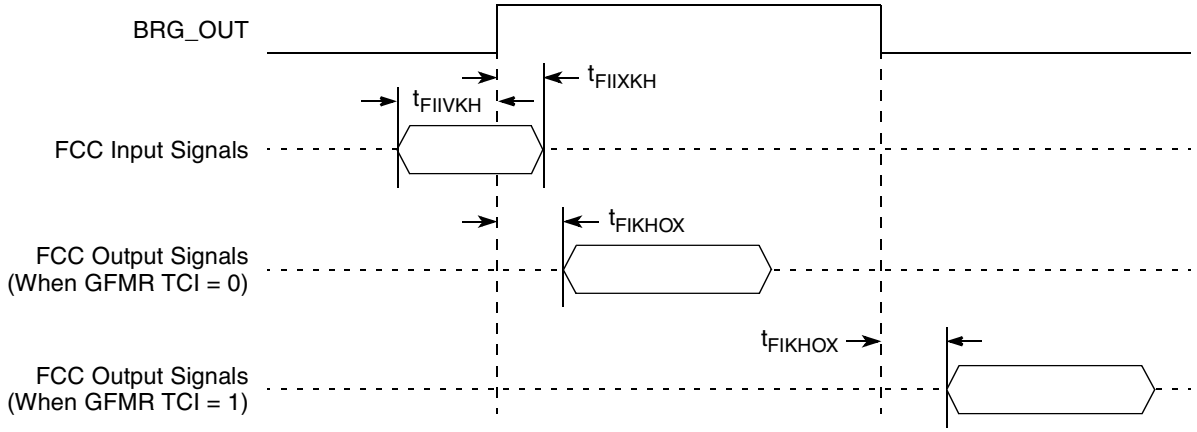

Figure 24. FCC Internal AC Timing Clock Diagram

Figure 25 shows the FCC external clock.

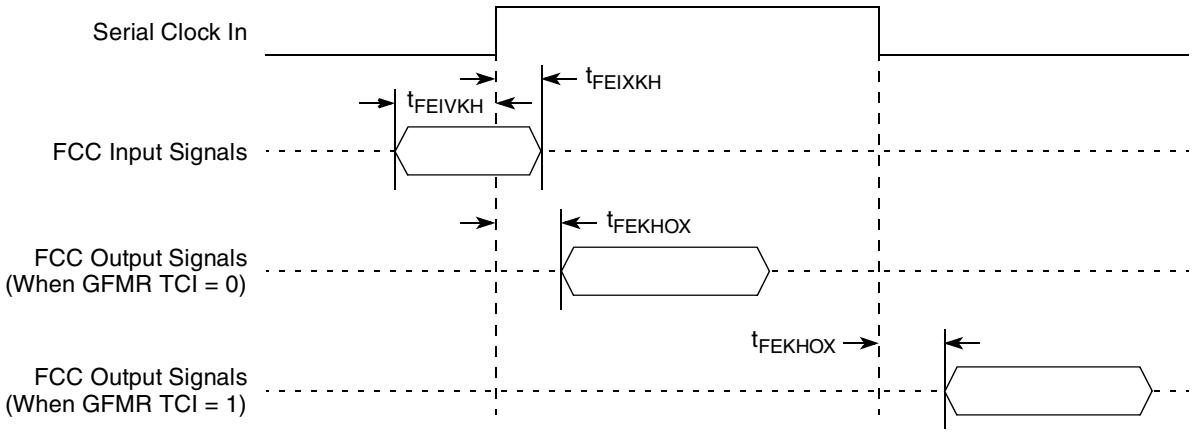

Figure 25. FCC External AC Timing Clock Diagram

Figure 26 shows Ethernet collision timing on FCCs.

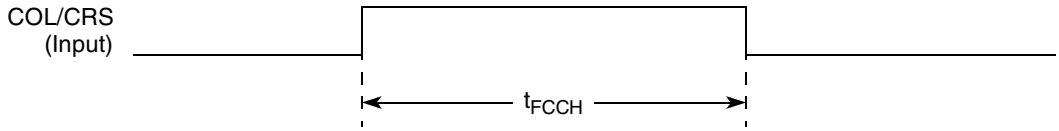

Figure 26. Ethernet Collision AC Timing Diagram (FCC)

Table 37 and Table 38 are examples of I^2C AC parameters at I^2C clock value of 100 kHz and 400 kHz respectively.

Table 37. CPM I^2C AC Timing (f_{SCL} = 100 kHz)

Characteristic	Symbol	Min	Max	Unit
SCL clock frequency (slave)	f_{SCL}	—	100	KHz
SCL clock frequency (master)	f_{SCL}	—	100	KHz
Bus free time between transmissions	t_{SDHDL}	4.7	—	µs
Low period of SCL	t_{SCLCH}	4.7	—	µs
High period of SCL	t_{SCHCL}	4	—	µs
Start condition setup time [2]	t_{SCHDL}	2	—	µs
Start condition hold time [2]	t_{SDLCL}	3	—	µs
Data hold time [2]	t_{SCLDX}	2	—	µs
Data setup time [2]	t_{SDVCH}	3	—	µs
SDA/SCL rise time	t_{SRISE}	—	1	µs
SDA/SCL fall time	t_{SFALL}	—	303	ns
Stop condition setup time	t_{SCHDH}	2	—	µs

Table 38. CPM I^2C AC Timing (f_{SCL} = 400 kHz)

Characteristic	Symbol	Min	Max	Unit
SCL clock frequency (slave)	f_{SCL}	—	400	KHz
SCL clock frequency (master)	f_{SCL}	—	400	KHz
Bus free time between transmissions	t_{SDHDL}	1.2	—	µs
Low period of SCL	t_{SCLCH}	1.2	—	µs
High period of SCL	t_{SCHCL}	1	—	µs
Start condition setup time [2]	t_{SCHDL}	420	—	ns
Start condition hold time [2]	t_{SDLCL}	630	—	ns
Data hold time [2]	t_{SCLDX}	420	—	ns
Data setup time [2]	t_{SDVCH}	630	—	ns
SDA/SCL rise time	t_{SRISE}	—	250	ns
SDA/SCL fall time	t_{SFALL}	—	75	ns
Stop condition setup time	t_{SCHDH}	420	—	ns

Figure 31 provides the AC test load for TDO and the boundary-scan outputs of the MPC8560.

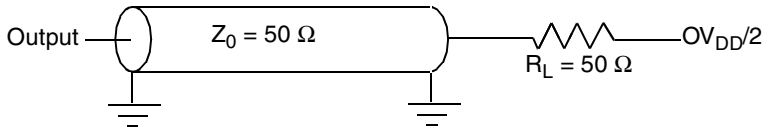

Figure 31. AC Test Load for the JTAG Interface

Figure 32 provides the JTAG clock input timing diagram.

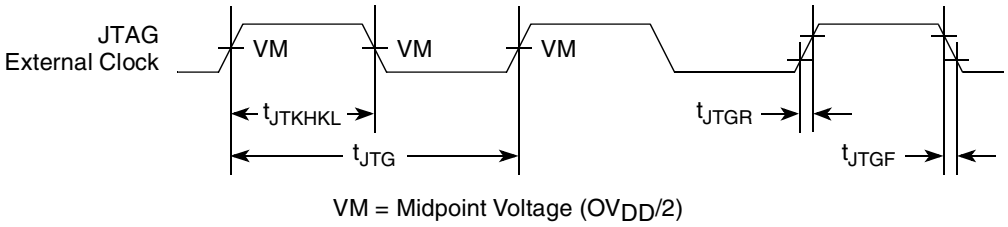

Figure 32. JTAG Clock Input Timing Diagram

Figure 33 provides the $\overline{\text{TRST}}$ timing diagram.

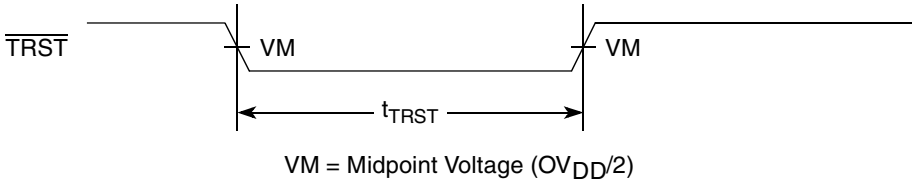

Figure 33. $\overline{\text{TRST}}$ Timing Diagram

Figure 34 provides the boundary-scan timing diagram.

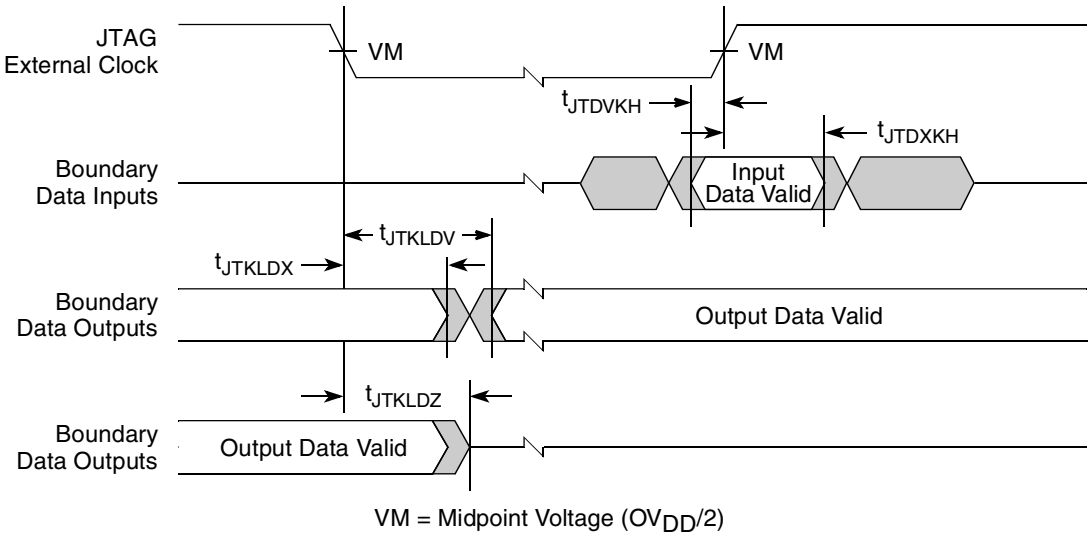

Figure 34. Boundary-Scan Timing Diagram

12.2 PCI/PCI-X AC Electrical Specifications

This section describes the general AC timing parameters of the PCI/PCI-X bus of the MPC8560. Note that the SYSCLK signal is used as the PCI input clock. Table 43 provides the PCI AC timing specifications at 66 MHz.

Table 43. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol [1]	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from SYSCLK	t_{PCKHOX}	2.0	—	ns	2, 9
SYSCLK to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3, 10
Input setup to SYSCLK	t_{PCIVKH}	3.0	—	ns	2, 4, 9
Input hold from SYSCLK	t_{PCIXKH}	0	—	ns	2, 4, 9
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ [9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	5, 6, 10
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	6, 10
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	7, 10

Notes:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI/PCI-X timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI/PCI-X timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 15, "Clocking."
6. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
7. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
8. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 µs.
9. Guaranteed by characterization.
10. Guaranteed by design.

- The peak differential signal of the transmitter output or receiver input, is A – B volts.
- The peak-to-peak differential signal of the transmitter output or receiver input, is 2 × (A – B) volts.

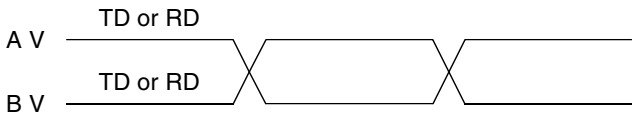

Figure 42. Differential Peak-to-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using numerical values, consider the case where a LVDS transmitter has a common mode voltage of 1.2 V and each signal has a swing that goes between 1.4 and 1.0 V. Using these values, the peak-to-peak voltage swing of the signals TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ is 400 mV. The differential signal ranges between 400 and –400 mV. The peak differential signal is 400 mV, and the peak-to-peak differential signal is 800 mV.

A timing edge is the zero-crossing of a differential signal. Each skew timing parameter on a parallel bus is synchronously measured on two signals relative to each other in the same cycle, such as data to data, data to clock, or clock to clock. A skew timing parameter may be relative to the edge of a signal or to the middle of two sequential edges.

Static skew represents the timing difference between signals that does not vary over time regardless of system activity or data pattern. Path length differences are a primary source of static skew.

Dynamic skew represents the amount of timing difference between signals that is dependent on the activity of other signals and varies over time. Crosstalk between signals is a source of dynamic skew.

Eye diagrams and compliance masks are a useful way to visualize and specify driver and receiver performance. This technique is used in several serial bus specifications. An example compliance mask is shown in Figure 43. The key difference in the application of this technique for a parallel bus is that the data is source synchronous to its bus clock while serial data is referenced to its embedded clock. Eye diagrams reveal the quality (cleanness, openness, goodness) of a driver output or receiver input. An advantage of using an eye diagram and a compliance mask is that it allows specifying the quality of a signal without requiring separate specifications for effects such as rise time, duty cycle distortion, data dependent dynamic skew, random dynamic skew, etc. This allows the individual semiconductor manufacturer maximum flexibility to trade off various performance criteria while keeping the system performance constant.

In using the eye pattern and compliance mask approach, the quality of the signal is specified by the compliance mask. The mask specifies the maximum permissible magnitude of the signal and the minimum permissible eye opening. The eye diagram for the signal under test is generated according to the specification. Compliance is determined by whether the compliance mask can be positioned over the eye diagram such that the eye pattern falls entirely within the unshaded portion of the mask.

Serial specifications have clock encoded with the data, but the LP-LVDS physical layer defined by RapidIO is a source synchronous parallel port so additional specifications to include effects that are not found in serial links are required. Specifications for the effect of bit to bit timing differences caused by static skew have been added and the eye diagrams specified are measured relative to the associated clock in order to include clock to data effects. With the transmit output (or receiver input) eye diagram, the user can determine if the transmitter output (or receiver input) is compliant with an oscilloscope with the appropriate software.

Table 48. RapidIO Driver AC Timing Specifications—500 Mbps Data Rate (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle	DC	48	52	%	2, 6
V_{OD} rise time, 20%–80% of peak-to-peak differential signal swing	t_{FALL}	200	—	ps	3, 6
V_{OD} fall time, 20%–80% of peak-to-peak differential signal swing	t_{RISE}	200	—	ps	6
Data valid	DV	1260	—	ps	
Skew of any two data outputs	t_{DPAIR}	—	180	ps	4, 6
Skew of single data outputs to associated clock	$t_{SKEW,PAIR}$	–180	180	ps	5, 6

Notes:

1.See Figure 44.

2.Requires ±100 ppm long term frequency stability.

3.Measured at V_{OD} = 0 V.

4.Measured using the RapidIO transmit mask shown in Figure 44.

5.See Figure 49.

6.Guaranteed by design.

Table 49. RapidIO Driver AC Timing Specifications—750 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential output high voltage	V_{OHD}	200	540	mV	1
Differential output low voltage	V_{OLD}	–540	–200	mV	1
Duty cycle	DC	48	52	%	2, 6
V_{OD} rise time, 20%–80% of peak-to-peak differential signal swing	t_{FALL}	133	—	ps	3, 6
V_{OD} fall time, 20%–80% of peak-to-peak differential signal swing	t_{RISE}	133	—	ps	6
Data valid	DV	800	—	ps	6
Skew of any two data outputs	t_{DPAIR}	—	133	ps	4, 6
Skew of single data outputs to associated clock	$t_{SKEW,PAIR}$	–133	133	ps	5, 6

Notes:

1.See Figure 44.

2.Requires ±100 ppm long term frequency stability.

3.Measured at V_{OD} = 0 V.

4.Measured using the RapidIO transmit mask shown in Figure 44.

5.See Figure 49.

6.Guaranteed by design.

13.3.2 RapidIO Receiver AC Timing Specifications

The RapidIO receiver AC timing specifications are provided in Table 51. A receiver shall comply with the specifications for each data rate/frequency for which operation of the receiver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The specifications apply over the receiver common mode and differential input voltage ranges.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7])

Table 51. RapidIO Receiver AC Timing Specifications—500 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1, 5
Data valid	DV	1080		ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}	—	380	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–300	300	ps	4

Notes:
1.Measured at V_{ID} = 0 V.
2.Measured using the RapidIO receive mask shown in Figure 46.
3.See Figure 49.
4.See Figure 48 and Figure 49.
5.Guaranteed by design.

Table 52. RapidIO Receiver AC Timing Specifications—750 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1, 5
Data valid	DV	600	—	ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}	—	400	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–267	267	ps	4

Notes:
1.Measured at V_{ID} = 0 V.
2.Measured using the RapidIO receive mask shown in Figure 46.
3.See Figure 49.
4.See Figure 48 and Figure 49.
5.Guaranteed by design.

Figure 48 shows the definitions of the data to clock static skew parameter $t_{SKEW,PAIR}$ and the data valid window parameter DV. The data and frame bits are those that are associated with the clock. The figure applies for all zero-crossings of the clock. All of the signals are differential signals. V_D represents V_{OD} for the transmitter and V_{ID} for the receiver. The center of the eye is defined as the midpoint of the region in which the magnitude of the signal voltage is greater than or equal to the minimum DV voltage.

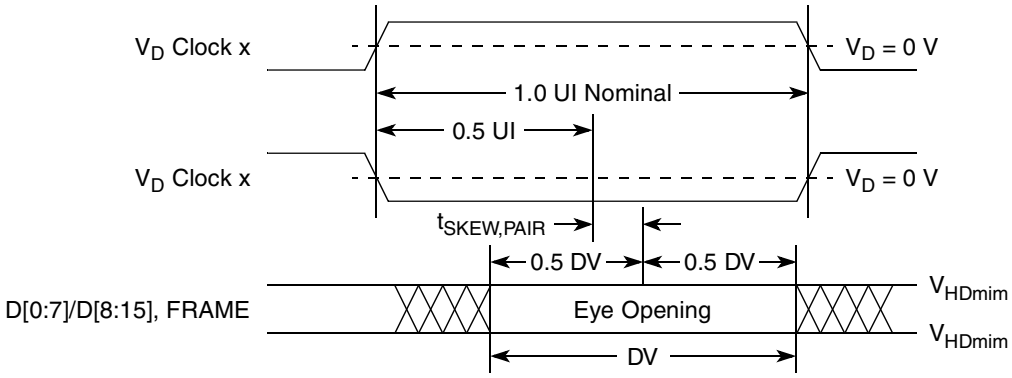

Figure 48. Data to Clock Skew

Figure 49 shows the definition of the data to data static skew parameter t_{DPAIR} and how the skew parameters are applied.

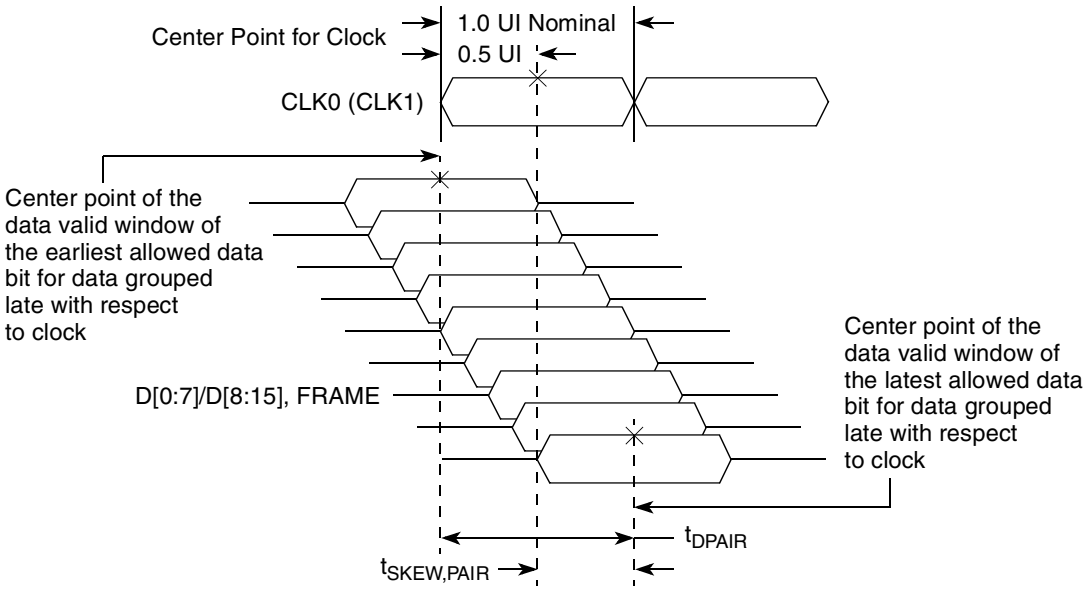

Figure 49. Static Skew Diagram

14.2 Mechanical Dimensions of the MPC8560 FC-PBGA

Figure 50 the mechanical dimensions and bottom surface nomenclature of the MPC8560, 783 FC-PBGA package.

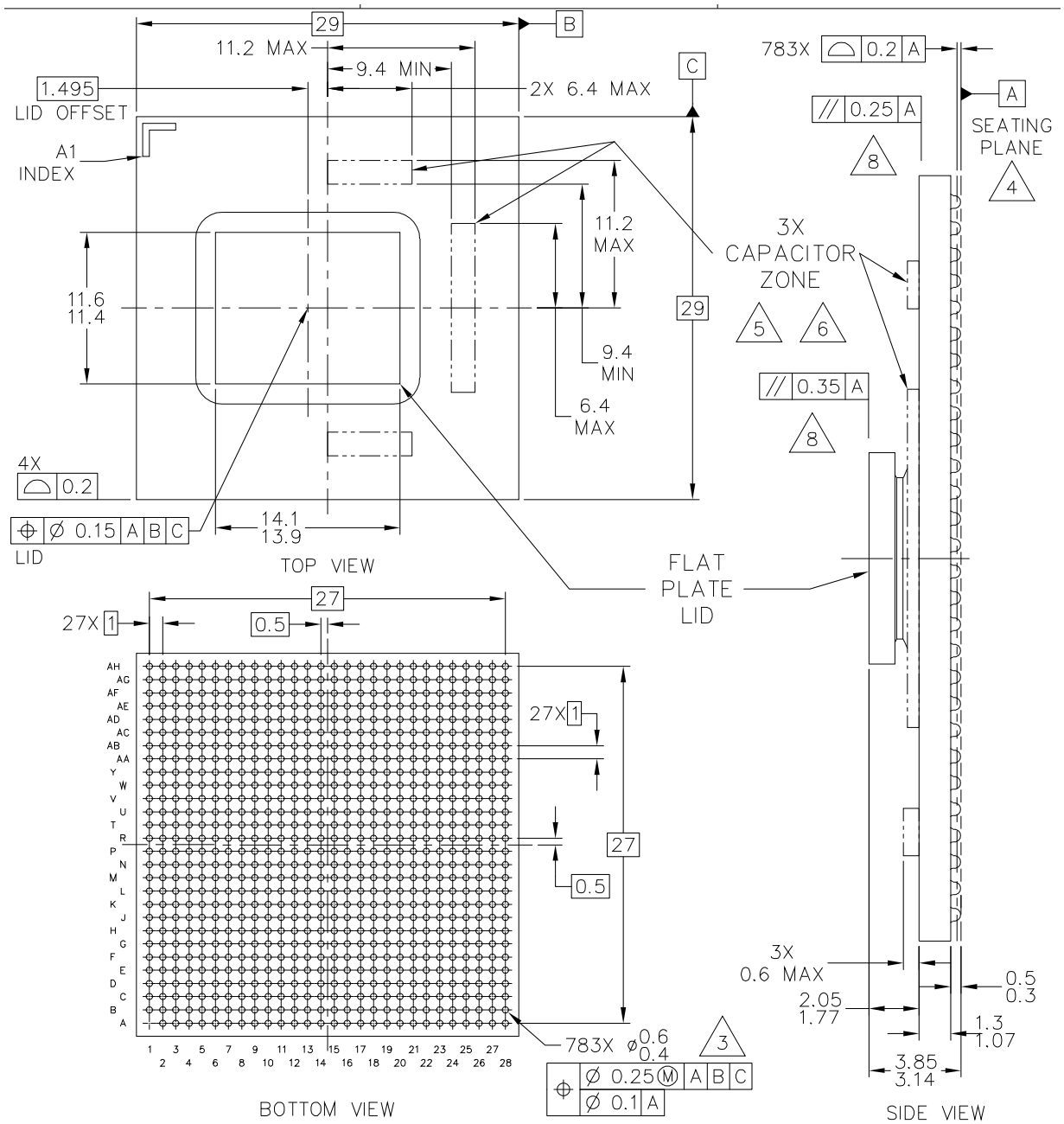

Figure 50. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8560 FC-PBGA

NOTES

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.

Table 54. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface				
MDQ[0:63]	M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12	I/O	GV_{DD}	—
MECC[0:7]	N20, M20, L19, E19, C21, A21, G19, A19	I/O	GV_{DD}	—
MDM[0:8]	L24, H28, F24, L21, E18, E16, G14, B13, M19	O	GV_{DD}	—
MDQS[0:8]	L26, J25, D25, A22, H18, F16, F14, C13, C20	I/O	GV_{DD}	—
MBA[0:1]	B18, B19	O	GV_{DD}	—
MA[0:14]	N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13	O	GV_{DD}	—
$\overline{\text{MWE}}$	D17	O	GV_{DD}	—
$\overline{\text{MRAS}}$	F17	O	GV_{DD}	—
$\overline{\text{MCAS}}$	J16	O	GV_{DD}	—
$\overline{\text{MCS}}$[0:3]	H16, G16, J15, H15	O	GV_{DD}	—
MCKE[0:1]	E26, E28	O	GV_{DD}	11
MCK[0:5]	J20, H25, A15, D20, F28, K14	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	F20, G27, B15, E20, F27, L14	O	GV_{DD}	—
MSYNC_IN	M28	I	GV_{DD}	—
MSYNC_OUT	N28	O	GV_{DD}	—
Local Bus Controller Interface				
LA[27]	U18	O	OV_{DD}	5, 9
LA[28:31]	T18, T19, T20, T21	O	OV_{DD}	7, 9
LAD[0:31]	AD26, AD27, AD28, AC26, AC27, AC28, AA22, AA23, AA26, Y21, Y22, Y26, W20, W22, W26, V19, T22, R24, R23, R22, R21, R18, P26, P25, P20, P19, P18, N22, N23, N24, N25, N26	I/O	OV_{DD}	—
LALE	V21	O	OV_{DD}	8, 9
LBCTL	V20	O	OV_{DD}	9
LCKE	U23	O	OV_{DD}	—
LCLK[0:2]	U27, U28, V18	O	OV_{DD}	—
$\overline{\text{LCS}}$[0:4]	Y27, Y28, W27, W28, R27	O	OV_{DD}	18
$\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$	R28	I/O	OV_{DD}	1

Table 54. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LCS6/DMA_DACK2	P27	O	OV_{DD}	1
LCS7/DMA_DDONE2	P28	O	OV_{DD}	1
LDP[0:3]	AA27, AA28, T26, P21	I/O	OV_{DD}	
LGPL0/LSDA10	U19	O	OV_{DD}	5, 9
LGPL1/LSDWE	U22	O	OV_{DD}	5, 9
LGPL2/LOE/LSDRAS	V28	O	OV_{DD}	8, 9
LGPL3/LSDCAS	V27	O	OV_{DD}	5, 9
LGPL4/LGTA/LUPWAIT/ LPBSE	V23	I/O	OV_{DD}	22
LGPL5	V22	O	OV_{DD}	5, 9
LSYNC_IN	T27	I	OV_{DD}	—
LSYNC_OUT	T28	O	OV_{DD}	—
LWE[0:1]/LSDDQM[0:1]/LBS[0:1]	AB28, AB27	O	OV_{DD}	1, 5, 9
LWE[2:3]/LSDDQM[2:3]/LBS[2:3]	T23, P24	O	OV_{DD}	1, 5, 9
DMA				
DMA_DREQ[0:1]	H5, G4	I	OV_{DD}	—
DMA_DACK[0:1]	H6, G5	O	OV_{DD}	—
DMA_DDONE[0:1]	H7, G6	O	OV_{DD}	—
Programmable Interrupt Controller				
MCP	AG17	I	OV_{DD}	—
UDE	AG16	I	OV_{DD}	—
IRQ[0:7]	AA18, Y18, AB18, AG24, AA21, Y19, AA19, AG25	I	OV_{DD}	—
IRQ8	AB20	I	OV_{DD}	9
IRQ9/DMA_DREQ3	Y20	I	OV_{DD}	1
IRQ10/DMA_DACK3	AF26	I/O	OV_{DD}	1
IRQ11/DMA_DDONE3	AH24	I/O	OV_{DD}	1
IRQ_OUT	AB21	O	OV_{DD}	2, 4
Ethernet Management Interface				
EC_MDC	F1	O	OV_{DD}	5, 9
EC_MDIO	E1	I/O	OV_{DD}	—

15 Clocking

This section describes the PLL configuration of the MPC8560. Note that the platform clock is identical to the CCB clock.

15.1 Clock Ranges

Table 55 provides the clocking specifications for the processor core and Table 56 provides the clocking specifications for the memory bus.

Table 55. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	667 MHz		833 MHz		1 GHz			
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	400	667	400	833	400	1000	MHz	1, 2, 3

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, "Platform/System PLL Ratio," and Section 15.3, "e500 Core PLL Ratio," for ratio settings.
2.)The minimum e500 core frequency is based on the minimum platform frequency of 200 MHz.
3.)The 1.0 GHz core frequency is based on a 1.3 V VDD supply voltage.

Table 56. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	667 MHz		833 MHz		1 GHz			
	Min	Max	Min	Max	Min	Max		
Memory bus frequency	100	166	100	166	100	166	MHz	1, 2, 3

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, "Platform/System PLL Ratio," and Section 15.3, "e500 Core PLL Ratio," for ratio settings.
2. The memory bus speed is half of the DDR data rate, hence, half of the platform clock frequency.
3.)The 1.0 GHz core frequency is based on a 1.3 V VDD supply voltage.

15.4 Frequency Options

Table 59 shows the expected frequency values for the platform frequency when using a CCB to SYSCLK ratio in comparison to the memory bus speed.

Table 59. Frequency Options with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)								
	16.67	25	33.33	41.63	66.67	83	100	111	133.33
	Platform/CCB Frequency (MHz)								
2							200	222	267
3					200	250	300	333	
4					267	333			
5				208	333				
6			200	250					
8		200	267	333					
9		225	300						
10		250	333						
12	200	300							
16	267								

16 Thermal

This section describes the thermal specifications of the MPC8560.

16.1 Thermal Characteristics

Table 60 provides the package thermal characteristics for the MPC8560.

Table 60. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection on four layer board (2s2p)	$R_{\theta JMA}$	16	°C/W	1, 2
Junction-to-ambient (@100 ft/min or 0.5 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	14	°C/W	1, 2
Junction-to-ambient (@200 ft/min or 1 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	12	°C/W	1, 2
Junction-to-board thermal	$R_{\theta JB}$	7.5	°C/W	3

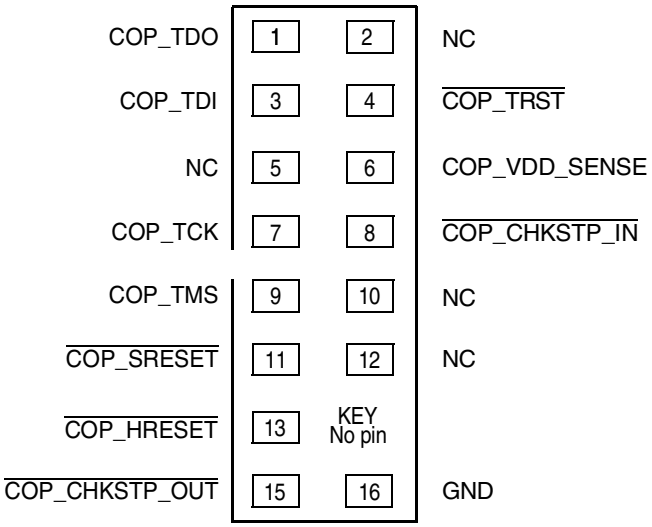

Figure 60. COP Connector Physical Pinout

17.8.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 61. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 kΩ resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

Table 62. Document Revision History (continued)

Rev. No.	Substantive Change(s)
1.2	Section 1.1.1—Updated feature list. Section 1.2.1.1—Updated notes for Table 1. Section 1.2.1.2—Removed 5-V PCI interface overshoot and undershoot figure. Section 1.2.1.3—Added this section to summarize impedance driver settings for various interfaces. Section 1.4—Updated rows in Reset Initialization timing specifications table. Added a table with DLL and PLL timing specifications. Section 1.5.2.2—Updated note 6 of DDR SDRAM Output AC Timing Specifications table. Section 1.7—Changed the minimum input low current from -600 to -15 μA for the RGMII DC electrical characteristics. Section 1.7.2—Changed LCS[3:4] to TSEC1_TXD[6:5]. Updated notes regarding LCS[3:4]. Section 1.13.2—Updated the mechanical dimensions diagram for the package. Section 1.13.3—Updated the notes for LBCTL, TRIG_OUT, and ASLEEP. Corrected pin assignments for IIC_SDA and IIC_SCL. Corrected reserved pin assignment of V11 to U11. V11 is actually $\overline{\text{PCI\_STOP}}$. Section 1.14.1—Updated the table for frequency options with respect to platform/CCB frequencies. Section 1.14.4—Edited Frequency options with respect to memory bus speeds.
1.1	Made updates throughout document. Section 1.6.1—Added symbols and note for the GTX_CLK125 timing parameters. Section 1.11.3—Updated pin list table: LGPL5/LSDAMUX to LGPL5, LA[27:29] and LA[30:31] to LA[27:31], TRST to $\overline{\text{TRST}}$, added GBE Clocking section and EC_GTX_CLK125 signal. Figure 50—Updated pin 2 connection information.
1	Original Customer Version.

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