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NXP USA Inc. - MPC8560PX833LC Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	833MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8560px833lc

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- Contiguous or discontiguous memory mapping
- Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
- Sleep mode support for self refresh SDRAM
- Supports auto refreshing
- On-the-fly power management using CKE signal
- Registered DIMM support
- Fast memory access via JTAG port
- 2.5-V SSTL2 compatible I/O
- RapidIO interface unit
 - 8-bit RapidIO I/O and messaging protocols
 - Source-synchronous double data rate (DDR) interfaces
 - Supports small type systems (small domain, 8-bit device ID)
 - Supports four priority levels (ordering within a level)
 - Reordering across priority levels
 - Maximum data payload of 256 bytes per packet
 - Packet pacing support at the physical layer
 - CRC protection for packets
 - Supports atomic operations increment, decrement, set, and clear
 - LVDS signaling
- RapidIO-compliant message unit
 - One inbound data message structure (inbox)
 - One outbound data message structure (outbox)
 - Supports chaining and direct modes in the outbox
 - Support of up to 16 packets per message
 - Support of up to 256 bytes per packet and up to 4 Kbytes of data per message
 - Supports one inbound doorbell message structure
- Programmable interrupt controller (PIC)
 - Programming model is compliant with the OpenPIC architecture
 - Supports 16 programmable interrupt and processor task priority levels
 - Supports 12 discrete external interrupts
 - Supports 4 message interrupts with 32-bit messages
 - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
 - Four global high resolution timers/counters that can generate interrupts
 - Supports 22 other internal interrupt sources
 - Supports fully nested interrupt delivery
 - Interrupts can be routed to external pin for external processing

Overview

- Interrupts can be routed to the e500 core's standard or critical interrupt inputs
- Interrupt summary registers allow fast identification of interrupt source
- I²C controller
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I²C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I²C addressing mode
 - Data integrity checked with preamble signature and CRC
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data operating at up to 166 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
 - Three protocol engines available on a per chip select basis:
 - General purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)
 - Dedicated single data rate SDRAM controller
 - Parity support
 - Default boot ROM chip select with configurable bus width (8-,16-, or 32-bit)
- Two three-speed (10/100/1Gb) Ethernet controllers (TSECs)
 - Dual IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab compliant controllers
 - Support for different Ethernet physical interfaces:
 - 10/100/1Gb Mbps IEEE 802.3 GMII
 - 10/100 Mbps IEEE 802.3 MII
 - 10 Mbps IEEE 802.3 MII
 - 1000 Mbps IEEE 802.3z TBI
 - 10/100/1Gb Mbps RGMII/RTBI
 - Full- and half-duplex support
 - Buffer descriptors are backward compatible with MPC8260 and MPC860T 10/100 programming models
 - 9.6-Kbyte jumbo frame support
 - RMON statistics support
 - 2-Kbyte internal transmit and receive FIFOs

Electrical Characteristics

- System performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter-specific events
 - Supports 64 reference events that can be counted on any of the 8 counters
 - Supports duration and quantity threshold counting
 - Burstiness feature that permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- System access port
 - Uses JTAG interface and a TAP controller to access entire system memory map
 - Supports 32-bit accesses to configuration registers
 - Supports cache-line burst accesses to main memory
 - Supports large block (4-Kbyte) uploads and downloads
 - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1TM-compliant, JTAG boundary scan
- 783 FC-PBGA package

2 Electrical Characteristics

This section provides the electrical specifications and thermal characteristics for the MPC8560. The MPC8560 is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

	Characteristic	Symbol	Max Value	Unit	Notes
Core supply voltage	For devices rated at 667 and 833 MHz For devices rated at 1 GHz	V _{DD}	–0.3 to 1.32 –0.3 to 1.43	V	_
PLL supply voltage	For devices rated at 667 and 833 MHz For devices rated at 1 GHz	AV _{DD}	-0.3 to 1.32 -0.3 to 1.43	V	_

Table 1. Absolute Maximum Ratings ¹

Chara	cteristic	Symbol Max Value		Unit	Notes
DDR DRAM I/O voltage		GV _{DD}	-0.3 to 3.63	V	—
Three-speed Ethernet I/O voltage		LV _{DD}	-0.3 to 3.63 -0.3 to 2.75	V	—
CPM, PCI/PCI-X, local bus, Rap management, DUART, system of I ² C, and JTAG I/O voltage	bidIO, 10/100 Ethernet,MII control and power management,	OV _{DD}	-0.3 to 3.63	V	3
Input voltage	DDR DRAM signals	MV _{IN}	–0.3 to (GV _{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV _{REF}	–0.3 to (GV _{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV _{IN}	–0.3 to (LV _{DD} + 0.3)	V	4, 5
	CPM, Local bus, RapidIO, 10/100 Ethernet, SYSCLK, system control and power management, I ² C, and JTAG signals	OV _{IN}	-0.3 to (OV _{DD} + 0.3)	V	5
	PCI/PCI-X	OV _{IN}	-0.3 to (OV _{DD} + 0.3)	V	6
Storage temperature range		T _{STG}	–55 to 150	°C	_

Table 1. Absolute Maximum Ratings ¹ (continued)

Notes:

- 1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 5. (M,L,O)VIN and MVREF may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
- 6. OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

2.1.2 Power Sequencing

The MPC8560 requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

- 1. V_{DD} , AV_{DD}
- 2. GV_{DD}, LV_{DD}, OV_{DD} (I/O supplies)

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90 percent of their value before the voltage rails on the current step reach 10 percent of theirs.

Power Characteristics

Table 6 provides estimated I/O power numbers for each block: DDR, PCI, Local Bus, RapidIO, TSEC, and CPM.

Interface	Parameter	GV _{DD} (2.5 V)	OV _{DD} (3.3 V)	LV _{DD} (3.3 V)	LV _{DD} (2.5 V)	Units	Notes
DDR I/O	CCB = 200 MHz	0.46	—	—	—	W	1
	CCB = 266 MHz	0.59	_	_	_		
	CCB = 300 MHz	0.66	_	_	_		
	CCB = 333 MHz	0.73	—	—	_		
PCI/PCI-X I/O	32-bit, 33 MHz	—	0.04	—	_	W	2
	32-bit 66 MHz	—	0.07	—	—		
	64-bit, 66 MHz	—	0.14	—	—		
	64-bit, 133 MHz	—	0.25	—	—		
Local Bus I/O	32-bit, 33 MHz	—	0.07	—	_	W	3
	32-bit, 66 MHz	—	0.13	—	—		
	32-bit, 133 MHz	—	0.24	—	—		
	32-bit, 167 MHz	—	0.30	—	—		
RapidIO I/O	500 MHz data rate	—	0.96	—	_	W	4
TSEC I/O	MII	—	—	10	—	mW	5, 6
	GMII, TBI (2.5 V)	—	—	—	40		
	GMII, TBI (3.3 V)	—	—	70	—		
	RGMII, RTBI	—	—	—	40		
CPM-FCC	MII	—	15	—	—	mW	7
	RMII	—	13	—	—		
	HDLC 16 Mbps	—	9	—	—		
	UTOPIA-8 SPHY	—	60	—	—		
	UTOPIA-8 MPHY	—	100	—	—		
	UTOPIA-16 SPHY	—	94	—	—		
	UTOPIA-16 MPHY	_	135	_	_		
CPM-SCC	HDLC 16 Mbps	—	4		—	mW	7

Table 6. Estimated Typical I/O Power Consumption

6.2.2 DDR SDRAM Output AC Timing Specifications

For chip selects $\overline{\text{MCS1}}$ and $\overline{\text{MCS2}}$, there will always be at least 200 DDR memory clocks coming out of self-refresh after an $\overline{\text{HRESET}}$ before a precharge occurs. This will not necessarily be the case for chip selects $\overline{\text{MCS0}}$ and $\overline{\text{MCS3}}$.

6.2.2.1 DLL Enabled Mode

Table 16 and Table 17 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface with the DDR DLL enabled.

Table 16. DDR SDRAM Output AC Timing Specifications-DLL Mode

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, (MCK[n]/MCK[n] crossing)	t _{MCK}	6	10	ns	2
On chip Clock Skew	t _{MCKSKEW}	—	150	ps	3, 8
MCK[n] duty cycle	t _{MCKH} /t _{MCK}	45	55	%	8
ADDR/CMD output valid	t _{DDKHOV}	—	3	ns	4, 9
ADDR/CMD output invalid	t _{DDKHOX}	1	—	ns	4, 9
Write CMD to first MDQS capture edge	t _{DDSHMH}	t _{MCK} + 1.5	t _{MCK} + 4.0	ns	5
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	^t ddkhds, ^t ddklds	900 1100 1200	_	ps	6, 9
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	^t DDKHDX, ^t DDKLDX	900 1100 1200	_	ps	6, 9
MDQS preamble start	t _{DDSHMP}	$0.75 imes t_{MCK} + 1.5$	$0.75 imes t_{MCK} + 4.0$	ns	7, 8

Parameters	Symbol	Min	Мах	Unit
Supply voltage 2.5 V	LV _{DD}	2.37	2.63	V
Output high voltage (LV _{DD} = Min, $I_{OH} = -1.0$ mA)	V _{OH}	2.00	LV _{DD} + 0.3	V
Output low voltage (LV _{DD} = Min, I_{OL} = 1.0 mA)	V _{OL}	GND – 0.3	0.40	V
Input high voltage	V _{IH}	1.70	LV _{DD} + 0.3	V
Input low voltage	V _{IL}	-0.3	0.70	V
Input high current (V_{IN} ¹ = LV_{DD})	Ι _Η	—	10	μA
Input low current (V _{IN} ¹ = GND)	IIL	-15	—	μA

Table 20. GMII, MII, RGMII, RTBI, and TBI DC Electrical Characteristics

Note:

1.Note that the symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

7.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

7.2.1 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

7.2.1.1 GMII Transmit AC Timing Specifications

Table 21 provides the GMII transmit AC timing specifications.

Table 21. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V \pm 5%, or LV_{DD}=2.5V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
GTX_CLK clock period	t _{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t _{GTXH} /t _{GTX}	40	—	60	%
GMII data TXD[7:0], TX_ER, TX_EN setup time	t _{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t _{GTKHDX} ³	0.5	_	5.0	ns

7.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

7.2.3.1 TBI Transmit AC Timing Specifications

Table 25 provides the TBI transmit AC timing specifications.

Table 25. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
GTX_CLK clock period	t _{TTX}	—	8.0	_	ns
GTX_CLK duty cycle	t _{TTXH} /t _{TTX}	40	—	60	%
TCG[9:0] setup time GTX_CLK going high	t _{TTKHDV}	2.0	—	_	ns
TCG[9:0] hold time from GTX_CLK going high	t _{TTKHDX}	1.0	—	_	ns
GTX_CLK clock rise and fall time	t _{TTXR} , t _{TTXF} ^{2,3}		—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of t(first two letters of functional block)(signal)(state

)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2.Signal timings are measured at 0.7 V and 1.9 V voltage levels.

3.Guaranteed by design.

Figure 12 shows the TBI transmit AC timing diagram.



Figure 12. TBI Transmit AC Timing Diagram

	[1
Parameter	POR Configuration	Symbol ¹	Min	Max	Unit	Notes
Input setup to local bus clock (except LUPWAIT)	—	t _{LBIVKH1}	1.8	—	ns	4, 5, 8
LUPWAIT input setup to local bus clock	—	t _{LBIVKH2}	1.7	—	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	—	t _{LBIXKH1}	0.5	—	ns	4, 5, 8
LUPWAIT input hold from local bus clock	—	t _{LBIXKH2}	1.0	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	—	t _{lbotot}	1.5	—	ns	6
Local bus clock to output valid (except	TSEC2_TXD[6:5] = 00	t _{LBKHOV1}	_	2.0	ns	4, 8
LAD/LDP and LALE)	TSEC2_TXD[6:5] = 11 (default)			3.5		
Local bus clock to data valid for LAD/LDP	TSEC2_TXD[6:5] = 00	t _{LBKHOV2}	_	2.2	ns	4, 8
	TSEC2_TXD[6:5] = 11 (default)			3.7		
Local bus clock to address valid for LAD	TSEC2_TXD[6:5] = 00	t _{LBKHOV3}	_	2.3	ns	4, 8
	TSEC2_TXD[6:5] = 11 (default)			3.8		
Local bus clock to LALE assertion		t _{LBKHOV4}		2.3	ns	4, 8
Output hold from local bus clock (except	TSEC2_TXD[6:5] = 00	t _{LBKHOX1}	0.7	—	ns	4, 8
LAD/LDF and LALE)	TSEC2_TXD[6:5] = 11 (default)		1.6			
Output hold from local bus clock for	TSEC2_TXD[6:5] = 00	t _{LBKHOX2}	0.7	—	ns	4, 8
LAD/LDP	TSEC2_TXD[6:5] = 11 (default)		1.6			
Local bus clock to output high Impedance	TSEC2_TXD[6:5] = 00	t _{LBKHOZ1}	_	2.5	ns	7, 9
(except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 11 (default)			3.8		

Table 31. Local Bus General Timing Parameters—DLL Enabled (continued)

10 JTAG

JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8560.

Table 39 provides the JTAG AC timing specifications as defined in Figure 32 through Figure 35.

Table 39. JTAG AC Timing Specifications (Independent of SYSCLK)¹

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Мах	Unit	Notes
JTAG external clock frequency of operation	f _{JTG}	0	33.3	MHz	_
JTAG external clock cycle time	t _{JTG}	30	—	ns	_
JTAG external clock pulse width measured at 1.4 V	t _{JTKHKL}	15	—	ns	_
JTAG external clock rise and fall times	t _{JTGR} & t _{JTGF}	0	2	ns	6
TRST assert time	t _{TRST}	25	_	ns	3
Input setup times: Boundary-scan data TMS, TDI	t _{JTDVKH} t _{JTIVKH}	4 0		ns	4
Input hold times: Boundary-scan data TMS, TDI	t _{JTDXKH} t _{JTIXKH}	20 25	—	ns	4
Valid times: Boundary-scan data TDO	^t jtkldv ^t jtklov	4 4	20 25	ns	5
Output hold times: Boundary-scan data TDO	^t jtkldx ^t jtklox		—	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	t _{jtkldz} t _{jtkloz}	3 3	19 9	ns	5, 6

Notes:

2. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)}

(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

4.Non-JTAG signal input timing with respect to t_{TCLK}.

5.Non-JTAG signal output timing with respect to t_{TCLK} .

6. Guaranteed by design.

^{1.}All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50- Ω load (see Figure 31). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

Figure 31 provides the AC test load for TDO and the boundary-scan outputs of the MPC8560.



Figure 31. AC Test Load for the JTAG Interface

Figure 32 provides the JTAG clock input timing diagram.



VM = Midpoint Voltage (OV_{DD}/2)

Figure 32. JTAG Clock Input Timing Diagram

Figure 33 provides the $\overline{\text{TRST}}$ timing diagram.



Figure 34 provides the boundary-scan timing diagram.



VM = Midpoint Voltage (OV_{DD}/2)



Figure 35 provides the test access port timing diagram.



Figure 35. Test Access Port Timing Diagram

11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8560.

11.1 I²C DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the I²C interface of the MPC8560.

Table 40. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V \pm 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
Input high voltage level	V _{IH}	$0.7 imes OV_{DD}$	OV _{DD} + 0.3	V	_
Input low voltage level	V _{IL}	-0.3	$0.3\times\text{OV}_{\text{DD}}$	V	
Low level output voltage	V _{OL}	0	$0.2\times\text{OV}_{\text{DD}}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t _{i2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between 0.1 \times OV_{DD} and 0.9 \times OV_{DD}(max)	lı	-10	10	μA	3
Capacitance for each I/O pin	CI	_	10	pF	_

Notes:

1.Output voltage (open drain or open collector) condition = 3 mA sink current.

2.Refer to the *MPC8560 PowerQUICC III Integrated Communications Processor Preliminary Reference Manual* for information on the digital filter used.

3.I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

MPC8560 Integrated Processor Hardware Specifications, Rev. 4.2

I2C

Package and Pin Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes			
JTAG							
тск	AF21	I	OV _{DD}	_			
TDI	AG21	I	OV _{DD}	12			
TDO	AF19	0	OV _{DD}	11			
TMS	AF23	I	OV _{DD}	12			
TRST	AG23	I	OV _{DD}	12			
	DFT						
LSSD_MODE	AG19	I	OV _{DD}	21			
L1_TSTCLK	AB22	I	OV _{DD}	21			
L2_TSTCLK	AG22	I	OV _{DD}	21			
TEST_SEL	AH20	I	OV _{DD}	3			
	Thermal Management						
THERM0	AG2	I	—	14			
THERM1	AH3	I	—	14			
	Power Management						
ASLEEP	AG18	I/O		9, 19			
Power and Ground Signals							
AV _{DD} 1	AH19	Power for e500 PLL (1.2 V)	AV _{DD} 1	_			
AV _{DD} 2	AH18	Power for CCB PLL (1.2 V)	AV _{DD} 2	_			
AV _{DD} 3	AH17	Power for CPM PLL (1.2 V)	AV _{DD} 3	_			
GND	 A12, A17, B3, B14, B20, B26, B27, C2, C4, C11,C17, C19, C22, C27, D8, E3, E12, E24, F11, F18, F23, G9, G12, G25, H4, H12, H14, H17, H20, H22, H27, J19, J24, K5, K9, K18, K23, K28, L6, L20, L25, M4, M12, M14, M16, M22, M27, N2, N13, N15, N17, P12, P14, P16, P23, R13, R15, R17, R20, R26, T3, T8, T10, T12, T14, T16, U6, U13, U15, U16, U17, U21, V7, V10, V26, W5, W18, W23, Y8, Y16, AA6, AA13, AB4, AB11, AB19, AC6, AC9, AD3, AD8, AD17, AF2, AF4, AF10, AF13, AF15, AF27, AG3, AG7, AG26 	_	—	_			
GV _{DD}	A14, A20, A25, A26, A27, A28, B17, B22, B28, C12, C28, D16, D19, D21, D24, D28, E17, E22, F12, F15, F19, F25, G13, G18, G20, G23, G28, H19, H24, J12, J17, J22, J27, K15, K20, K25, L13, L23, L28, M25, N21	Power for DDR DRAM I/O Voltage (2.5 V)	GV _{DD}	_			

15 Clocking

This section describes the PLL configuration of the MPC8560. Note that the platform clock is identical to the CCB clock.

15.1 Clock Ranges

Table 55 provides the clocking specifications for the processor core and Table 56 provides the clocking specifications for the memory bus.

Characteristic	Maximum Processor Core Frequency							
	667 MHz		833 MHz		1 GHz		Unit	Notes
	Min	Мах	Min	Max	Min	Мах		
e500 core processor frequency	400	667	400	833	400	1000	MHz	1, 2, 3

Table 55. Processor Core Clocking Specifications

Notes:

1.Caution: The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, "Platform/System PLL Ratio," and Section 15.3, "e500 Core PLL Ratio," for ratio settings.

2.) The minimum e500 core frequency is based on the minimum platform frequency of 200 MHz.

3.)The 1.0 GHz core frequency is based on a 1.3 V VDD supply voltage.

Table 56. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency							
	667 MHz		833 MHz		1 GHz		Unit	Notes
	Min	Max	Min	Max	Min	Max		
Memory bus frequency	100	166	100	166	100	166	MHz	1, 2, 3

Notes:

Caution: The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, "Platform/System PLL Ratio," and Section 15.3, "e500 Core PLL Ratio," for ratio settings.

2. The memory bus speed is half of the DDR data rate, hence, half of the platform clock frequency.

3.) The 1.0 GHz core frequency is based on a 1.3 V VDD supply voltage.

15.2 Platform/System PLL Ratio

The platform clock is the clock that drives the L2 cache, the DDR SDRAM data rate, and the e500 core complex bus (CCB), and is also called the CCB clock. The values are determined by the binary value on LA[28:31] at power up, as shown in Table 57.

There is no default for this PLL ratio; these signals must be pulled to the desired values.

Binary Value of LA[28:31] Signals	Ratio Description
0000	16:1 ratio CCB clock: SYSCLK (PCI bus)
0001	Reserved
0010	2:1 ratio CCB clock: SYSCLK (PCI bus)
0011	3:1 ratio CCB clock: SYSCLK (PCI bus)
0100	4:1 ratio CCB clock: SYSCLK (PCI bus)
0101	5:1 ratio CCB clock: SYSCLK (PCI bus)
0110	6:1 ratio CCB clock: SYSCLK (PCI bus)
0111	Reserved
1000	8:1 ratio CCB clock: SYSCLK (PCI bus)
1001	9:1 ratio CCB clock: SYSCLK (PCI bus)
1010	10:1 ratio CCB clock: SYSCLK (PCI bus)
1011	Reserved
1100	12:1 ratio CCB clock: SYSCLK (PCI bus)
1101	Reserved
1110	Reserved
1111	Reserved

Table 57. CCB Clock Ratio

15.3 e500 Core PLL Ratio

Table 58 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LALE and LGPL2 at power up, as shown in Table 58.

Table 58.	e500	Core to	ССВ	Ratio
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Binary Value of LALE, LGPL2 Signals	Ratio Description
00	2:1 e500 core:CCB
01	5:2 e500 core:CCB
10	3:1 e500 core:CCB
11	7:2 e500 core:CCB

Thermal

Figure 53 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 53. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

16.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 54 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 51). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink, the heat sink should be slowly removed. Heating the heat sink to 40-50°C with an air gun can soften the interface material and make the removal easier. The use of an adhesive for heat sink attach is not recommended.

Thermal

ltem No	QTY	MEI PN	Description
1	1	MFRAME-2000	HEATSINK FRAME
2	1	MSNK-1120	EXTRUDED HEATSINK
3	1	MCLIP-1013	CLIP
4	4	MPPINS-1000	FRAME ATTACHMENT PINS



Illustrative source provided by Millennium Electronics (MEI)

Figure 57. Exploded Views (2) of a Heat Sink Attachment using a Plastic Fence

The die junction-to-ambient and the heat sink-to-ambient thermal resistances are common figure-of-merits used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature: airflow, board population (local heat flux of adjacent components), system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the boards, as well as, system-level designs.

Figure 58 shows the PLL power supply filter circuit.



Figure 58. PLL Power Supply Filter Circuit

17.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8560 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8560 system, and the MPC8560 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pins of the MPC8560. These decoupling capacitors should receive their power from separate V_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μ F (AVX TPS tantalum or Sanyo OSCON).

17.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} , GV_{DD} , or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , GV_{DD} , LV_{DD} , OV_{DD} , and GND pins of the MPC8560.

17.5 Output Buffer DC Impedance

The MPC8560 drivers are characterized over process, voltage, and temperature. There are two driver types: a push-pull single-ended driver (open drain for I^2C) for all buses except RapidIO, and a current-steering differential driver for the RapidIO port.

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 59). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices.

Rev. No.	Substantive Change(s)
3.2	Updated Table 1 and Table 2 with 1.0 GHz device parameter requirements. Added Section 2.1.2, "Power Sequencing". Added CPM port signal drive strength to Table 3. Updated Table 4 with Maximum power data. Updated Table 4 and Table 5 with 1 GHz speed grade information. Updated Table 6 with corrected typical I/O power numbers. Updated Table 7 Note 2 lower voltage measurement point. Replaced Table 7 Note 5 with spread spectrum clocking guidelines. Added to Table 8 rise and fall time information.
	Added Section 4.4, "Real Time Clock Timing". Added precharge information to Section 6.2.2, "DDR SDRAM Output AC Timing Specifications". Removed V_{IL} and V_{IH} references from Table 21, Table 22, Table 23, and Table 24. Added reference level note to Table 21, Table 22, Table 23, Table 24, Table 25, Table 26, and Table 27. Updated TXD references to TCG in Section 7.2.3.1, "TBI Transmit AC Timing Specifications". Updated t _{TTKHDX} value in Table 25. Updated PMA_RX_CLK references to RX_CLK in Section 7.2.3.2, "TBI Receive AC Timing Specifications". Updated RXD references to RCG in Section 7.2.3.2, "TBI Receive AC Timing Specifications". Updated Table 27 Note 2. Corrected Table 29 f _{MDC} and t _{MDC} to reflect the correct minimum operating frequency. Updated Table 29 t _{MDKHDV} and t _{MDKHDX} values for clarification. Added t _{LBKHKT} and updated Note 2 in Table 32. Corrected LGTA timing references in Figure 17. Updated Figure 18, Figure 20, and Figure 22. Corrected FCC output timing reference labels in Figure 24 and Figure 25. Updated Figure 50. Clarified Table 54 Note 5. Updated Table 55 and Table 56 with 1 GHz information.
	Added heat sink removal discussion to Section 16.2.3, "Thermal Interface Materials". Corrected and added 1 GHz part number to Table 63.
3.1	Updated Table 4 and Table 5. Added Table 6. Added MCK duty cycle to Table 16. Updated f_{MDC} , t_{MDC} , t_{MDKHDV} , and t_{MDKHDX} parameters in Table 29. Added LALE to $t_{LBKHOV3}$ parameter in Table 31 and Table 32, and updated Figure 17. Corrected active level designations of some of the pins in Table 54. Updated Table 63.

Table 62. Document Revision History (continued)

19.2 Part Marking

Parts are marked as the example shown in Figure 62.



Notes:

MMMMM is the 5-digit mask number.

ATWLYYWWA is the traceability code.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States. YWWLAZ is the assembly traceability code.

Figure 62. Part Marking for FC-PBGA Device