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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	833MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8560vt833lb

- System performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the 8 counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- System access port
  - Uses JTAG interface and a TAP controller to access entire system memory map
  - Supports 32-bit accesses to configuration registers
  - Supports cache-line burst accesses to main memory
  - Supports large block (4-Kbyte) uploads and downloads
  - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1™-compliant, JTAG boundary scan
- 783 FC-PBGA package

2 Electrical Characteristics

This section provides the electrical specifications and thermal characteristics for the MPC8560. The MPC8560 is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

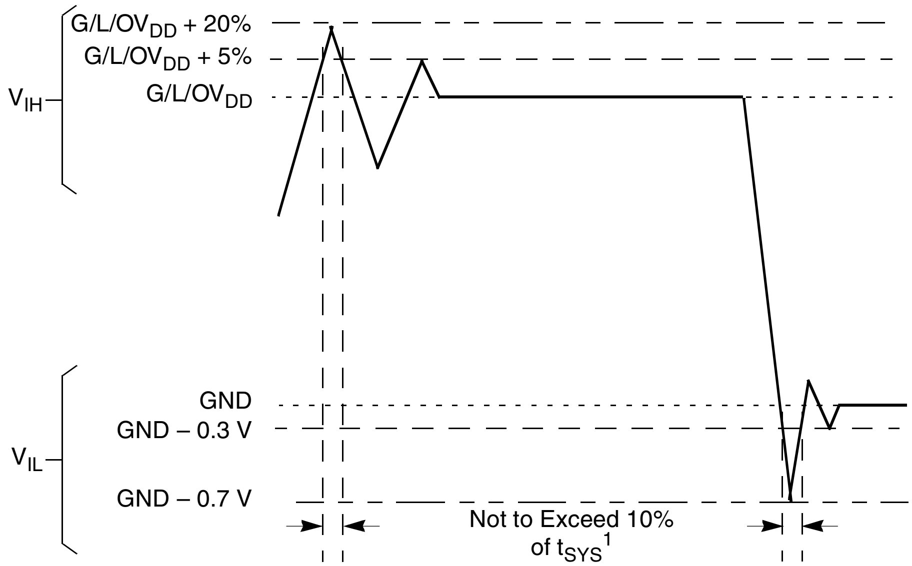
2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings [1]

Characteristic	Symbol	Max Value	Unit	Notes
Core supply voltage For devices rated at 667 and 833 MHz For devices rated at 1 GHz	V_{DD}	 –0.3 to 1.32 –0.3 to 1.43	V	—
PLL supply voltage For devices rated at 667 and 833 MHz For devices rated at 1 GHz	AV_{DD}	 –0.3 to 1.32 –0.3 to 1.43	V	—

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8560.



Note:
t_{SYS} refers to the clock period associated with the SYSCLK signal.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

The MPC8560 core voltage must always be provided at nominal 1.2 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

7.2.2.2 MII Receive AC Timing Specifications

Table 24 provides the MII receive AC timing specifications.

Table 24. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX} [3]	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise and fall time	t_{MRXR}, t_{MRXF} [2,3]	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 11 shows the MII receive AC timing diagram.

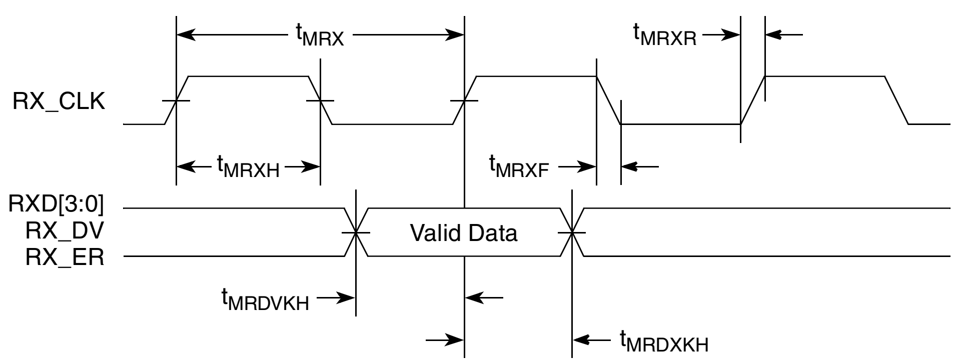


Figure 11. MII Receive AC Timing Diagram

7.2.4 RGMII and RTBI AC Timing Specifications

Table 27 presents the RGMII and RTBI AC timing specifications.

Table 27. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT} [5]	–500	0	500	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns
Clock period[3]	t_{RGT} [6]	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4]	t_{RGTH}/t_{RGT} [6]	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3]	t_{RGTH}/t_{RGT} [6]	40	50	60	%
Rise and fall time	t_{RGTR}, t_{RGTF} [6,7]	—	—	0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. The RGMII specification requires that PC board designer add 1.5 ns or greater in trace delay to the RX_CLK in order to meet this specification. However, as stated above, this device will function with only 1.0 ns of delay.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by characterization.
6. Guaranteed by design.
7. Signal timings are measured at 0.5 V and 2.0 V voltage levels.

Figure 14 shows the RGMII and RTBI AC timing and multiplexing diagrams.

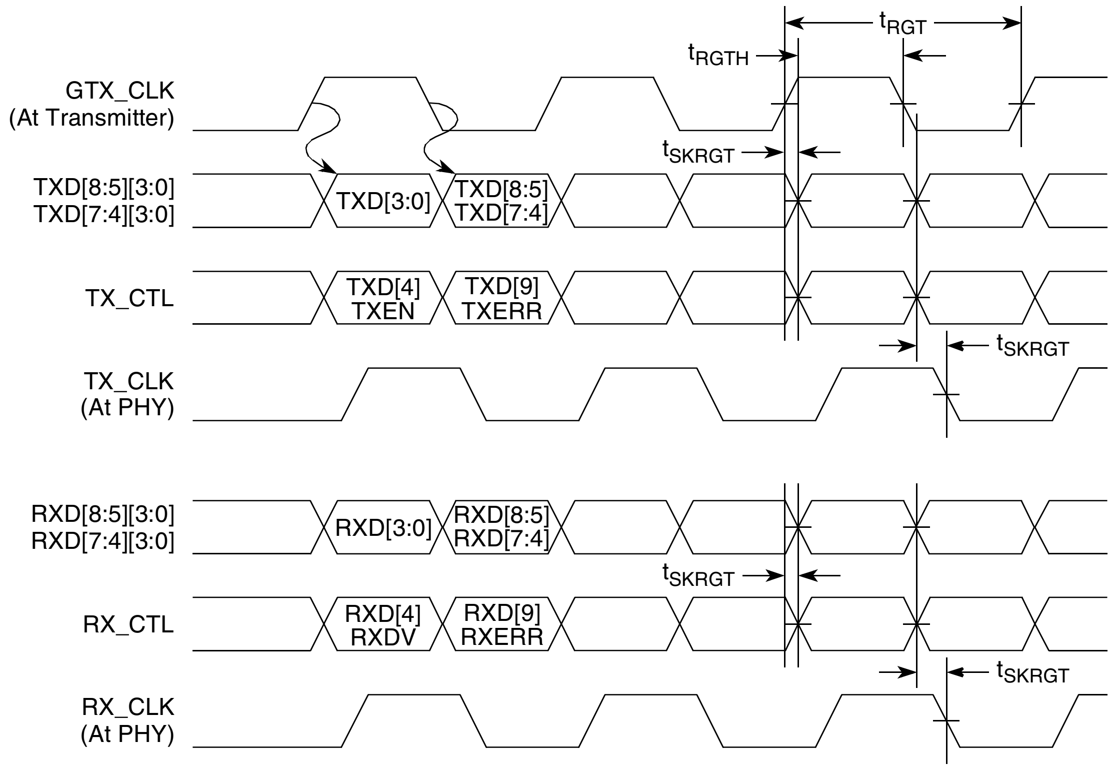


Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

7.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 7.1, "Three-Speed Ethernet Controller (TSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics."

7.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 28.

Table 28. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.13	3.47	V
Output high voltage (OV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	1.70	—	V
Input low voltage	V_{IL}	—	0.90	V

Figure 24 shows the FCC internal clock.

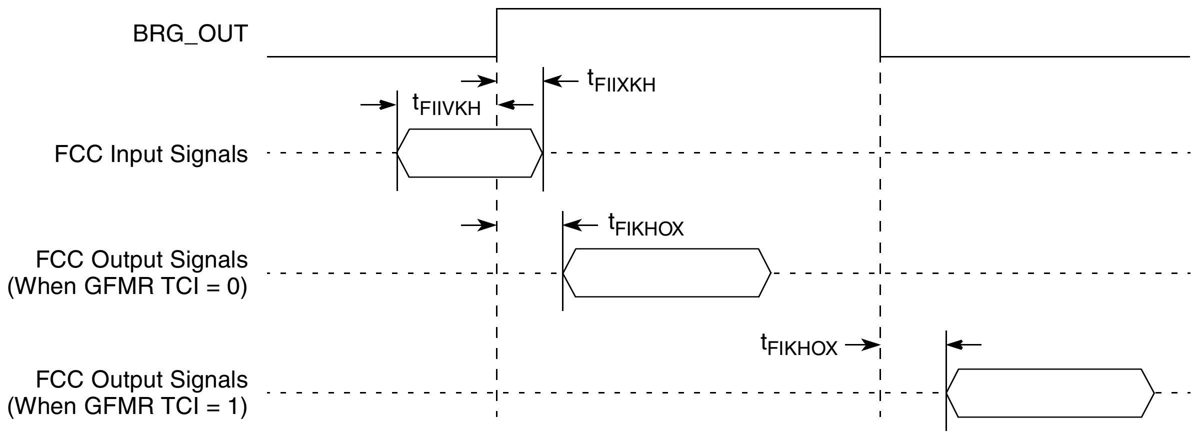


Figure 24. FCC Internal AC Timing Clock Diagram

Figure 25 shows the FCC external clock.

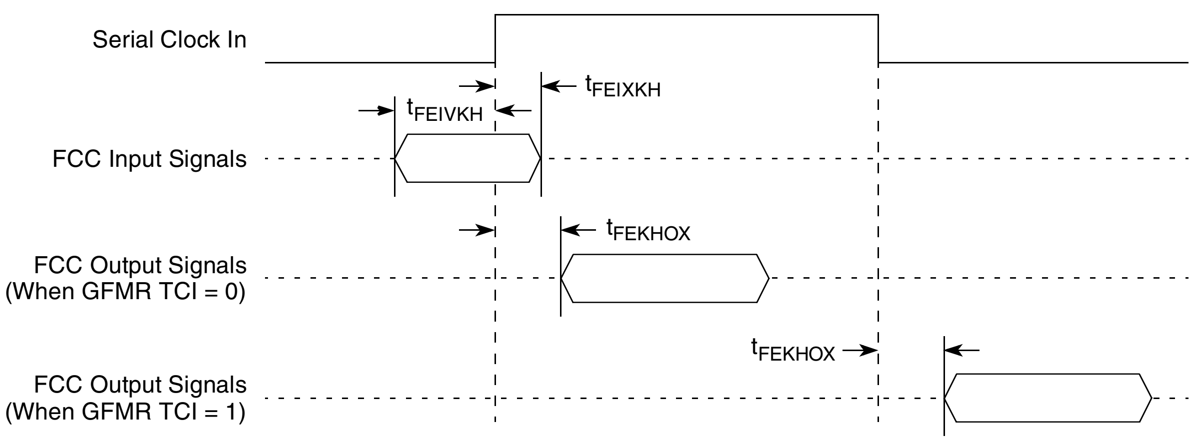


Figure 25. FCC External AC Timing Clock Diagram

Figure 26 shows Ethernet collision timing on FCCs.

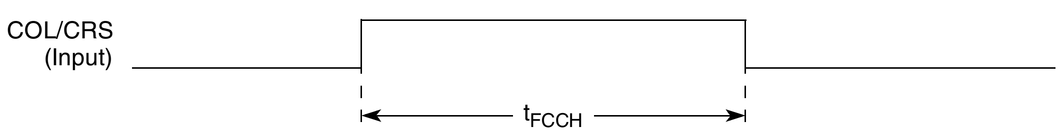


Figure 26. Ethernet Collision AC Timing Diagram (FCC)

Figure 16 provides the AC test load for PCI and PCI-X.

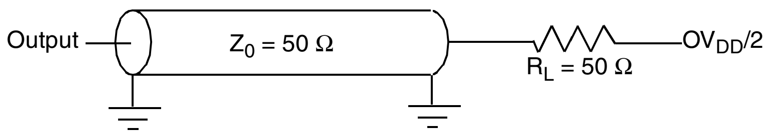


Figure 38. PCI/PCI-X AC Test Load

Figure 39 shows the PCI/PCI-X input AC timing conditions.

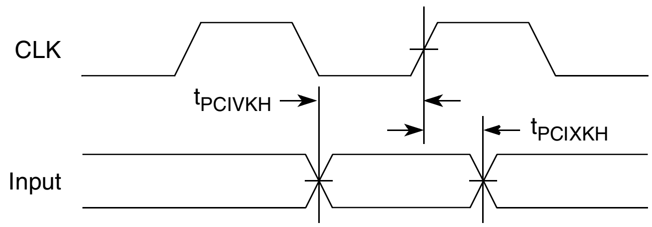


Figure 39. PCI-PCI-X Input AC Timing Measurement Conditions

Figure 40 shows the PCI/PCI-X output AC timing conditions.

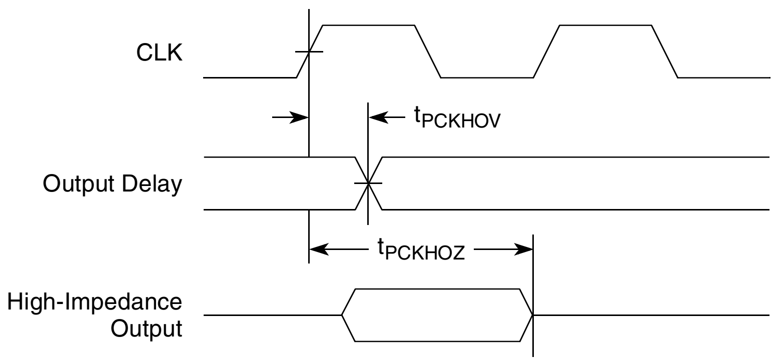


Figure 40. PCI-PCI-X Output AC Timing Measurement Condition

Table 44 provides the PCI-X AC timing specifications at 66 MHz.

Table 44. PCI-X AC Timing Specifications at 66 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	—	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t_{PCKHOX}	0.7	—	ns	1, 10
SYSCLK to output high impedance	t_{PCKHOZ}	—	7	ns	1, 4, 8, 11
Input setup time to SYSCLK	t_{PCIVKH}	1.7	—	ns	3, 5
Input hold time from SYSCLK	t_{PCIXKH}	0.5	—	ns	10
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time	t_{PCRVRH}	10	—	clocks	11
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	11
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	9, 11

Table 44. PCI-X AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	—	clocks	11
$\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time	t_{PCRHIX}	0	50	ns	6, 11

Notes:

1. See the timing measurement conditions in the *PCI-X 1.0a Specification*.
2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
3. Setup time for point-to-point signals applies to $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ only. All other signals are bused.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
6. Maximum value is also limited by delay to the first transaction (time for $\overline{\text{HRESET}}$ high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of $\overline{\text{HRESET}}$ must be negated no later than two clocks before the first $\overline{\text{FRAME}}$ and must be floated no later than one clock before $\overline{\text{FRAME}}$ is asserted.
7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
8. Device must meet this specification independent of how many outputs switch simultaneously.
9. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification*.
10. Guaranteed by characterization.
11. Guaranteed by design.

Table 45 provides the PCI-X AC timing specifications at 133 MHz.

Table 45. PCI-X AC Timing Specifications at 133 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	—	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t_{PCKHOX}	0.7	—	ns	1, 11
SYSCLK to output high impedance	t_{PCKHOZ}	—	7	ns	1, 4, 8, 12
Input setup time to SYSCLK	t_{PCIVKH}	1.4	—	ns	3, 5, 9, 11
Input hold time from SYSCLK	t_{PCIXKH}	0.5	—	ns	11
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time	t_{PCRVRH}	10	—	clocks	12
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	12
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	10, 12
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	—	clocks	12

Figure 41 shows the DC driver signal levels.

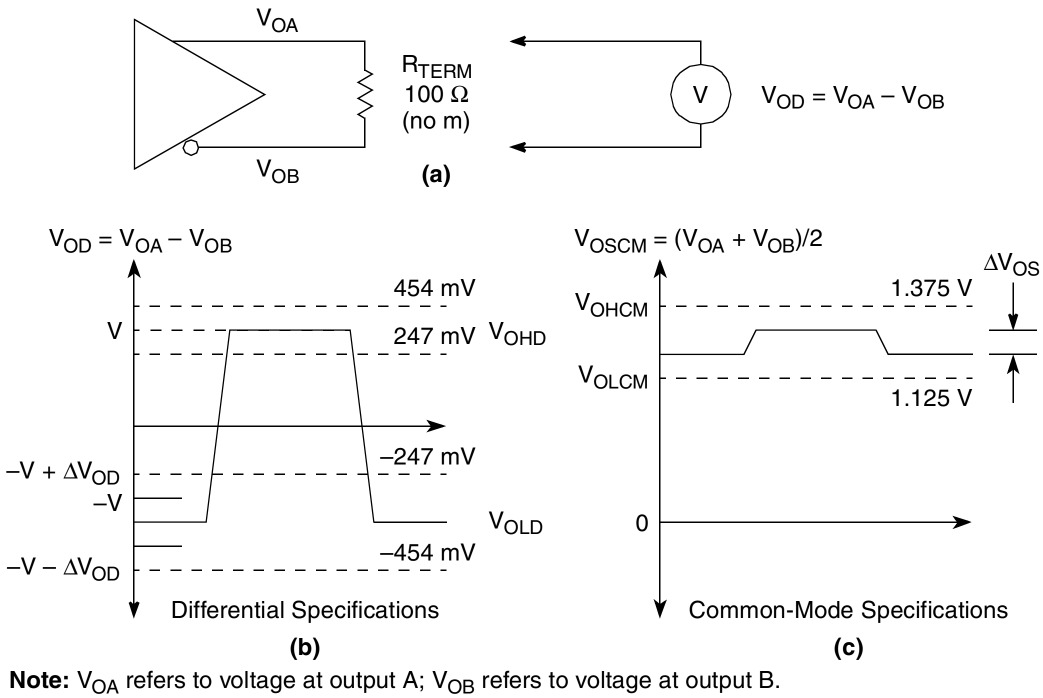


Figure 41. DC Driver Signal Levels

13.2 RapidIO AC Electrical Specifications

This section contains the AC electrical specifications for a RapidIO 8/16 LP-LVDS device. The interface defined is a parallel differential low-power high-speed signal interface. Note that the source of the transmit clock on the RapidIO interface is dependent on the settings of the LGPL[0:1] signals at reset. Note that the default setting makes the core complex bus (CCB) clock the source of the transmit clock. See Chapter 4 of the Reference Manual for more details on reset configuration settings.

13.3 RapidIO Concepts and Definitions

This section specifies signals using differential voltages. Figure 42 shows how the signals are defined. The figure shows waveforms for either a transmitter output (TD and $\overline{TD}$) or a receiver input (RD and $\overline{RD}$). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- The transmitter output and receiver input signals TD, $\overline{TD}$, RD, and $\overline{RD}$ each have a peak-to-peak swing of A-B volts.
- The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} – V_{\overline{TD}}$.
- The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} – V_{\overline{RD}}$.
- The differential output signal of the transmitter or input signal of the receiver, ranges from A – B volts to – (A – B) volts.

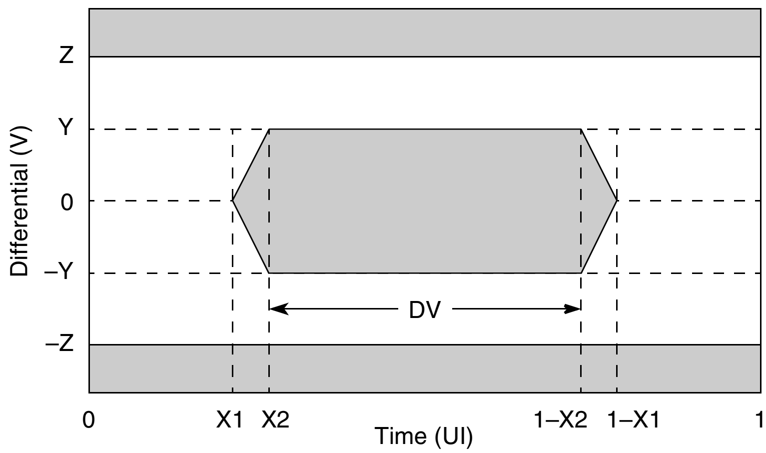


Figure 43. Example Compliance Mask

Y = minimum data valid amplitude
Z = maximum amplitude
1 UI = 1 unit interval = 1/baud rate
X1 = end of zero crossing region
X2 = beginning of data valid window
DV = data valid window = 1 – 2 × X2

The waveform of the signal under test must fall within the unshaded area of the mask to be compliant. Different masks are used for the driver output and the receiver input allowing each to be separately specified.

13.3.1 RapidIO Driver AC Timing Specifications

Driver AC timing specifications are provided in Table 48, Table 49, and Table 50. A driver shall comply with the specifications for each data rate/frequency for which operation of the driver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The output of a driver shall be connected to a 100 Ω, ±1%, differential (bridged) resistive load.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7]).

Table 48. RapidIO Driver AC Timing Specifications—500 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential output high voltage	V_{OHD}	200	540	mV	1
Differential output low voltage	V_{OLD}	–540	–200	mV	1

The eye pattern for a data signal is generated by making a large number of recordings of the signal and then overlaying the recordings. The number of recordings used to generate the eye shall be large enough that further increasing the number of recordings used does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not. Each data signal in the interface shall be carrying random or pseudo-random data when the recordings are made. If pseudo-random data is used, the length of the pseudo-random sequence (repeat length) shall be long enough that increasing the length of the sequence does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not comply with the mask. The data carried by any given data signal in the interface may not be correlated with the data carried by any other data signal in the interface. The zero-crossings of the clock associated with a data signal shall be used as the timing reference for aligning the multiple recordings of the data signal when the recordings are overlaid.

While the method used to make the recordings and overlay them to form the eye pattern is not specified, the method used shall be demonstrably equivalent to the following method. The signal under test is repeatedly recorded with a digital oscilloscope in infinite persistence mode. Each recording is triggered by a zero-crossing of the clock associated with the data signal under test. Roughly half of the recordings are triggered by positive-going clock zero-crossings and roughly half are triggered by negative-going clock zero-crossings. Each recording is at least 1.9 UI in length (to ensure that at least one complete eye is formed) and begins 0.5 UI before the trigger point (0.5 UI before the associated clock zero-crossing). Depending on the length of the individual recordings used to generate the eye pattern, one or more complete eyes will be formed. Regardless of the number of eyes, the eye whose center is immediately to the right of the trigger point is the eye used for compliance testing.

An example of an eye pattern generated using the above method with recordings 3 UI in length is shown in Figure 45. In this example, there is no skew between the signal under test and the associated clock used to trigger the recordings. If skew was present, the eye pattern would be shifted to the left or right relative to the oscilloscope trigger point.

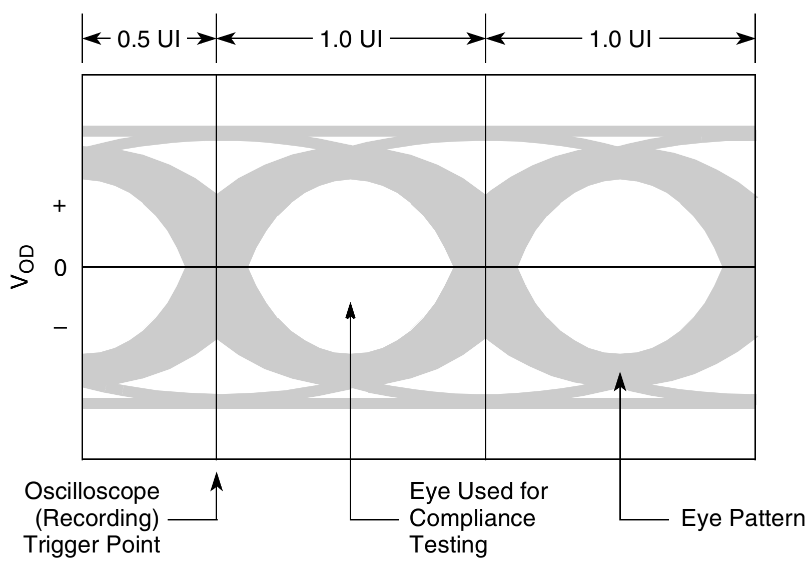


Figure 45. Example Driver Output Eye Pattern

3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
7. The socket lid must always be oriented to A1.

14.3 Pinout Listings

Table 54 provides the pin-out listing for the MPC8560, 783 FC-PBGA package.

Table 54. MPC8560 Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI/PCI-X				
PCI_AD[63:0]	AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14, V15, W15, Y15, AA15, AB15, AC15, AD15, AG15, AH15, V16, W16, AB16, AC16, AD16, AE16, AF16, V17, W17, Y17, AA17, AB17, AE17, AF17, AF18, AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9, AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11, AG11, AH11, V12, W12, Y12, AB12, AD12, AE12, AG12, AH12, V13, Y13, AB13, AC13	I/O	OV_{DD}	17
PCI_C_$\overline{\text{BE}}$[7:0]	AG13, AH13, V14, W14, AH8, AB10, AD11, AC12	I/O	OV_{DD}	17
PCI_PAR	AA11	I/O	OV_{DD}	—
PCI_PAR64	Y14	I/O	OV_{DD}	—
$\overline{\text{PCI\_FRAME}}$	AC10	I/O	OV_{DD}	2
$\overline{\text{PCI\_TRDY}}$	AG10	I/O	OV_{DD}	2
$\overline{\text{PCI\_IRDY}}$	AD10	I/O	OV_{DD}	2
$\overline{\text{PCI\_STOP}}$	V11	I/O	OV_{DD}	2
$\overline{\text{PCI\_DEVSEL}}$	AH10	I/O	OV_{DD}	2
PCI_IDSEL	AA9	I	OV_{DD}	—
$\overline{\text{PCI\_REQ64}}$	AE13	I/O	OV_{DD}	5, 10
$\overline{\text{PCI\_ACK64}}$	AD13	I/O	OV_{DD}	2
$\overline{\text{PCI\_PERR}}$	W11	I/O	OV_{DD}	2
$\overline{\text{PCI\_SERR}}$	Y11	I/O	OV_{DD}	2, 4
$\overline{\text{PCI\_REQ0}}$	AF5	I/O	OV_{DD}	—
$\overline{\text{PCI\_REQ}}$[1:4]	AF3, AE4, AG4, AE5	I	OV_{DD}	—
$\overline{\text{PCI\_GNT}}$[0]	AE6	I/O	OV_{DD}	—
$\overline{\text{PCI\_GNT}}$[1:4]	AG5, AH5, AF6, AG6	O	OV_{DD}	5, 9

Table 54. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
RIO_RD[0:7]	T25, U25, V25, W25, AA25, AB25, AC25, AD25	I	OV_{DD}	—
$\overline{\text{RIO\_RD}}$[0:7]	T24, U24, V24, W24, AA24, AB24, AC24, AD24	I	OV_{DD}	—
RIO_RFRAME	AE27	I	OV_{DD}	—
$\overline{\text{RIO\_RFRAME}}$	AE26	I	OV_{DD}	—
RIO_TCLK	AC20	O	OV_{DD}	11
$\overline{\text{RIO\_TCLK}}$	AE21	O	OV_{DD}	11
RIO_TD[0:7]	AE18, AC18, AD19, AE20, AD21, AE22, AC22, AD23	O	OV_{DD}	—
$\overline{\text{RIO\_TD}}$[0:7]	AD18, AE19, AC19, AD20, AC21, AD22, AE23, AC23	O	OV_{DD}	—
RIO_TFRAME	AE24	O	OV_{DD}	—
$\overline{\text{RIO\_TFRAME}}$	AE25	O	OV_{DD}	—
RIO_TX_CLK_IN	AF24	I	OV_{DD}	—
$\overline{\text{RIO\_TX\_CLK\_IN}}$	AF25	I	OV_{DD}	—
I^2C interface				
IIC_SDA	AH22	I/O	OV_{DD}	4, 20
IIC_SCL	AH23	I/O	OV_{DD}	4, 20
System Control				
$\overline{\text{HRESET}}$	AH16	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	AG20	O	OV_{DD}	—
$\overline{\text{SRESET}}$	AF20	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN}}$	M11	I	OV_{DD}	—
$\overline{\text{CKSTP\_OUT}}$	G1	O	OV_{DD}	2, 4
Debug				
TRIG_IN	N12	I	OV_{DD}	—
TRIG_OUT/READY	G2	O	OV_{DD}	6, 9, 19
MSRCID[0:1]	J9, G3	O	OV_{DD}	5, 6, 9
MSRCID[2:4]	F3, F5, F2	O	OV_{DD}	6
MDVAL	F4	O	OV_{DD}	6
Clock				
SYSCLK	AH21	I	OV_{DD}	—
RTC	AB23	I	OV_{DD}	—
CLK_OUT	AF22	O	OV_{DD}	11

15.2 Platform/System PLL Ratio

The platform clock is the clock that drives the L2 cache, the DDR SDRAM data rate, and the e500 core complex bus (CCB), and is also called the CCB clock. The values are determined by the binary value on LA[28:31] at power up, as shown in Table 57.

There is no default for this PLL ratio; these signals must be pulled to the desired values.

Table 57. CCB Clock Ratio

Binary Value of LA[28:31] Signals	Ratio Description
0000	16:1 ratio CCB clock: SYSCLK (PCI bus)
0001	Reserved
0010	2:1 ratio CCB clock: SYSCLK (PCI bus)
0011	3:1 ratio CCB clock: SYSCLK (PCI bus)
0100	4:1 ratio CCB clock: SYSCLK (PCI bus)
0101	5:1 ratio CCB clock: SYSCLK (PCI bus)
0110	6:1 ratio CCB clock: SYSCLK (PCI bus)
0111	Reserved
1000	8:1 ratio CCB clock: SYSCLK (PCI bus)
1001	9:1 ratio CCB clock: SYSCLK (PCI bus)
1010	10:1 ratio CCB clock: SYSCLK (PCI bus)
1011	Reserved
1100	12:1 ratio CCB clock: SYSCLK (PCI bus)
1101	Reserved
1110	Reserved
1111	Reserved

15.3 e500 Core PLL Ratio

Table 58 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LALE and LGPL2 at power up, as shown in Table 58.

Table 58. e500 Core to CCB Ratio

Binary Value of LALE, LGPL2 Signals	Ratio Description
00	2:1 e500 core:CCB
01	5:2 e500 core:CCB
10	3:1 e500 core:CCB
11	7:2 e500 core:CCB

The spring mounting should be designed to apply the force only directly above the die. By localizing the force, rocking of the heat sink is minimized. One suggested mounting method attaches a plastic fence to the board to provide the structure on which the heat sink spring clips. The plastic fence also provides the opportunity to minimize the holes in the printed-circuit board and to locate them at the corners of the package. Figure 56 and Figure 57 provide exploded views of the plastic fence, heat sink, and spring clip.

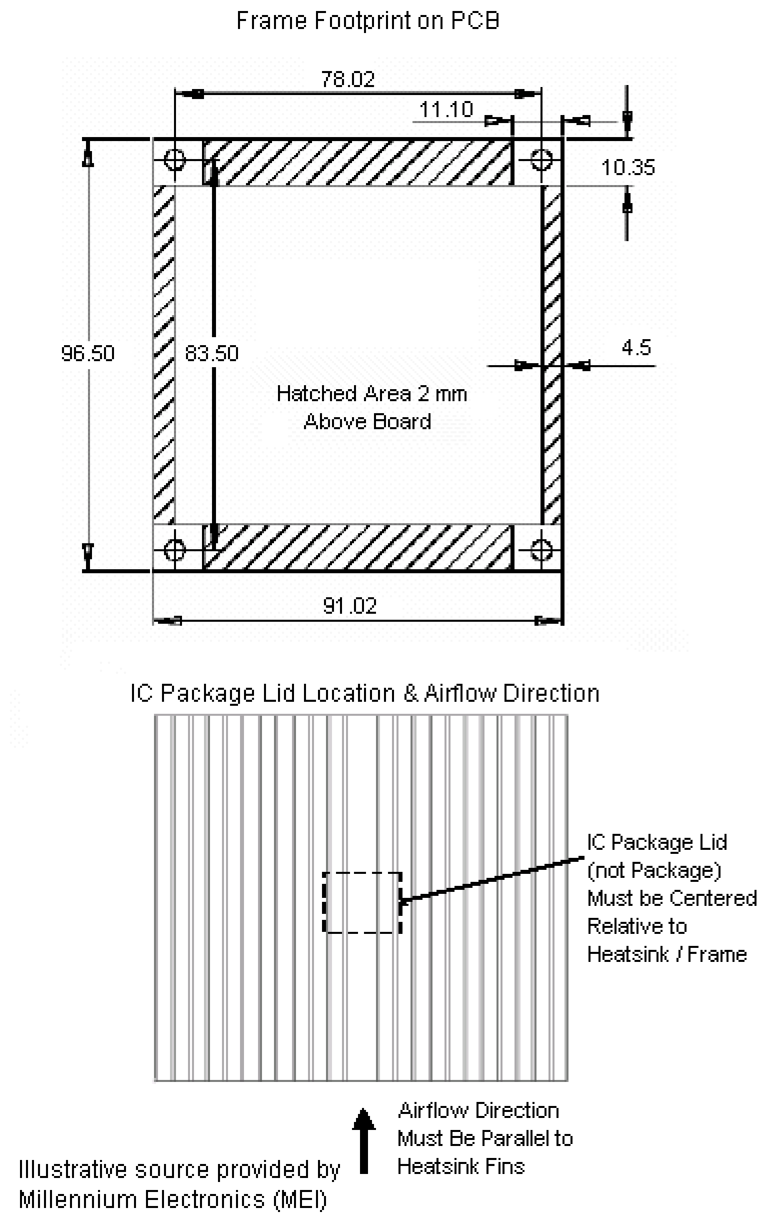
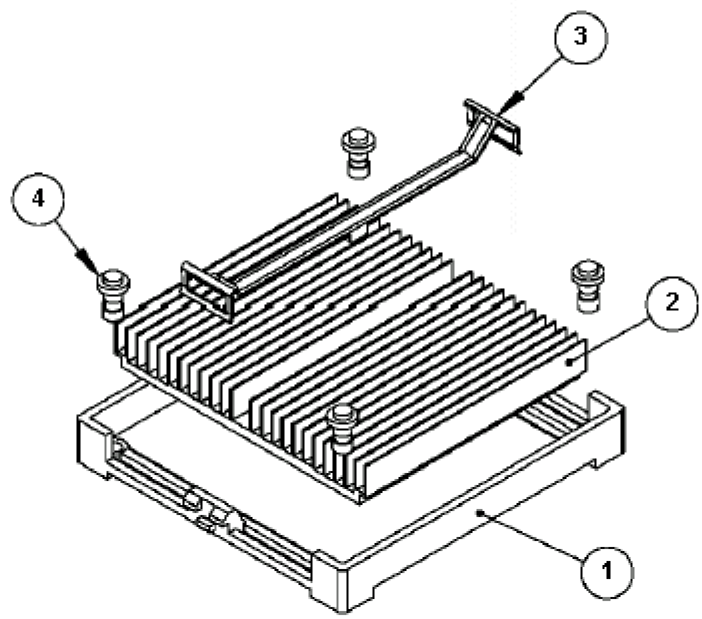


Figure 56. Exploded Views (1) of a Heat Sink Attachment using a Plastic Force

Item No	QTY	MEI PN	Description
1	1	MFRAME-2000	HEATSINK FRAME
2	1	MSNK-1120	EXTRUDED HEATSINK
3	1	MCLIP-1013	CLIP
4	4	MPPINS-1000	FRAME ATTACHMENT PINS



Illustrative source provided by
Millennium Electronics (MEI)

Figure 57. Exploded Views (2) of a Heat Sink Attachment using a Plastic Fence

The die junction-to-ambient and the heat sink-to-ambient thermal resistances are common figure-of-merits used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature: airflow, board population (local heat flux of adjacent components), system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the boards, as well as, system-level designs.

When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

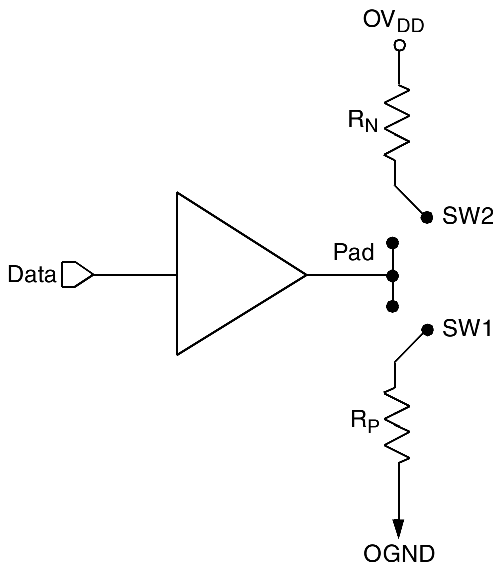


Figure 59. Driver Impedance Measurement

The output impedance of the RapidIO port drivers targets 200-Ω differential resistance. The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 61 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 61. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI/PCI-X	DDR DRAM	RapidIO	Symbol	Unit
R_N	43 Target	25 Target	20 Target	NA	Z_0	W
R_P	43 Target	25 Target	20 Target	NA	Z_0	W
Differential	NA	NA	NA	200 Target	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

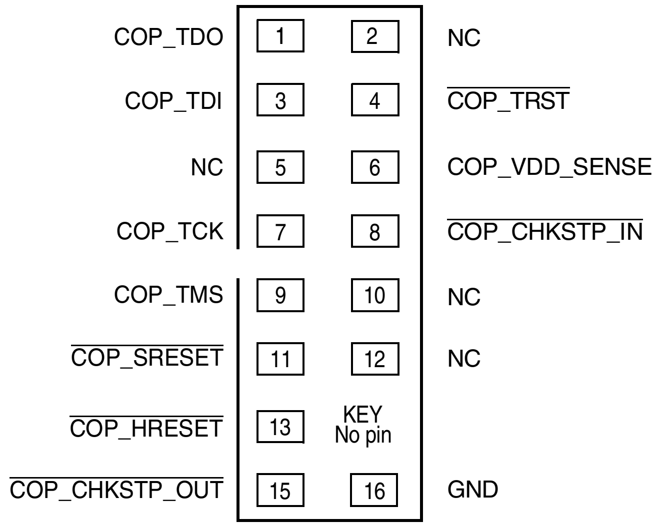


Figure 60. COP Connector Physical Pinout

17.8.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 61. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 kΩ resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

Table 62. Document Revision History (continued)

Rev. No.	Substantive Change(s)
3.2	Updated Table 1 and Table 2 with 1.0 GHz device parameter requirements. Added Section 2.1.2, “Power Sequencing”. Added CPM port signal drive strength to Table 3. Updated Table 4 with Maximum power data. Updated Table 4 and Table 5 with 1 GHz speed grade information. Updated Table 6 with corrected typical I/O power numbers. Updated Table 7 Note 2 lower voltage measurement point. Replaced Table 7 Note 5 with spread spectrum clocking guidelines. Added to Table 8 rise and fall time information. Added Section 4.4, “Real Time Clock Timing”. Added precharge information to Section 6.2.2, “DDR SDRAM Output AC Timing Specifications”. Removed V_{IL} and V_{IH} references from Table 21, Table 22, Table 23, and Table 24. Added reference level note to Table 21, Table 22, Table 23, Table 24, Table 25, Table 26, and Table 27. Updated TXD references to TCG in Section 7.2.3.1, “TBI Transmit AC Timing Specifications”. Updated t_{TTKHDX} value in Table 25. Updated PMA_RX_CLK references to RX_CLK in Section 7.2.3.2, “TBI Receive AC Timing Specifications”. Updated RXD references to RCG in Section 7.2.3.2, “TBI Receive AC Timing Specifications”. Updated Table 27 Note 2. Corrected Table 29 f_{MDC} and t_{MDC} to reflect the correct minimum operating frequency. Updated Table 29 t_{MDKHDV} and t_{MDKHDX} values for clarification. Added t_{LBKHKT} and updated Note 2 in Table 32. Corrected $\overline{\text{LGTA}}$ timing references in Figure 17. Updated Figure 18, Figure 20, and Figure 22. Corrected FCC output timing reference labels in Figure 24 and Figure 25. Updated Figure 50. Clarified Table 54 Note 5. Updated Table 55 and Table 56 with 1 GHz information. Added heat sink removal discussion to Section 16.2.3, “Thermal Interface Materials”. Corrected and added 1 GHz part number to Table 63.
3.1	Updated Table 4 and Table 5. Added Table 6. Added MCK duty cycle to Table 16. Updated f_{MDC}, t_{MDC}, t_{MDKHDV}, and t_{MDKHDX} parameters in Table 29. Added LALE to $t_{LBKHOV3}$ parameter in Table 31 and Table 32, and updated Figure 17. Corrected active level designations of some of the pins in Table 54. Updated Table 63.

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