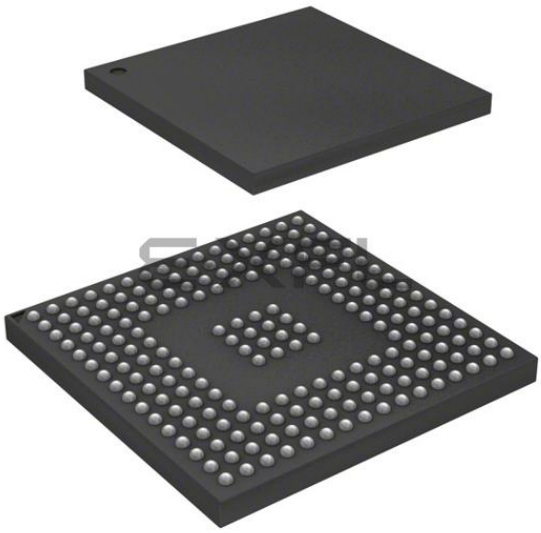

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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
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Oscillator Type	Internal
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3 Pin Assignments

3.1 208-ball MAPBGA Pin Assignments

Figure 3 shows the 208-ball MAPBGA pin assignments.

Figure 3. MPC5668x 208-ball MAPBGA (full diagram)

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PF8	PF[8] SCK_C	88	00 01 10 11	Port F GPIO DSPI_C Serial Clock — —	I/O I/O — —	V_{DDE2}	MH	—	—	P1	P1
PF9	PF[9] SOUT_C	89	00 01 10 11	Port F GPIO DSPI_C Serial Data Out — —	I/O O — —	V_{DDE2}	MH	—	—	T2	T2
PF10	PF[10] SIN_C	90	00 01 10 11	Port F GPIO DSPI_C Serial Data In — —	I/O I — —	V_{DDE2}	SH	—	—	R1	R1
PF11	PF[11] PCS_C[0] PCS_D[5] PCS_A[4]	91	00 01 10 11	Port F GPIO DSPI_C Peripheral Chip Select DSPI_D Peripheral Chip Select DSPI_A Peripheral Chip Select	I/O I/O O O	V_{DDE2}	SH	—	—	R3	R3
PF12	PF[12] SCK_D	92	00 01 10 11	Port F GPIO DSPI_D Serial Clock — —	I/O I/O — —	V_{DDE3}	MH	—	—	N14	N14
PF13	PF[13] SOUT_D	93	00 01 10 11	Port F GPIO DSPI_D Serial Data Out — —	I/O O — —	V_{DDE3}	MH	—	—	M14	M14
PF14	PF[14] SIN_D	94	00 01 10 11	Port F GPIO DSPI_D Serial Data In — —	I/O I — —	V_{DDE3}	SH	—	—	P14	P14
PF15	PF[15] PCS_D[0] PCS_A[5] PCS_B[4]	95	00 01 10 11	Port F GPIO DSPI_D Peripheral Chip Select DSPI_A Peripheral Chip Select DSPI_B Peripheral Chip Select	I/O I/O O O	V_{DDE3}	SH	—	—	P13	P13
Port G (16)											
PG0	PG[0] PCS_A[4] PCS_B[3] AN[48]	96	00 01 10 11	Port G GPIO DSPI_A Peripheral Chip Select DSPI_B Peripheral Chip Select ADC Analog Input	I/O O O I	V_{DDE2}	SHA	—	—	B3	B3
PG1	PG[1] PCS_A[5] PCS_B[4] AN[49]	97	00 01 10 11	Port G GPIO DSPI_A Peripheral Chip Select DSPI_B Peripheral Chip Select ADC Analog Input	I/O O O I	V_{DDE2}	SHA	—	—	A3	A3

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PG2	PG[2] PCS_D[1] SCL_C AN[50]	98	00 01 10 11	Port G GPIO DSPI_D Peripheral Chip Select I^2C_C Serial Clock ADC Analog Input	I/O O I/O I	V_{DDE3}	SHA	—	—	H14	H14
PG3	PG[3] PCS_D[2] SDA_C AN[51]	99	00 01 10 11	Port G GPIO DSPI_D Peripheral Chip Select I^2C_C Serial Data ADC Analog Input	I/O O I/O I	V_{DDE3}	SHA	—	—	J14	J14
PG4	PG[4] PCS_D[3] SCL_B AN[52]	100	00 01 10 11	Port G GPIO DSPI_D Peripheral Chip Select I^2C_B Serial Clock ADC Analog Input	I/O O I/O I	V_{DDE3}	SHA	—	—	K14	K14
PG5	PG[5] PCS_D[4] SDA_B AN[53]	101	00 01 10 11	Port G GPIO DSPI_D Peripheral Chip Select I^2C_B Serial Data ADC Analog Input	I/O O I/O I	V_{DDE3}	SHA	—	—	L14	L14
PG6	PG[6] PCS_C[1] FEC_MDC AN[54]	102	00 01 10 11	Port G GPIO DSPI_C Peripheral Chip Select Ethernet Mgmt. Data Clock ADC Analog Input	I/O O O I	V_{DDE3}	MHA	—	—	H15	H15
PG7	PG[7] PCS_C[2] FEC_MDIO AN[55]	103	00 01 10 11	Port G GPIO DSPI_C Peripheral Chip Select Ethernet Mgmt. Data I/O ADC Analog Input	I/O O I/O I	V_{DDE3}	MHA	—	—	J15	J15
PG8	PG[8] eMIOS[7] FEC_TX_CLK AN[56]	104	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Clock ADC Analog Input	I/O I/O I I	V_{DDE3}	SHA	—	—	K15	K15
PG9	PG[9] eMIOS[6] FEC_CRS AN[57]	105	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Carrier Sense ADC Analog Input	I/O I/O I I	V_{DDE3}	SHA	—	—	L15	L15
PG10	PG[10] eMIOS[5] FEC_TX_ER AN[58]	106	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Error ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	M15	M15
PG11	PG[11] eMIOS[4] FEC_RX_CLK AN[59]	107	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Receive Clock ADC Analog Input	I/O I/O I I	V_{DDE3}	SHA	—	—	J16	J16
PG12	PG[12] eMIOS[3] FEC_TXD[0] AN[60]	108	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	K16	K16

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PJ1	PJ[1] eMIOS[14] PCS_A[5]	129	00 01 10 11	Port J GPIO eMIOS Channel DSPI_A Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T7	T7
PJ2	PJ[2] eMIOS[13] PCS_B[1]	130	00 01 10 11	Port J GPIO eMIOS Channel DSPI_B Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	R8	R8
PJ3	PJ[3] eMIOS[12] PCS_B[2]	131	00 01 10 11	Port J GPIO eMIOS Channel DSPI_B Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T8	T8
PJ4	PJ[4] eMIOS[11] PCS_C[3]	132	00 01 10 11	Port J GPIO eMIOS Channel DSPI_C Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	R9	R9
PJ5	PJ[5] eMIOS[10] PCS_C[4]	133	00 01 10 11	Port J GPIO eMIOS Channel DSPI_C Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T9	T9
PJ6	PJ[6] eMIOS[09] PCS_D[5]	134	00 01 10 11	Port J GPIO eMIOS Channel DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	R10	R10
PJ7	PJ[7] eMIOS[08] PCS_D[1]	135	00 01 10 11	Port J GPIO eMIOS Channel DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T10	T10
PJ8	PJ[8] eMIOS[07]	136	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	T11	T11
PJ9	PJ[9] eMIOS[06]	137	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	R11	R11
PJ10	PJ[10] eMIOS[05]	138	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	N12	N12
PJ11	PJ[11] eMIOS[04]	139	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	P12	P12

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PJ12	PJ[12] eMIOS[03]	140	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	R12	R12
PJ13	PJ[13] eMIOS[02]	141	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	T12	T12
PJ14	PJ[14] eMIOS[01]	142	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	R13	R13
PJ15	PJ[15] eMIOS[00]	143	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	T13	T13
Port K (11)											
PK0	PK[0] MLBCLK SCK_B CLKOUT	144	00 01 10 11	Port K GPIO Media Local Bus Clock DSPI_B Serial Clock CLKOUT (Test Only)	I/O I I/O O	V_{DDEMLB}	F	—	—	L1	L1
PK1	PK[1] MLBSIG SOUT_B PCS_D[4]	145	00 01 10 11	Port K GPIO Media Local Bus Signal DSPI_B Serial Data Out DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDEMLB}	F	—	—	K1	K1
PK2	PK[2] MLBDAT SIN_B PCS_D[5]	146	00 01 10 11	Port K GPIO Media Local Bus Data DSPI_B Serial Data In DSPI_D Peripheral Chip Select	I/O I/O I O	V_{DDEMLB}	F	—	—	K2	K2
PK3	PK[3] FR_A_RX MA[0] PCS_C[1]	147	00 01 10 11	Port K GPIO FlexRay A Receive Data ADC Ext. Mux Address Select DSPI_C Peripheral Chip Select	I/O I O O	V_{DDE2}	SH	—	—	T3	T3
PK4	PK[4] FR_A_TX MA[1] PCS_C[2]	148	00 01 10 11	Port K GPIO FlexRay A Transmit Data ADC Ext. Mux Address Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	R4	R4
PK5	PK[5] FR_A_TX_EN MA[2] PCS_C[3]	149	00 01 10 11	Port K GPIO FlexRay A Transmit Enable ADC Ext. Mux Address Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	T4	T4

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
MDO11	MDO[11]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	M7
Miscellaneous Pins (9)											
EXTAL	EXTAL EXTCLK	—	—	Main Crystal Oscillator Input External Clock Input	I I	V_{DDSYN}	A	EXTAL		A14	A14
XTAL	XTAL	—	—	Main Crystal Oscillator Output	O	V_{DDSYN}	A	XTAL		A13	A13
TDI	TDI	—	—	JTAG Test Data Input	I	V_{DDE2}	SH	TDI (Pull Up)		J3	J3
TDO	TDO	—	—	JTAG Test Data Output	O	V_{DDE2}	MH	TDO (Pull Up[8])		M3	M3
TMS	TMS	—	—	JTAG Test Mode Select Input	I	V_{DDE2}	MH	TMS (Pull Up)		L3	L3
TCK	TCK	—	—	JTAG Test Clock Input	I	V_{DDE2}	SH	TCK (Pull Down)		P3	P3
JCOMP	JCOMP	—	—	JTAG Compliancy	I	V_{DDE2}	SH	JCOMP (Pull Down)		K3	K3
TEST	TEST	—	—	Test Mode Select	I	V_{DDE3}	IH	TEST[9]		M13	M13
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	—	—	External Reset	I/O	V_{DDE1}	MH	$\overline{\text{RESET}}$ (Pull Up)		A11	A11

1 The primary signal name is used as the pin label on the BGA map for identification purposes.

2 Each line in the Signal Name column corresponds to a separate signal function on the pin. For all device I/O pins, the primary, alternate, or GPIO signal functions are designated in the PA field of the System Integration Unit (SIU) PCR registers except where explicitly noted.

3 The GPIO number is the same as the corresponding pad configuration register (SIU_PCR*n*) number.

4 The PA bitfield in the SIU_PCR*n* register selects the signal function for the pin. A dash in the Description field of this table indicates that this value for PC is reserved on this pin, and should not be used.

5 The pad type is indicated by one or more of the following abbreviations: A–analog, F—fast speed, H–high voltage, I—input-only, M–medium speed, S–slow speed. For example, pad type SH designates a slow high-voltage pad.

6 The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. The terminology used in this column is: O – output, I – input, Up – weak pull up enabled, Down – weak pulldown enabled, Low – output driven low, High – output driven high. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin. The signal name to the left or right of the slash indicates the pin is enabled.

7 The Function After Reset of a GPI function is general purpose input. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin.

8 Pullup is enabled only when JCOMP is negated.

9 Tie to V_{SS} for normal operation.

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for either hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 4}$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

Table 8. DC Electrical Specifications

Spec	Characteristic	Symbol	Min	Max	Unit
6	3.3–5.0 V External I/O Supply Voltage[2] V_{DDE1} V_{DDE2} V_{DDE3} V_{DDE4}		 3.0 3.0 3.0 3.0	 5.5 5.5 5.5 5.5	V
7	2.5 V – 3.3 V External I/O Supply Voltage (MLB)	V_{DDEMLB}[3]	2.375	3.6	V
8	3.3 V External I/O Supply Voltage (Nexus)	V_{DDENEX}	3.0	3.6	V
9	Pad Input High Voltage Hysteresis enabled Hysteresis disabled (IHA/SH/SHA/MH/MHA)[4, 5] Hysteresis disabled (F)	V_{IH}	 0.65 × V_{DDE} 0.55 × V_{DDE} 0.55 × V_{DDE}	V_{DDE} + 0.3	V
10	Pad Input Low Voltage Hysteresis enabled Hysteresis disabled (IHA/SH/SHA/MH/MHA)[4, 5] Hysteresis disabled (F)	V_{IL}	V_{SS} – 0.3	 0.35 × V_{DDE} 0.40 × V_{DDE} 0.40 × V_{DDE}	V
11	Pad Input Hysteresis	V_{HYS}	0.1 × V_{DDE}		V
12	Analog (IHA) Input Voltage	V_{INDC}	V_{SSA} – 0.3	V_{DDA} + 0.3	V
13	Pad Output High Voltage[6, 7, 8]	V_{OH}	0.8 × V_{DDE}	—	V
14	Pad Output Low Voltage[8]	V_{OL}	—	0.2 × V_{DDE}	V
15	Input Capacitance (Digital Pins: Pad type F, MH, SH)[4]	C_{IN}	—	7	pF
16	Input Capacitance (Analog Pins: Pad type IHA)[4, 5]	C_{IN_A}	—	10	pF
17	Input Capacitance (Shared digital/analog pins: MHA, SHA)[4]	C_{IN_M}	—	12	pF
18	I/O Weak Pull Up/Down Absolute Current[4, 9] Pad F: 2.375 V – 3.6 V Pad SH/MH/IHA: 3.0 V – 3.6 V Pad SH/MH/IHA: 4.5 V – 5.5 V	I_{ACT}	 25 10 35	 180 95 200	µA
19	I/O Input Leakage Current[10]	I_{INACT_D}	–2.5	2.5	µA
20	DC Injection Current (per pin)	I_{IC}	–1.0	1.0	mA
21	Analog Input Current, Channel Off[11] (Analog pins IHA)[4, 5]	I_{INACT_A}	–150	150	nA
22	Analog Reference High Voltage	V_{RH}	V_{DDA} – 500	V_{DDA}	mV
23	Analog Reference Low Voltage	V_{RL}	V_{SSA}	V_{SSA} + 500	mV
24	V_{SS} to V_{SSA} Differential Voltage	$V_{SS} – V_{SSA}$	–100	100	mV
25	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} – V_{SS}$	–100	100	mV
26	Slew rate on V_{DDA}, V_{DDEx}, V_{DDSYN}, V_{DD33}, and V_{RC} power supply pins	V_{Ramp}	—	100	V/ms
27	Capacitive Supply Load (V_{DD})	V_{Load}	8	—	µF
28	Capacitive Supply Load (V_{DD33}, V_{DDSYN})	V_{Load}	1	—	µF

1 When V_{RCSEL} = V_{SSA} (low), V_{DDSYN} and V_{DD33} are externally supplied. When V_{RCSEL} = V_{DDA} (high), V_{DDSYN} and V_{DD33} are generated by internal voltage regulators. When V_{RCSEL} = V_{SSA} (low), V_{DDSYN} and V_{DD33} cannot be 100 mV higher than V_{RC}.

Table 9. Operating Currents (continued)

Spec	Characteristic	Symbol	Typ[1] 25 °C Ambient	Max[1] –40–150 °C Junction	Unit
5	V_{DDSYN} Current V_{DD33} @ 3.0 V – 3.6 V Run mode Sleep mode – Optional[4] 4–40 MHz osc enabled w/ no clock – Optional[4] 4–40 MHz osc enabled w/ clock	I_{DDSYN}	 5 1 +150 +300	 10 20 +350 +400	 mA µA µA µA
6	V_{RC} Current (excluding I_{DD}, I_{DD33}, I_{DDSYN})[5] V_{RC} @ 3.135 V – 5.5 V Run mode Sleep mode – Optional[4] 16MIRC enabled	I_{RC}	 1 0 +40	 10 10 +60	 mA µA µA
7	V_{DD} Current V_{DD} @ 1.08 V – 1.32 V Run mode (Maximum @ 116 MHz)[6] Sleep mode – Optional[4] 128KIRC enabled – Optional[4] 16MIRC enabled – Optional[4] 32 kHz osc enabled – Optional[4] 4–40 MHz osc enabled w/ no clock – Optional[4] 4–40 MHz osc enabled w/ clock – Optional[4] 32 KB RAM – Optional[4] 64 KB RAM – Optional[4] 128 KB RAM	I_{DD}	 200 100 +5 +200 +5 +5 +150 +10 +20 +40	 340 900 +10 +220 +20 +20 +200 +150 +300 +600	 mA µA µA µA µA µA µA µA µA µA

1 Typ – Nominal voltage levels and functional activity. Max – Maximum voltage levels and functional activity.

2 Static state of pins is when input pins are disabled or not being toggled and driven to a valid input level, output pins are not toggling or driving against any current loads, and internal pull devices are disabled or not pulling against any current loads.

3 Dynamic current from pins is application-specific and depends on active pull devices, switching outputs, output capacitive and current loads, and switching inputs. Refer to Table 10 for more information.

4 Optional currents are values that should be added to their respective current specifications to obtain the actual value for that specification when the optional function is active. The plus sign (+) in the Typ and Max columns indicates these optional currents. For example, V_{DDSYN} in Sleep mode draws 1 .µA (typ). With the optional 4–40 MHz osc enabled w/ no clock, add 150 .µA for a total of 151 .µA (typ).

5 V_{RC} Current excluding the current supply to V_{DD33}, V_{DDSYN} and V_{DD} from V_{RC}.

6 Maximum supply current transition: 50mA per 20µS observation window.

4.7 I/O Pad Current Specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 10 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 10.

Table 10. I/O Pad Average I_{DDE} Specifications[1]

Spec	Pad Type[2]	Symbol	Period (ns)	Load[3] (pF)	V_{DDE} (V)	Drive/Slew Rate Select	I_{DDE} Avg (mA)	I_{DDE} RMS (mA)
1	Slow	$I_{DRV\_SSR\_HV}$	37	50	5.5	11	14	
2			130	50	5.5	01	5.3	
3			650	50	5.5	00	1.1	
4			840	200	5.5	00	3	
6	Medium	$I_{DRV\_MSR\_HV}$	24	50	5.5	11	9	
7			62	50	5.5	01	2.5	
8			317	50	5.5	00	0.5	
9			425	200	5.5	00	1.5	
11	Fast	I_{DRV_FC}	10	50	3.6	11	50.4	101.6
12			10	30	3.6	10	14.2	57.3
13			10	20	3.6	01	16.4	43.6
14			10	10	3.6	00	9.8	15.9
15			10	50	2.75	11	22.9	45.3
16			10	30	2.75	10	6.7	25.3
17			10	20	2.75	01	4.5	17.3
18			10	10	2.75	00	3	9.6
19	Input	$I_{DRV\_I\_HV}$	7	0.5	5.5	N/A	N/A	N/A

1 These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

2 Slow = SH or SHA; Medium = MH or MHA; Fast = F; Input = IHA. See Table 2.

3 All loads are lumped.

4.8 Low Voltage Characteristics

Table 13. Low Voltage Monitors

Spec	Characteristic	Symbol	Min	Typical	Max	Unit
1	Power-on-Reset Assert Level[1]	V_{POR}	1.5	—	2.8	V
2	Low Voltage Monitor 3.3 V[2] Assert Level De-assert Level	 V_{LVI33A} V_{LVI33D}	 3.00 3.04	 3.05 3.12	 3.10 3.19	V
3	Low Voltage Monitor Synthesizer[3] Assert Level De-assert Level	 $V_{LVISYNA}$ $V_{LVISYND}$	 3.00 3.04	 3.05 3.12	 3.10 3.19	V
4	Low Voltage Monitor 3.0 V Low Threshold[1] VRCSEL = V_{SSA} Assert Level De-assert Level VRCSEL = V_{DDA} Assert Level De-assert Level	 $V_{LVI\_VDDA\_LOA}$ $V_{LVI\_VDDA\_LOD}$ $V_{LVI\_VDDA\_LOA}$ $V_{LVI\_VDDA\_LOD}$	 3.00 3.04 3.25 3.35	 3.05 3.12 3.35 3.45	 3.10 3.19 3.48 3.55	V
5	Low Voltage Monitor 5.0 V[1, 4] Assert Level De-assert Level	 $V_{LVI\_VDDA\_A}$ $V_{LVI\_VDDA\_D}$	 4.35 4.45	 4.475 4.575	 4.55 4.65	V
6	Low Voltage Monitor 5.0 V High Threshold[1, 5] Assert Level De-assert Level	 $V_{LVI\_VDDA\_HA}$ $V_{LVI\_VDDA\_HD}$	 4.50 4.50	 4.675 4.675	 4.80 4.80	V

1 Monitors V_{DDA}.

2 Monitors V_{DD33}.

3 Monitors V_{DDSYN}.

4 Disabled when $V_{RCSEL} = V_{SSA}$.

4.9 Oscillators Electrical Characteristics

Table 14. 3.3 V High Frequency External Oscillator

Spec	Characteristic	Symbol	Min	Max	Unit
1	Frequency Range	f_{ref}	4[1]	40	MHz
2	Duty Cycle of reference	t_{DC}	40	60	%
3	EXTAL Input High Voltage External crystal mode[2] External clock mode	V_{IHEXT}	 V_{XTAL} + 0.4 0.65 × V_{DDSYN}	 V_{DDSYN} + 0.3 V_{DDSYN} + 0.3	V
4	EXTAL Input Low Voltage External crystal mode[3] External clock mode	V_{ILEXT}	 V_{DDSYN} – 0.3 V_{DDSYN} – 0.3	 V_{XTAL} – 0.4 0.35 × V_{DDSYN}	V
5	XTAL Current[4]	I_{XTAL}	1	3	mA
6	Total On-chip stray capacitance on XTAL	C_{S_XTAL}	—	3	pF
7	Total On-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	3	pF

Table 17. 5V Low Frequency (128 kHz) Internal RC Oscillator

Spec	Characteristic	Symbol	Range	Min	Typ	Max	Unit
1	Frequency before trim[1]	F_{ut128}	35%	83.2	128	172.8	kHz
2	Frequency after loading factory trim[2]	F_{t128}	7%	119.0	128	137.0	kHz
3	Application trim resolution[3]	T_{s128}	—	—	—	±2	%
4	Application frequency trim step[3]	F_{s128}	—	—	4	—	kHz
5	Startup Time	S_{t128}	—	—	—	100	µs

1 Across process, voltage, and temperature.

2 Across voltage and temperature.

3 Fixed voltage and temperature.

4.10 FMPLL Electrical Characteristics

Table 18. FMPLL Electrical Specifications[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	System Frequency[2]	f_{SYS}	—	116	MHz
2	PLL Reference Frequency Range	f_{REF}	4	40	MHz
3	PLL Frequency	f_{PLL}	$\frac{f_{vco(min)}}{(ERFD+1)}$		MHz
4	Loss of Reference Frequency [3]	f_{LOR}	100	2000	kHz
5	Self Clocked Mode Frequency	f_{SCM}	16	64	MHz
6	PLL Lock Time[4]	t_{LPLL}	—	400	µs
7	Duty Cycle of Reference	t_{DC}	40	60	%
8	Frequency un-LOCK Range	f_{UL}	–4.0	4.0	% f_{SYS}
9	Frequency LOCK Range	f_{LCK}	–2.0	2.0	% f_{SYS}
10	CLKOUT Period Jitter,[5] Measured at f_{SYS} Max Cycle-to-cycle Jitter	C_{Jitter}	–5	5	%f_{SYS}
11	CLKOUT Jitter at ≥ 50 µs period	C_{Jitter}	–250	250	ns
12	Peak-to-Peak Frequency Modulation Range Limit [6,7] (f_{SYS}Max must not be exceeded)	C_{mod}	0	4	%f_{SYS}
13	FM Depth Tolerance[8]	C_{mod_err}	–0.50	0.50	%f_{SYS}
14	VCO Frequency[9]	f_{VCO}	192	600	MHz
15	Modulation Rate Limits[10]	f_{MOD}	0.400	1	MHz

1 V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H.

2 The maximum frequency value is with frequency modulation disabled. If frequency modulation is enabled, the maximum frequency value should be de-rated by the percentage of modulation enabled so that the maximum frequency is not exceeded.

3 "Loss of Reference Frequency" is the reference frequency detected internally, which transitions the PLL into self clocked mode.

4 This specification applies to the period required for the PLL to re-lock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, lock time will be additive with crystal startup time.

5 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{jitter} + C_{mod}.

6 Modulation depth selected must not result in f_{PLL} value greater than the f_{PLL} maximum specified value.

7 Maximum and minimum variations from programmed modulation depth are 2%, 3%, and 4% peak-to-peak. Use only these settings.

8 Depth tolerance is the programmed modulation depth ±0.25% of f_{SYS}.

9 See the Block Guide for VCO frequency synthesis equations.

10 Modulation rates less than 400 kHz will result in exceedingly long FM calibration durations. Modulation rates greater than 1 MHz will result in reduced calibration accuracy.

4.11 ADC Electrical Characteristics

Table 19. ADC Conversion Specifications (Operating)

Spec	Characteristic	Symbol	Min	Max	Unit
1	Analog High Reference Voltage	V_{RH}	V_{DDA} – 0.5	V_{DDA}	V
2	Analog Low Reference Voltage	V_{RL}	0	0.5	V
3	Analog Input Voltage	AV_{IN}	V_{RL}	V_{RH}	V
4	Sampling Frequency	F_S	—	1.53	MHz
5	Maximum ADC Clock Frequency	F_{MAX}	—	60	MHz
6	Sampling Time V_{DDA} = 3.0 V – 3.6 V V_{DDA} > 3.6 V – 5.5 V	t_S	 250 125	—	ns
7	Differential Non Linearity	DNL	–1.0	1.0	LSB
8	Integral Non Linearity	INL	–1.5	1.5	LSB
9	Offset Error	OFS	–1.0	1.0	LSB
10	Gain Error	GNE	–2.0	2.0	LSB
11	Total Unadjusted Error [1]	TUE	–2.0	2.0	LSB

1 TUE assumes no pin activity on pins adjacent to analog channel or output driver activity on corresponding V_{DDE} segment.

4.12 Flash Memory Electrical Characteristics

Table 20. Flash Program and Erase Specifications[1]

Spec	Characteristic	Symbol	Min	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time[4]	$t_{dwprogram}$	—	—	500	µs
2	Page (128 bits and 256 bits) Program Time[4]	$t_{pprogram}$	—	160	500	µs
3	16 KB Block Pre-program and Erase Time	$t_{16kpperase}$	—	1000	5000	ms
4	64 KB Block Pre-program and Erase Time	$t_{64kpperase}$	—	1800	5000	ms
5	128 KB Block Pre-program and Erase Time	$t_{128kpperase}$	—	2600	7500	ms

Table 22. Pad AC Specifications (5.0 V, 2.5 V)[1] (continued)

Spec	Pad Type[2]	SRC/DSC[3]	Output Delay[4,4] (ns)	Rise/Fall[5,6] (ns)	Load Drive (pF)
2	Medium	00	142/186	65/89	50
			195/253	91/122	200
		01	20/35	8.7/16.6	50
			41/64	24/35	200
		11	12/11	5.3/5.9	50
			32/34	21/23	200
3	Fast[8]	00	2.7	1.5	10
		01			20
		10			30
		11			50
4	Input	N/A	1.9/1.9	1.5/1.5	0.5

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at F_{SYS} = 116 MHz, V_{DD} = 1.08 – 1.32 V, V_{DDE} = 1.62 – 1.98 V, V_{DDEH} = 4.5 – 5.5 V, V_{RC33} and V_{DDPLL} = 3.0 – 3.6 V, $T_A = T_L$ to T_H.

2 Slow = SH or SHA; Medium = MH or MHA; Fast = F; Input = IHA. See Table 2.

3 SRC/DSC are bit fields in the Pad Configuration Registers. SRC—Slew Rate Control (slow and medium pad types only), DSC—Drive Strength Control (fast pad type only).

4 This parameter is supplied for reference and is not guaranteed by design and not tested.

5 This parameter is guaranteed by characterization before qualification rather than 100% tested.

6 Delay and rise/fall are measured to 20% or 80% of the respective signal.

7 Add a maximum of one system clock to the output delay for delay with respect to system clock.

8 Output delay is shown in. Add a maximum of one system clock to the output delay for delay with respect to system clock.

Table 23. De-rated Pad AC Specifications (3.3 V, 3.3 V)[1]

Spec	Pad Type[2]	SRC/DSC[3]	Out Delay[4,5] (ns)	Rise/Fall[6,] (ns)	Load Drive (pF)
1	Slow[7]	00	408/431	188/204	50
			533/592	250/288	200
		01	80/90	38/44	50
			146/167	82/96	200
		11	27/28	15/17	50
			81/92	57/67	200
2	Medium	00	184/240	79/107	50
			253/330	114/153	200
		01	28/47	11.8/21.8	50
			58/88	34/49	200
		11	18/17	7.6/8.9	50
			46/51	30/35	200

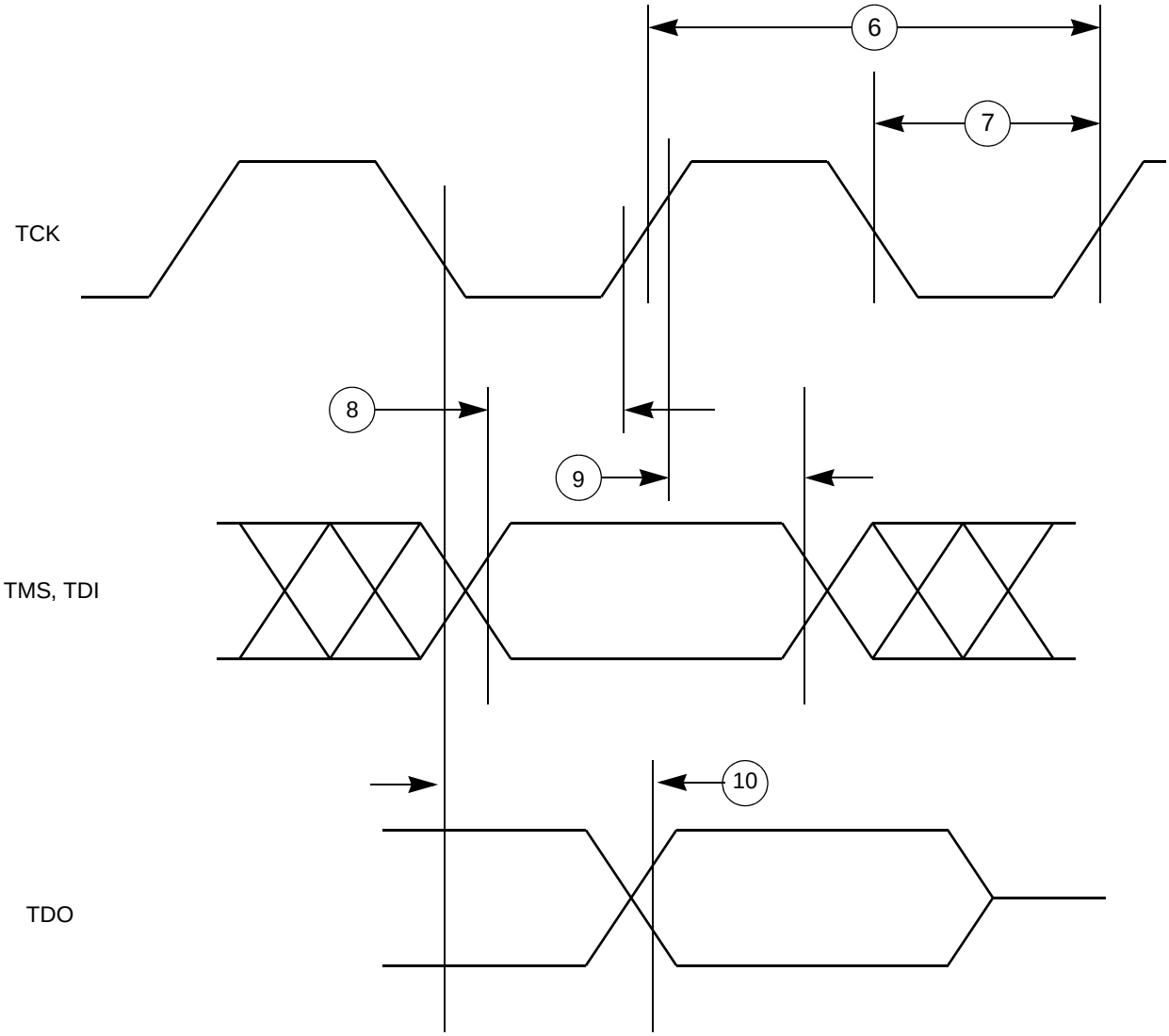

Figure 14. Nexus TDI, TMS, TDO Timing

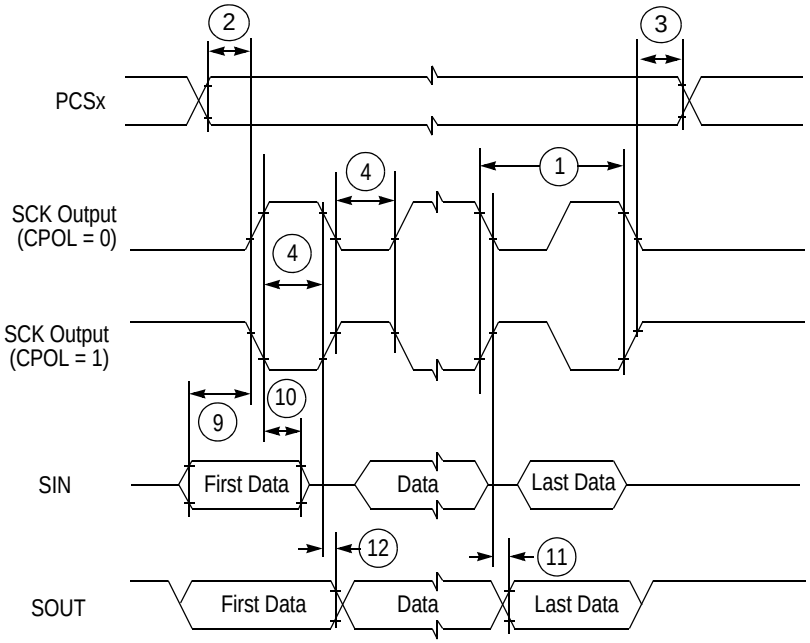

Figure 16. DSPI Classic SPI Timing — Master, CPHA = 0

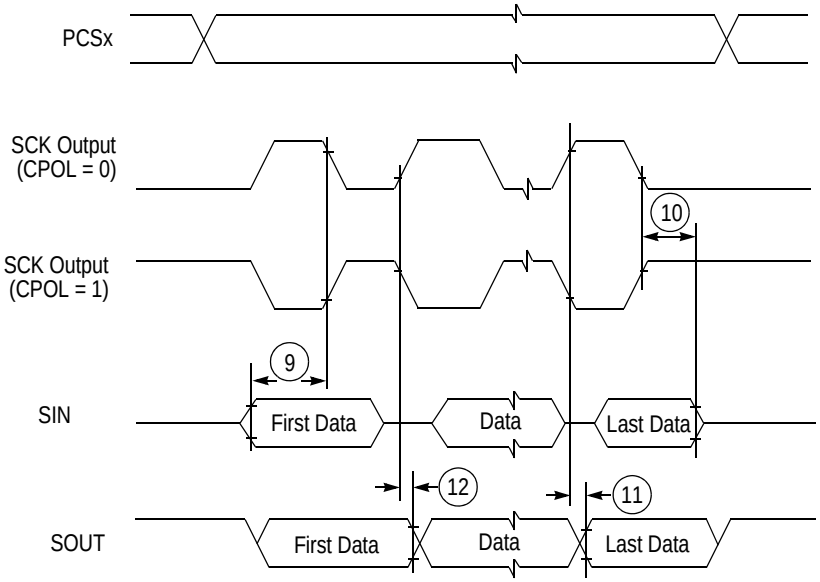

Figure 17. DSPI Classic SPI Timing — Master, CPHA = 1

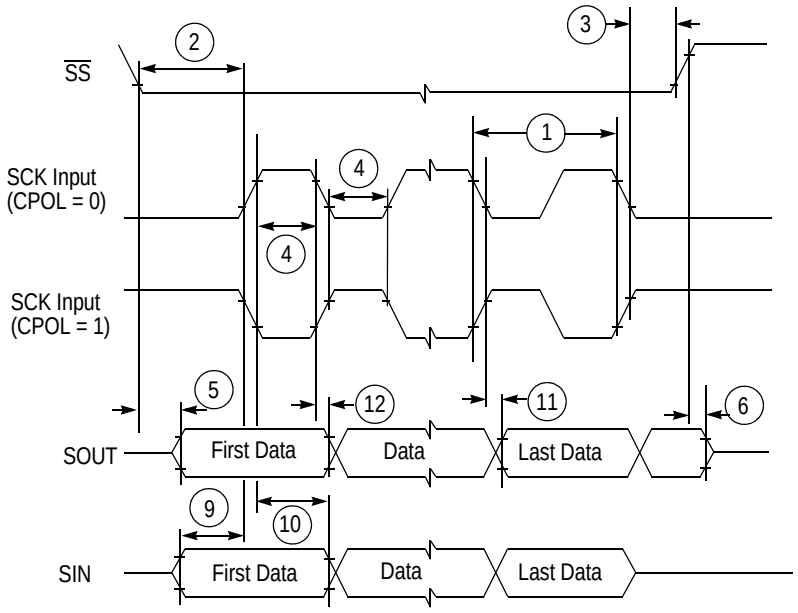

Figure 18. DSPI Classic SPI Timing — Slave, CPHA = 0

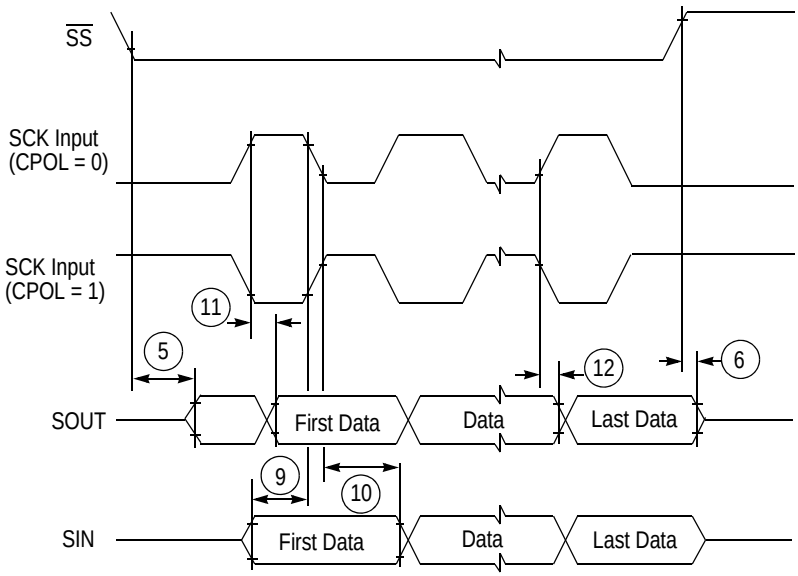

Figure 19. DSPI Classic SPI Timing — Slave, CPHA = 1

Table 31. MLB Timing for MLB Speed 256 Fs or 512 Fs (continued)

Spec	Parameter	Symbol	Min	Typ	Max	Unit	Comments
10	MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	—	t_{mckl}	ns	
11	Bus Hold time[3]	t_{mdzh}	4	—	—	ns	
12	MLBSIG/MLBDAT output valid from MLBCLK rising	t_{mcrdv}	—	—	8	ns	

- Ground = 0.0V
- Load Capacitance = 60 pF, SIU_PCR144–SIU_PCR146[DSC] = 0b11.
- MLB speed of 256 Fs or 512 Fs (Fs = 48 kHz)
  Unless otherwise noted, all timing parameters are specified from the valid voltage threshold in Table 30.

1 The Controller can shut off MLBCLK to place MLB in a low-power state.

2 Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (ns p-p).

3 The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

Table 32. MLB Timing for MLB Speed 1024 Fs

Spec	Parameter	Symbol	Min	Typ	Max	Unit	Comments
1	MLBCLK Operating Frequency[1]	f_{mck}	45.056 — — —	— 49.152 — —	— — 49.2544 51.200	MHz	1024 Fs at 44.0 kHz 1024 Fs at 48.0 kHz 1024 Fs at 48.1 kHz 1024 Fs PLL unlocked
2	MLBCLK rise time	t_{mckr}	—	—	1	ns	V_{IL} to V_{IH}
3	MLBCLK fall time	t_{mckf}	—	—	1	ns	V_{IH} to V_{IL}
4	MLBCLK cycle time	t_{mckc}	—	20.3	—	ns	V_{IL} to V_{IH}
5	MLBCLK low time	t_{mckl}	6.5 6.1	7.7 7.3	—	ns	1024 Fs PLL unlocked
6	MLBCLK high time	t_{mckh}	9.7 9.3	10.6 10.2	—	ns	1024 Fs PLL unclocked
7	MLBCLK pulse width variation[2]	t_{mpwv}	—	—	0.7	ns p-p	
8	MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	1	—	—	ns	
9	MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	0	—	—	ns	
10	MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	—	t_{mckl}	ns	
11	Bus Hold time[3]	t_{mdzh}	2	—	—	ns	
12	MLBSIG/MLBDAT output valid from MLBCLK rising	t_{mcrdv}	—	—	7	ns	

- Ground = 0.0V
- Load Capacitance = 40 pF, SIU_PCR144–SIU_PCR146[DSC] = 0b00.
- MLB speed = 1024Fs (Fs = 48 kHz)
- Unless otherwise noted, timing parameters are specified from the valid voltage threshold in Table 30.

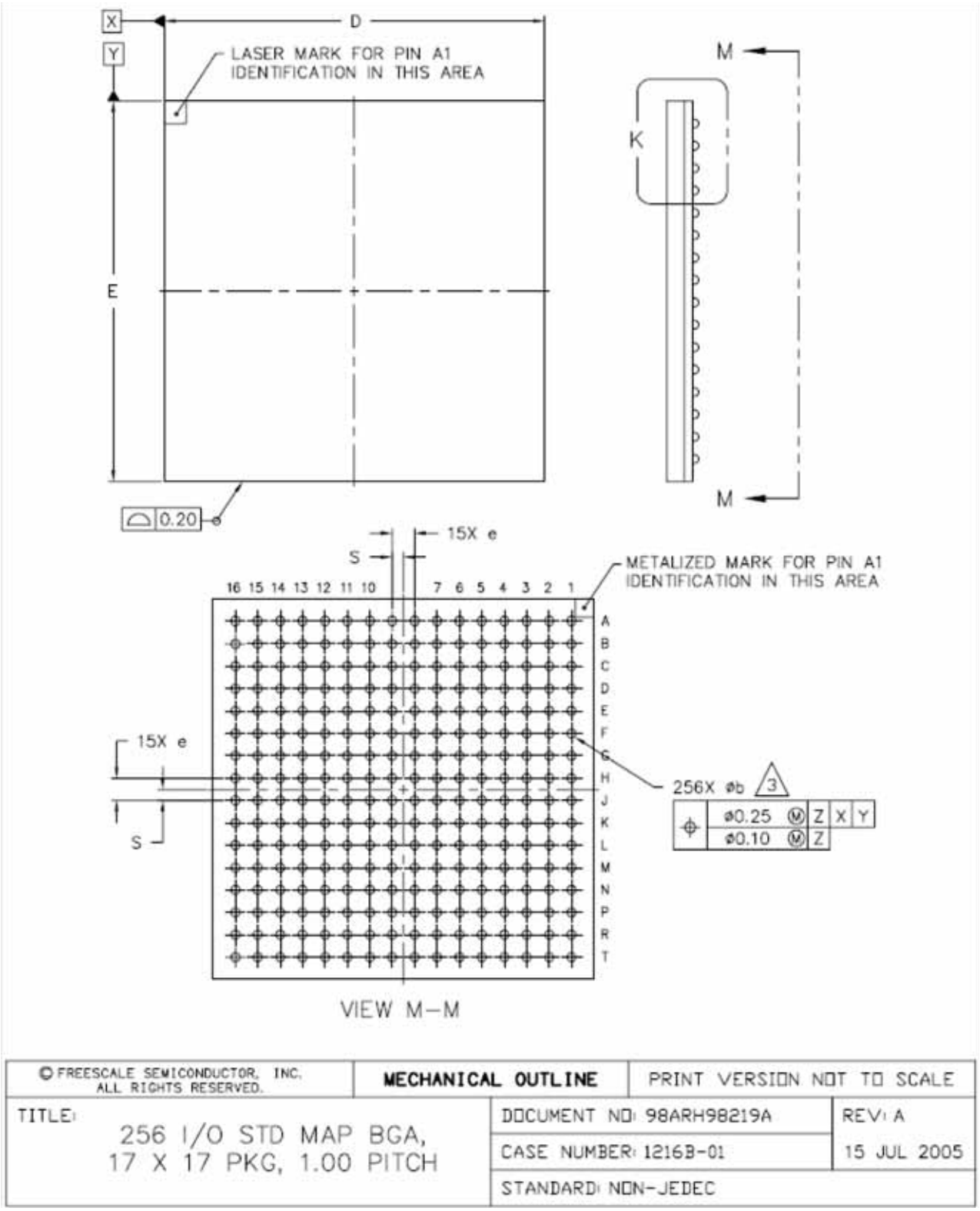

Figure 32. 256 MAPBGA Package Mechanical Drawing

6 Revision History

Table 37 describes the changes made to this document between revisions.

Table 37. Revision History

Revision	Date	Description
0	April 2008	Preliminary release.
1	June 2008	Initial release: Advance Information.
2	Jan 2009	Release: Advance Information.
3	September 2009	Release: Advance Information, interim updates.
4	January 2011	Release: Technical Data, interim updates.
5	January 2011	Release: Technical Data, interim updates.
6	March 2011	Release: Technical Data, interim updates.