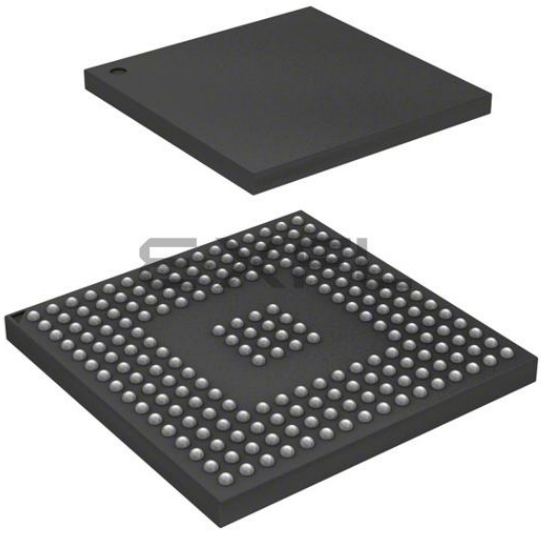

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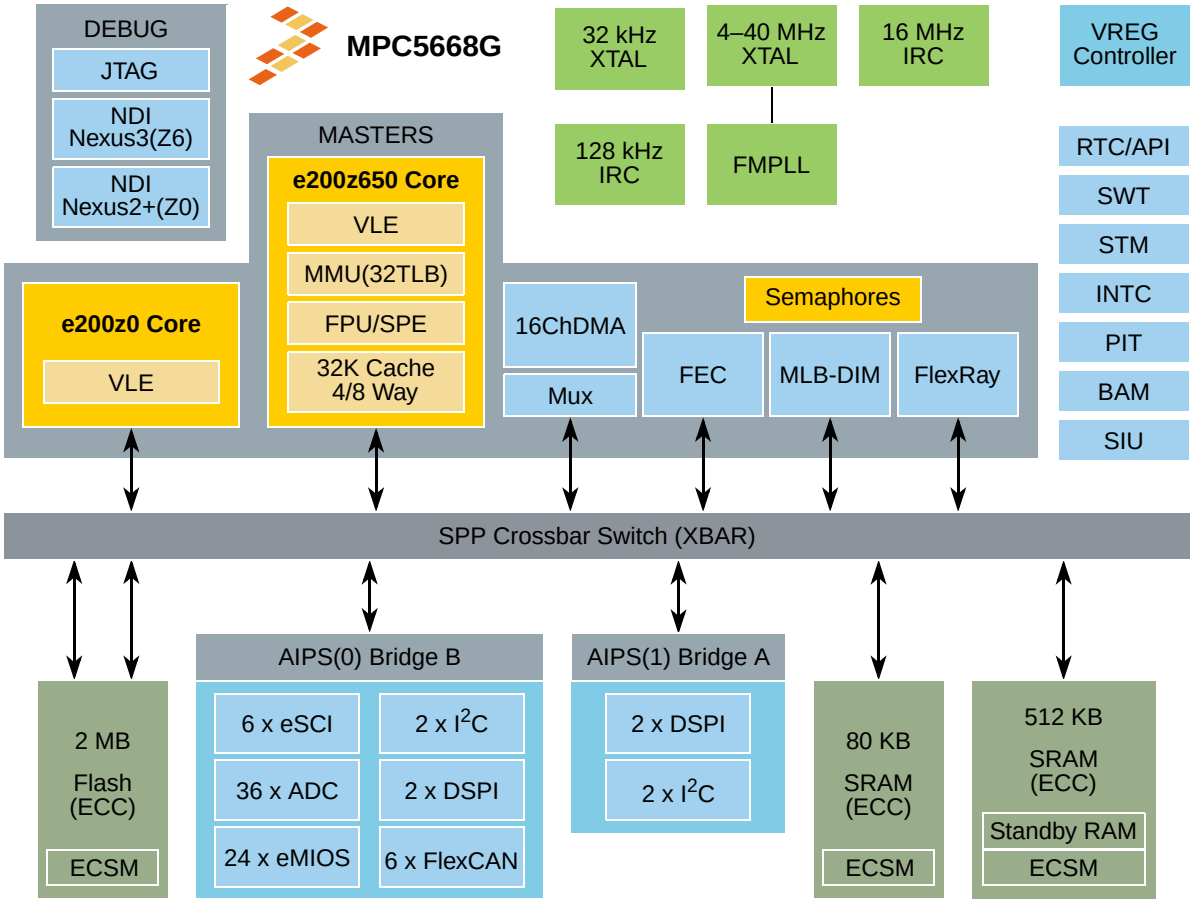
Details	
Product Status	Active
Core Processor	e200z650
Core Size	32-Bit Single-Core
Speed	116MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	155
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	592K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 36x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BGA
Supplier Device Package	208-BGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5668gf1ammg

2 MPC5668x Block Diagrams

Figure 1 shows a top-level block diagram of the MPC5668G device.

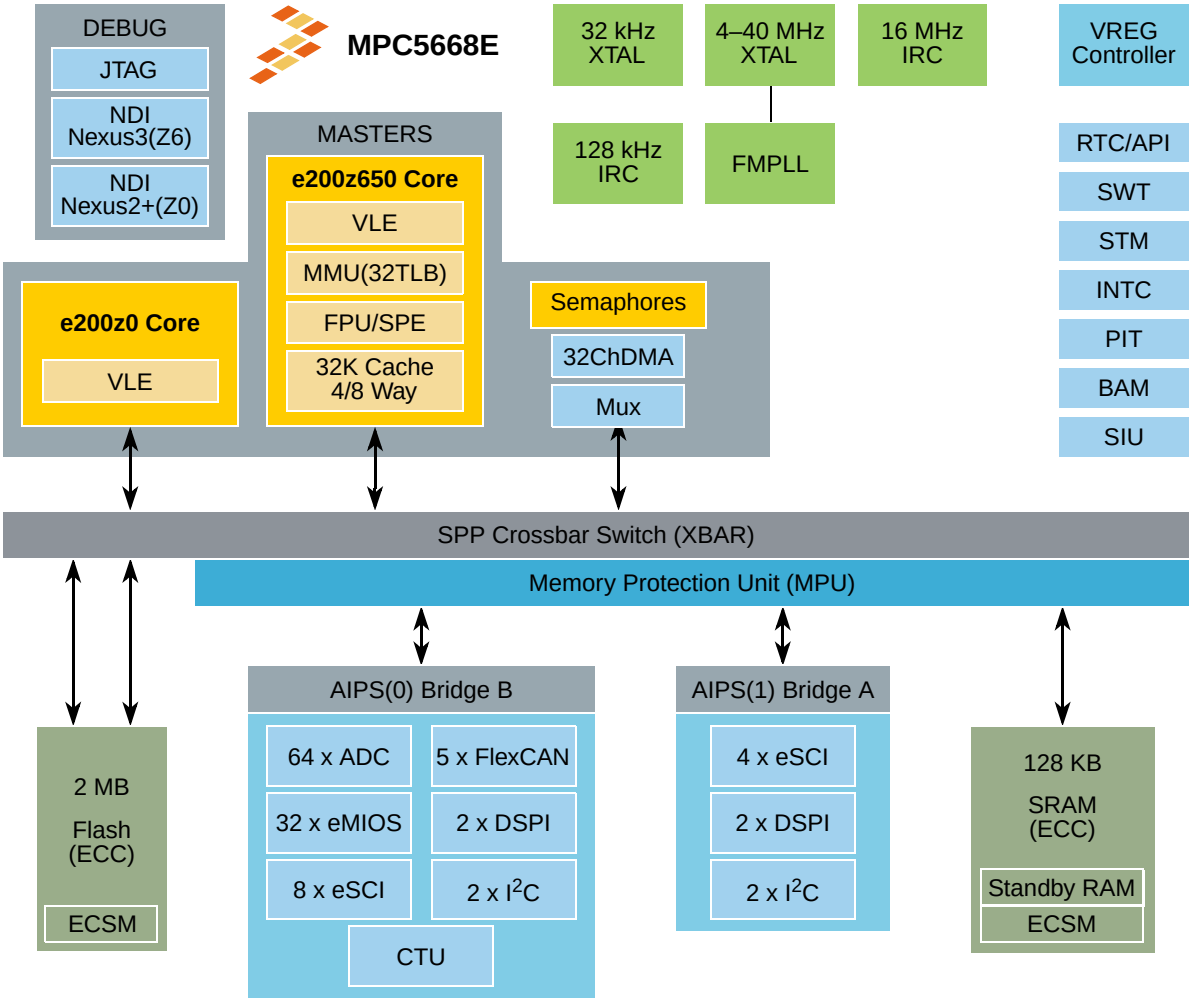


LEGEND

ADC	– Analog to Digital Converter	**I²C**	– Inter IC Controller
BAM	– Boot Assist Module	**INTC**	– Interrupt Controller
DSPI	– Serial Peripherals Interface	**JTAG**	– Joint Test Action Group interface
ECC	– Error Correction Code	**MLB-DIM**	– Media Local Bus Device Interface Module
ECSM	– Error Correction Status Module	**NDI**	– Nexus Debug Interface
eMIOS	– Timed Input Output	**PIT**	– Periodic Interrupt Timer
eDMA	– Enhanced Direct Memory Access controller	**RTC**	– Real Time Clock
eSCI	– Serial Communications Interface	**SIU**	– System Integration
FEC	– Fast Ethernet Controller	**STM**	– System Timer Module
FlexCAN	– Controller Area Network controller	**SWT**	– Software Watchdog Timer
FlexRay™	– FlexRay Bus Controller	**VREG**	– Voltage Regulator
FMPLL	– Frequency Modulated Phase Locked Loop		

Figure 1. MPC5668G Block Diagram

Figure 2 shows a top level block diagram for the MPC5668E device.



LEGEND

ADC	– Analog to Digital Converter	**I²C**	– Inter IC Controller
BAM	– Boot Assist Module	**INTC**	– Interrupt Controller
CTU	– Cross Triggering Unit	**JTAG**	– Joint Test Action Group interface
DSPI	– Serial Peripherals Interface controller	**MPU**	– Memory Protection Unit
ECC	– Error Correction Code	**NDI**	– Nexus Debug Interface
ECSM	– Error Correction Status Module	**PIT**	– Periodic Interrupt Timer
eDMA	– Enhanced Direct Memory Access controller	**RTC**	– Real Time Clock
eMIOS200	– Timed Input Output	**SIU**	– System Integration
eSCI	– Serial Communications Interface	**STM**	– System Timer Module
FlexCAN	– Controller Area Network controller	**SWT**	– Software Watchdog Timer
FMPLL	– Frequency Modulated Phase Locked Loop	**VREG**	– Voltage Regulator

Figure 2. MPC5668E Block Diagram

3.3 Pin Muxing and Reset States

Table 2 shows the signals properties for each pin on MPC5668x. For all port pins that have an associated SIU_PCR*n* register to control pin properties, the supported functions column lists the functions associated with the programming of the SIU_PCR*n*[PA] bit in the order: general-purpose input/output (GPIO), function 1, function 2, and function 3 (see Figure 5). When an alternate function is not implemented for a value of SIU_PCR*n*[PA], a dash is shown in the Description column and the respective value in the PA bit field is reserved.

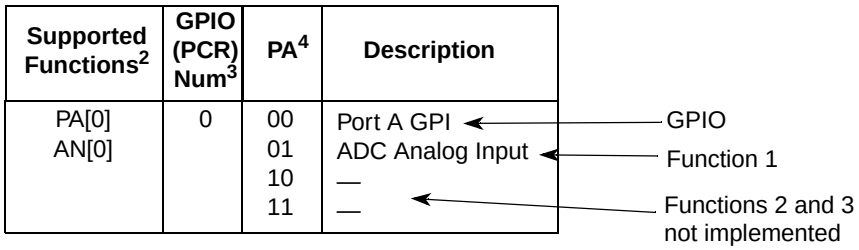


Figure 5. Supported Functions Example

Table 2. MPC5668x Signal Properties

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
Port A (16)											
PA0	PA[0] AN[0]	0	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	D15	D15
PA1	PA[1] AN[1]	1	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	E15	E15
PA2	PA[2] AN[2]	2	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	F16	F16
PA3	PA[3] AN[3]	3	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	F15	F15
PA4	PA[4] AN[4]	4	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	G16	G16
PA5	PA[5] AN[5]	5	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	G15	G15

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
Port B (16)											
PB0	PB[0] AN[16]/ANW	16	00 01 10 11	Port B GPIO ADC Analog Input/Mux In — —	I/O I — —	V_{DDE1}	SHA	—	—	B14	B14
PB1	PB[1] AN[17]/ANX	17	00 01 10 11	Port B GPIO ADC Analog Input/Mux In — —	I/O I — —	V_{DDE1}	SHA	—	—	C14	C14
PB2	PB[2] AN[18]/ANY	18	00 01 10 11	Port B GPIO ADC Analog Input/Mux In — —	I/O I — —	V_{DDE1}	SHA	—	—	B13	B13
PB3	PB[3] AN[19]/ANZ	19	00 01 10 11	Port B GPIO ADC Analog Input/Mux In — —	I/O I — —	V_{DDE1}	SHA	—	—	C13	C13
PB4	PB[4] AN[20]	20	00 01 10 11	Port B GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	C12	C12
PB5	PB[5] AN[21]	21	00 01 10 11	Port B GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	D12	D12
PB6	PB[6] AN[22]	22	00 01 10 11	Port B GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	C11	C11
PB7	PB[7] AN[23]	23	00 01 10 11	Port B GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	D11	D11
PB8	PB[8] AN[24] PCS_A[2]	24	00 01 10 11	Port B GPIO ADC Analog Input DSPI_A Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	A10	A10
PB9	PB[9] AN[25] PCS_A[3]	25	00 01 10 11	Port B GPIO ADC Analog Input DSPI_A Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	B12	B12

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PD9	PD[9] CNRX_E RXD_L SDA_C	57	00 01 10 11	Port D GPIO FlexCAN_E Receive SCI_L Receive I^2C_C Serial Data	I/O I I I/O	V_{DDE2}	SH	—	—	F1	F1
PD10	PD[10] CNTX_F TXD_M SCL_D	58	00 01 10 11	Port D GPIO FlexCAN_F Transmit SCI_M Transmit I^2C_D Serial Clock	I/O O O I/O	V_{DDE2}	SH	—	—	F2	F2
PD11	PD[11] CNRX_F RXD_M SDA_D	59	00 01 10 11	Port D GPIO FlexCAN_F Receive SCI_M Receive I^2C_D Serial Data	I/O I I I/O	V_{DDE2}	SH	—	—	G1	G1
PD12	PD[12] TXD_A	60	00 01 10 11	Port D GPIO eSCI_A Transmit — —	I/O O — —	V_{DDE2}	SH	—	—	G2	G2
PD13	PD[13] RXD_A	61	00 01 10 11	Port D GPIO eSCI_A Receive — —	I/O I — —	V_{DDE2}	SH	—	—	H1	H1
PD14	PD[14] TXD_B	62	00 01 10 11	Port D GPIO eSCI_B Transmit — —	I/O O — —	V_{DDE2}	SH	—	—	C3	C3
PD15	PD[15] RXD_B	63	00 01 10 11	Port D GPIO eSCI_B Receive — —	I/O I — —	V_{DDE2}	SH	—	—	D3	D3
Port E (16)											
PE0	PE[0] TXD_C eMIOS[31]	64	00 01 10 11	Port E GPIO eSCI_C Transmit eMIOS Channel —	I/O O I/O —	V_{DDE2}	SH	—	—	E3	E3
PE1	PE[1] RXD_C eMIOS[30]	65	00 01 10 11	Port E GPIO eSCI_C Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	E4	E4
PE2	PE[2] TXD_D eMIOS[29]	66	00 01 10 11	Port E GPIO eSCI_D Transmit eMIOS Channel —	I/O O I/O	V_{DDE2}	SH	—	—	F4	F4

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PE3	PE[3] RXD_D eMIOS[28]	67	00 01 10 11	Port E GPIO eSCI_D Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	F3	F3
PE4	PE[4] TXD_E eMIOS[27]	68	00 01 10 11	Port E GPIO eSCI_E Transmit eMIOS Channel —	I/O O I/O	V_{DDE2}	SH	—	—	G3	G3
PE5	PE[5] RXD_E eMIOS[26]	69	00 01 10 11	Port E GPIO eSCI_E Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	H3	H3
PE6	PE[6] TXD_F eMIOS[25]	70	00 01 10 11	Port E GPIO eSCI_F Transmit eMIOS Channel —	I/O O I/O	V_{DDE2}	SH	—	—	M2	M2
PE7	PE[7] RXD_F eMIOS[24]	71	00 01 10 11	Port E GPIO eSCI_F Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	L2	L2
PE8	PE[8] TXD_G PCS_A[1]	72	00 01 10 11	Port E GPIO eSCI_G Transmit DSPI_A Peripheral Chip Select —	I/O O O	V_{DDE2}	SH	—	—	J4	J4
PE9	PE[9] RXD_G PCS_A[4]	73	00 01 10 11	Port E GPIO eSCI_G Receive DSPI_A Peripheral Chip Select —	I/O I O	V_{DDE2}	SH	—	—	M4	M4
PE10	PE[10] TXD_H PCS_B[3]	74	00 01 10 11	Port E GPIO eSCI_H Transmit DSPI_B Peripheral Chip Select —	I/O O O	V_{DDE2}	SH	—	—	N3	N3
PE11	PE[11] RXD_H PCS_B[2]	75	00 01 10 11	Port E GPIO eSCI_H Receive DSPI_B Peripheral Chip Select —	I/O I O	V_{DDE2}	SH	—	—	N4	N4
PE12	PE[12] TXD_J PCS_C[5]	76	00 01 10 11	Port E GPIO eSCI_J Transmit DSPI_C Peripheral Chip Select —	I/O O O	V_{DDE2}	SH	—	—	P4	P4
PE13	PE[13] RXD_J PCS_C[3]	77	00 01 10 11	Port E GPIO eSCI_J Receive DSPI_C Peripheral Chip Select —	I/O I O	V_{DDE2}	SH	—	—	P5	P5

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PG2	PG[2] PCS_D[1] SCL_C AN[50]	98	00 01 10 11	Port G GPIO DSPI_D Peripheral Chip Select I^2C_C Serial Clock ADC Analog Input	I/O O I/O I	V_{DDE3}	SHA	—	—	H14	H14
PG3	PG[3] PCS_D[2] SDA_C AN[51]	99	00 01 10 11	Port G GPIO DSPI_D Peripheral Chip Select I^2C_C Serial Data ADC Analog Input	I/O O I/O I	V_{DDE3}	SHA	—	—	J14	J14
PG4	PG[4] PCS_D[3] SCL_B AN[52]	100	00 01 10 11	Port G GPIO DSPI_D Peripheral Chip Select I^2C_B Serial Clock ADC Analog Input	I/O O I/O I	V_{DDE3}	SHA	—	—	K14	K14
PG5	PG[5] PCS_D[4] SDA_B AN[53]	101	00 01 10 11	Port G GPIO DSPI_D Peripheral Chip Select I^2C_B Serial Data ADC Analog Input	I/O O I/O I	V_{DDE3}	SHA	—	—	L14	L14
PG6	PG[6] PCS_C[1] FEC_MDC AN[54]	102	00 01 10 11	Port G GPIO DSPI_C Peripheral Chip Select Ethernet Mgmt. Data Clock ADC Analog Input	I/O O O I	V_{DDE3}	MHA	—	—	H15	H15
PG7	PG[7] PCS_C[2] FEC_MDIO AN[55]	103	00 01 10 11	Port G GPIO DSPI_C Peripheral Chip Select Ethernet Mgmt. Data I/O ADC Analog Input	I/O O I/O I	V_{DDE3}	MHA	—	—	J15	J15
PG8	PG[8] eMIOS[7] FEC_TX_CLK AN[56]	104	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Clock ADC Analog Input	I/O I/O I I	V_{DDE3}	SHA	—	—	K15	K15
PG9	PG[9] eMIOS[6] FEC_CRS AN[57]	105	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Carrier Sense ADC Analog Input	I/O I/O I I	V_{DDE3}	SHA	—	—	L15	L15
PG10	PG[10] eMIOS[5] FEC_TX_ER AN[58]	106	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Error ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	M15	M15
PG11	PG[11] eMIOS[4] FEC_RX_CLK AN[59]	107	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Receive Clock ADC Analog Input	I/O I/O I I	V_{DDE3}	SHA	—	—	J16	J16
PG12	PG[12] eMIOS[3] FEC_TXD[0] AN[60]	108	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	K16	K16

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PG13	PG[13] eMIOS[2] FEC_TXD[1] AN[61]	109	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	L16	L16
PG14	PG[14] eMIOS[1] FEC_TXD[2] AN[62]	110	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	M16	M16
PG15	PG[15] eMIOS[0] FEC_TXD[3] AN[63]	111	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	N16	N16
Port H (16)											
PH0	PH[0] eMIOS[31] FEC_COL	112	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Collision —	I/O I/O I —	V_{DDE3}	SH	—	—	T14	T14
PH1	PH[1] eMIOS[30] FEC_RX_DV	113	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data Valid —	I/O I/O I —	V_{DDE3}	SH	—	—	P16	P16
PH2	PH[2] eMIOS[29] FEC_TX_EN	114	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Transmit Enable —	I/O I/O O —	V_{DDE3}	MH	—	—	R16	R16
PH3	PH[3] eMIOS[28] FEC_RX_ER	115	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Error —	I/O I/O I —	V_{DDE3}	SH	—	—	N15	N15
PH4	PH[4] eMIOS[27] FEC_RXD[0]	116	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	P15	P15
PH5	PH[5] eMIOS[26] FEC_RXD[1]	117	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	R14	R14
PH6	PH[6] eMIOS[25] FEC_RXD[2]	118	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	R15	R15

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for either hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 4}$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

2 $V_{DDE1} – V_{DDE4}$ are separate power segments and may be powered independently with no differential voltage constraints between the power segments. $V_{DDE1} – V_{DDE3}$ pad power segments contain ADC analog input channels and thus the input analog signal level may be clamped to the V_{DDE} level, resulting in inaccurate ADC results if the V_{DDE} voltage level is less than V_{DDA}.

3 When $V_{RCSEL} = V_{DDA}$ (high), the internally generated V_{DD33} voltage may be used to power V_{DDEMLB} as long as the PK[0:2] pads remain in the disabled default state with their output buffers, input buffers, and pull devices disabled.

4 The pad type is indicated by one or more of the following abbreviations: A–analog, F—fast speed, H–high voltage, I—input-only, M–medium speed, S–slow speed. For example, pad type SH designates a slow high-voltage pad.

5 The IHA pads are related to V_{DDA}.

6 Characterization Based Capability:
IOH_F = {12, 20, 30, 40} mA and IOL_F = {24, 40, 50, 65} mA for {00, 01,10, 11} drive mode with V_{DDE} = 3.0 V;
IOH_F = {7, 13, 18, 25} mA and IOL_F = {18, 30, 35, 50} mA for {00, 01, 10, 11} drive mode with V_{DDE} = 2.25 V;
IOH_F = {3, 7, 10, 15} mA and IOL_F = {12, 20, 27, 35} mA for {00, 01, 10, 11} drive mode with V_{DDE} = 1.62 V.

7 Characterization Based Capability:
IOH_S = {6, 11.6} mA and IOL_S = {9.2, 17.7} mA for {slow, medium} I/O with V_{DDEH} = 4.5 V;
IOH_S = {2.8, 5.4} mA and IOL_S = {4.2, 8.1} mA for {slow, medium} I/O with V_{DDEH} = 3.0 V

8 All V_{OL}/V_{OH} values 100% tested with ±2 mA load.

9 Absolute value of current, measured at V_{IL} and V_{IH}.

10 Weak pull up/down inactive. Measured at V_{DDE} = 5.25 V. Applies to pad types: SH and MH. Leakage specification guaranteed only when power supplies are within specified operating conditions.

11 Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to pad types: pad_a and pad_ae.

4.6 Operating Current Specifications

Table 9. Operating Currents

Spec	Characteristic	Symbol	Typ[1] 25 °C Ambient	Max[1] –40–150 °C Junction	Unit
Equations	$I_{TOTAL} = I_{DDE} + I_{DDA} + I_{RH} + I_{DD33} + I_{DDSYN} + I_{RC} + I_{DD}$ $I_{DDE} = I_{DDE1} + I_{DDE2} + I_{DDE3} + I_{DDE4} + I_{DDEMLB}$	—	—	—	—
1	V_{DDE} Current $V_{DDE(1,2,3,4)}$ @ 3.0 V – 5.5 V V_{DDEMLB} @ 2.375 V – 3.6 V Static[2] Dynamic[3]	I_{DDE}	 0 Note 3	 30 25	 µA mA
2	V_{DDA} Current V_{DDA} @ 3.0 V – 5.5 V Run mode Sleep mode – Optional 32 kHz osc enabled	I_{DDA}	 1 20 +5	 30 50 +15	 mA µA µA
3	V_{RH} Current V_{RH} @ 3.0 V – 5.5 V Run mode Sleep mode	I_{RH}	 300 1	 700 30	 µA µA
4	V_{DD33} Current V_{DD33} @ 3.0 V – 3.6 V Run mode Sleep mode	I_{DD33}	 10 10	 20 20	 mA µA

4.8 Low Voltage Characteristics

Table 13. Low Voltage Monitors

Spec	Characteristic	Symbol	Min	Typical	Max	Unit
1	Power-on-Reset Assert Level[1]	V_{POR}	1.5	—	2.8	V
2	Low Voltage Monitor 3.3 V[2] Assert Level De-assert Level	 V_{LVI33A} V_{LVI33D}	 3.00 3.04	 3.05 3.12	 3.10 3.19	V
3	Low Voltage Monitor Synthesizer[3] Assert Level De-assert Level	 $V_{LVISYNA}$ $V_{LVISYND}$	 3.00 3.04	 3.05 3.12	 3.10 3.19	V
4	Low Voltage Monitor 3.0 V Low Threshold[1] VRCSEL = V_{SSA} Assert Level De-assert Level VRCSEL = V_{DDA} Assert Level De-assert Level	 $V_{LVI\_VDDA\_LOA}$ $V_{LVI\_VDDA\_LOD}$ $V_{LVI\_VDDA\_LOA}$ $V_{LVI\_VDDA\_LOD}$	 3.00 3.04 3.25 3.35	 3.05 3.12 3.35 3.45	 3.10 3.19 3.48 3.55	V
5	Low Voltage Monitor 5.0 V[1, 4] Assert Level De-assert Level	 $V_{LVI\_VDDA\_A}$ $V_{LVI\_VDDA\_D}$	 4.35 4.45	 4.475 4.575	 4.55 4.65	V
6	Low Voltage Monitor 5.0 V High Threshold[1, 5] Assert Level De-assert Level	 $V_{LVI\_VDDA\_HA}$ $V_{LVI\_VDDA\_HD}$	 4.50 4.50	 4.675 4.675	 4.80 4.80	V

1 Monitors V_{DDA}.

2 Monitors V_{DD33}.

3 Monitors V_{DDSYN}.

4 Disabled when $V_{RCSEL} = V_{SSA}$.

4.9 Oscillators Electrical Characteristics

Table 14. 3.3 V High Frequency External Oscillator

Spec	Characteristic	Symbol	Min	Max	Unit
1	Frequency Range	f_{ref}	4[1]	40	MHz
2	Duty Cycle of reference	t_{DC}	40	60	%
3	EXTAL Input High Voltage External crystal mode[2] External clock mode	V_{IHEXT}	 V_{XTAL} + 0.4 0.65 × V_{DDSYN}	 V_{DDSYN} + 0.3 V_{DDSYN} + 0.3	V
4	EXTAL Input Low Voltage External crystal mode[3] External clock mode	V_{ILEXT}	 V_{DDSYN} – 0.3 V_{DDSYN} – 0.3	 V_{XTAL} – 0.4 0.35 × V_{DDSYN}	V
5	XTAL Current[4]	I_{XTAL}	1	3	mA
6	Total On-chip stray capacitance on XTAL	C_{S_XTAL}	—	3	pF
7	Total On-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	3	pF

Table 23. De-rated Pad AC Specifications (3.3 V, 3.3 V)[1] (continued)

Spec	Pad Type[2]	SRC/DSC[3]	Out Delay[4,5] (ns)	Rise/Fall[6], (ns)	Load Drive (pF)
3	Fast[8]	00	2.5	1.2	10
		01		1.2	20
		10		1.2	30
		11		1.2	50
4	Input	N/A	3/3	1.5/1.5	0.5

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at F_{SYS} = 116 MHz, V_{DD} = 1.08 – 1.32 V, V_{DDE} = 3.0 – 3.6 V, V_{DDEH} = 3.0 – 3.6 V, V_{RC33} and V_{DDPLL} = 3.0 – 3.6 V, $T_A = T_L$ to T_H.

2 Slow = SH or SHA; Medium = MH or MHA; Fast = F; Input = IHA. See Table 2.

3 SRC/DSC are bit fields in the Pad Configuration Registers. SRC—Slew Rate Control (slow and medium pad types only), DSC—Drive Strength Control (fast pad type only).

4 This parameter is supplied for reference and is not guaranteed by design and not tested.

5 Delay and rise/fall are measured to 20% or 80% of the respective signal.

6 This parameter is guaranteed by characterization before qualification rather than 100% tested.

7 Add a maximum of one system clock to the output delay for delay with respect to system clock.

8 Output delay is shown in Figure 6. Add a maximum of one system clock to the output delay for delay with respect to system clock.

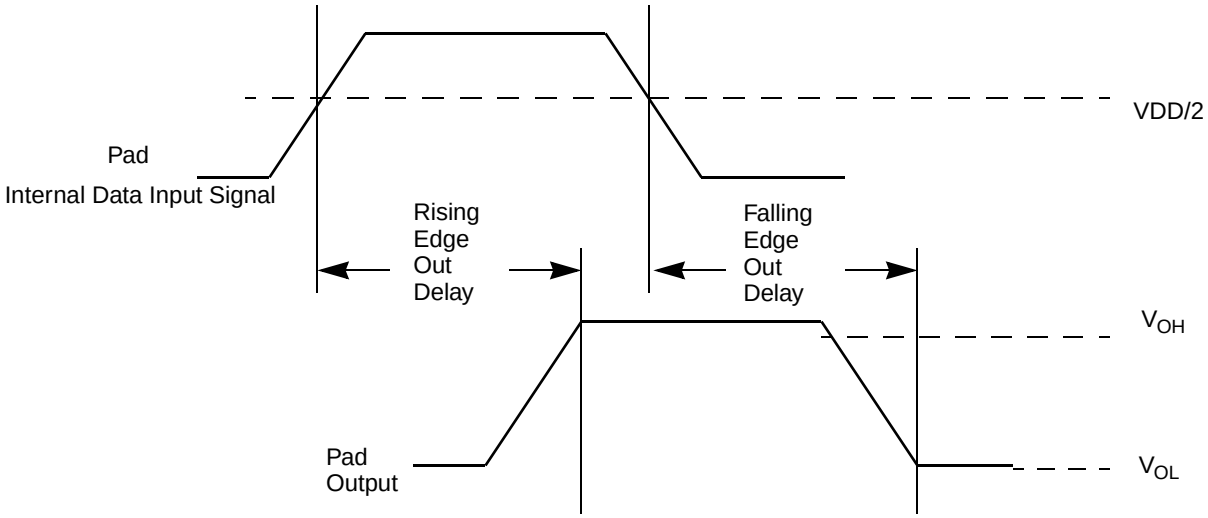


Figure 6. Pad Output Delay

4.14 AC Timing

4.14.1 Reset and Boot Configuration Pins

Table 24. Reset and Boot Configuration Timing

Spec	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	150	—	ns
2	BOOTCFG Setup Time after $\overline{\text{RESET}}$ Valid	t_{RCSU}	—	100	µs
3	BOOTCFG Hold Time from $\overline{\text{RESET}}$ Valid	t_{RCH}	0	—	µs

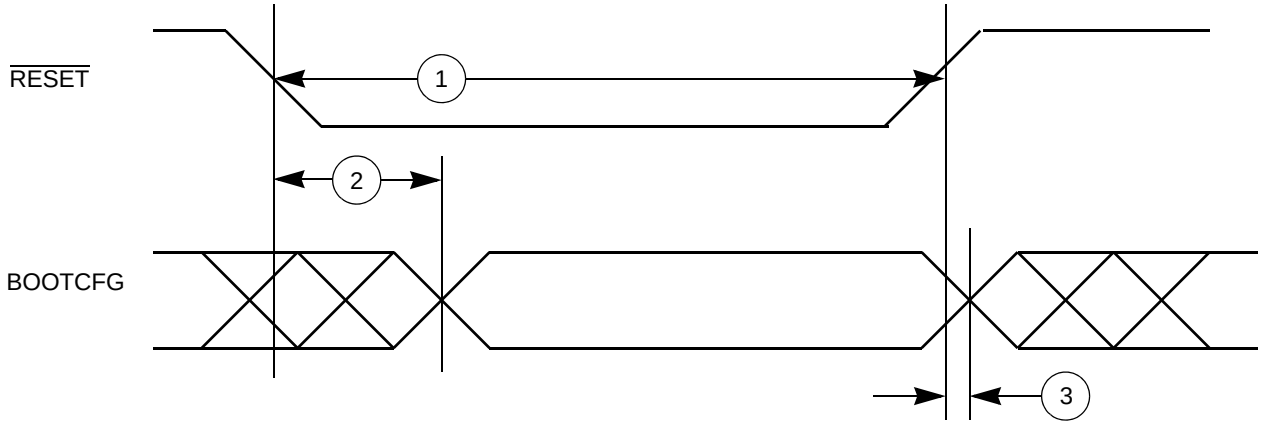


Figure 7. Reset and Boot Configuration Timing

4.14.2 External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) Pins

Table 25. IRQ/NMI Timing

Spec	Characteristic	Symbol	Min	Max	Unit
1	IRQ/NMI Pulse Width Low	t_{IPWL}	3	—	t_{SYS}
2	IRQ/NMI Pulse Width High	T_{IPWH}	3	—	t_{SYS}
3	IRQ/NMI Edge to Edge Time[1]	t_{ICYC}	6	—	t_{SYS}

[1] Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

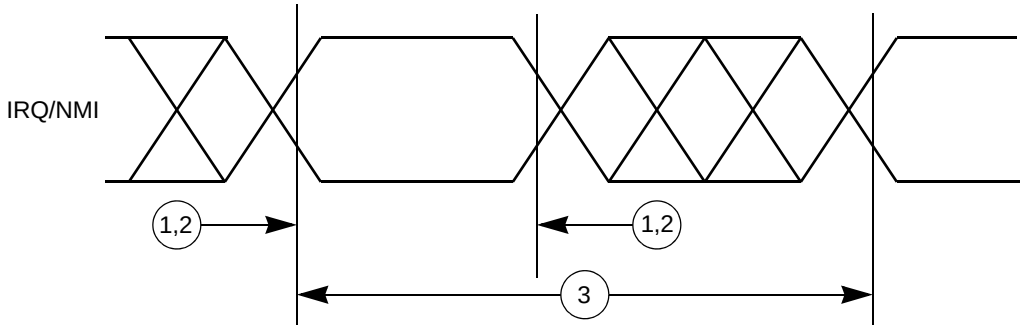


Figure 8. IRQ and NMI Timing

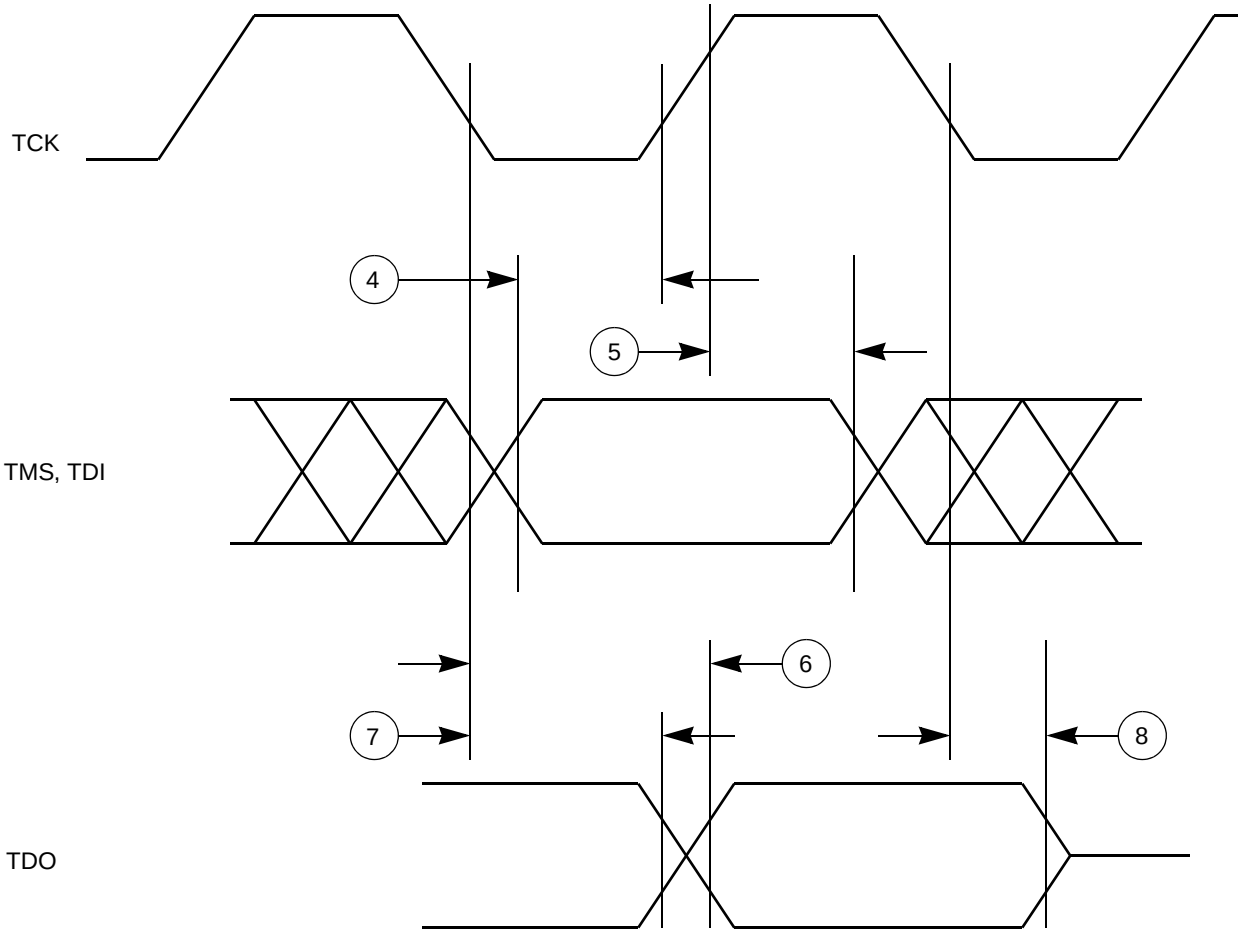


Figure 10. JTAG Test Access Port Timing

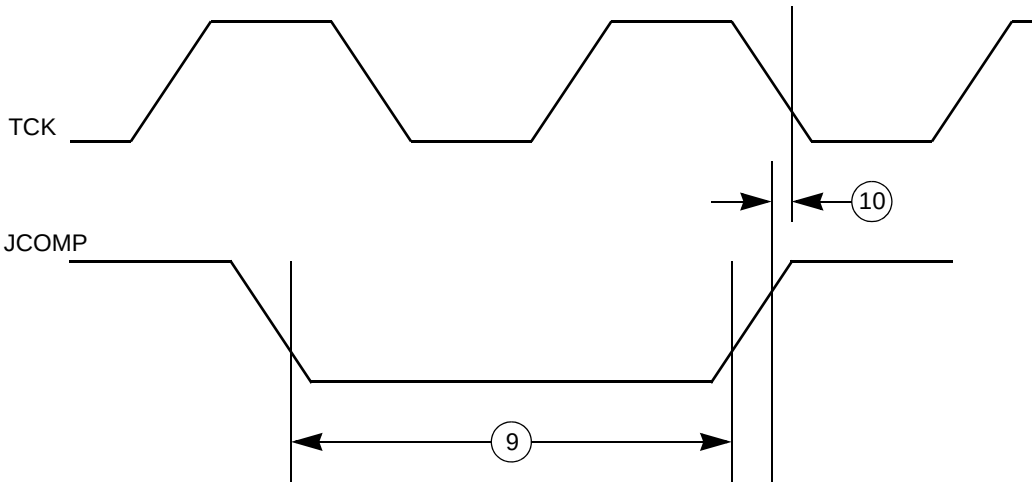


Figure 11. JTAG JCOMP Timing

4.14.5 Enhanced Modular I/O Subsystem (eMIOS)

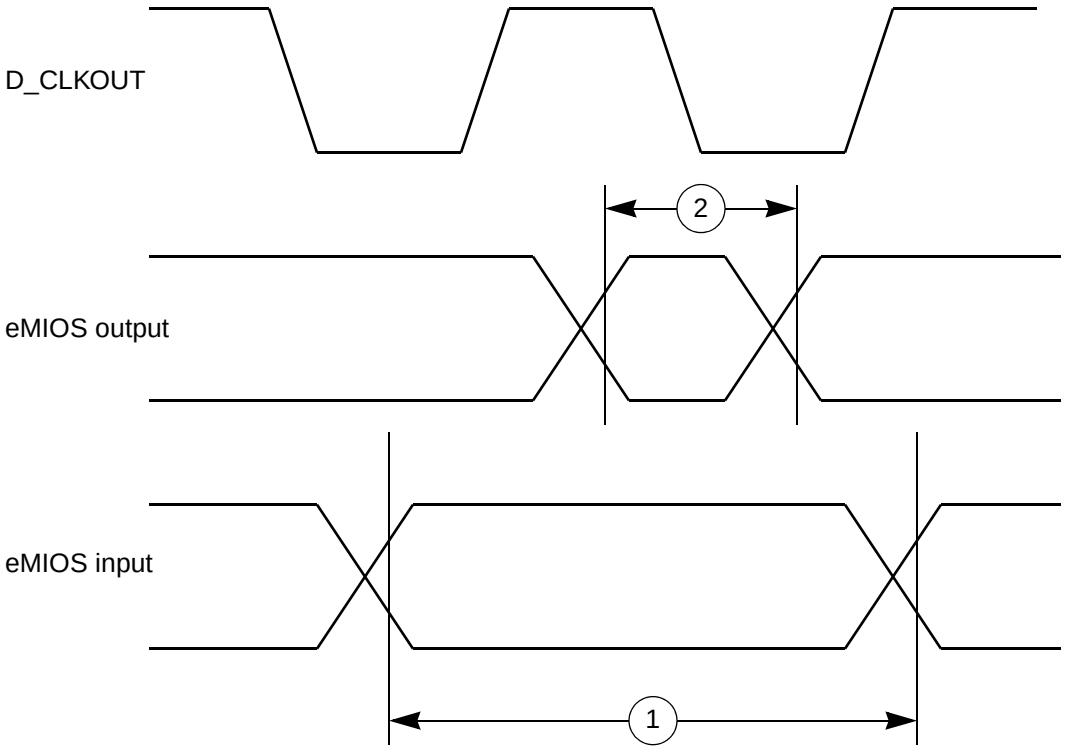
Table 28. eMIOS Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{CYC}
2	eMIOS Output Pulse Width	t_{MOPW}	1[2]	—	t_{CYC}

1 eMIOS timing specified at V_{DDE} = 3.0 – 5.5 V, $T_A = T_L$ to T_H, and CL = 30 pF with SRC = 0b11.

2 This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

Figure 15. eMIOS Timing



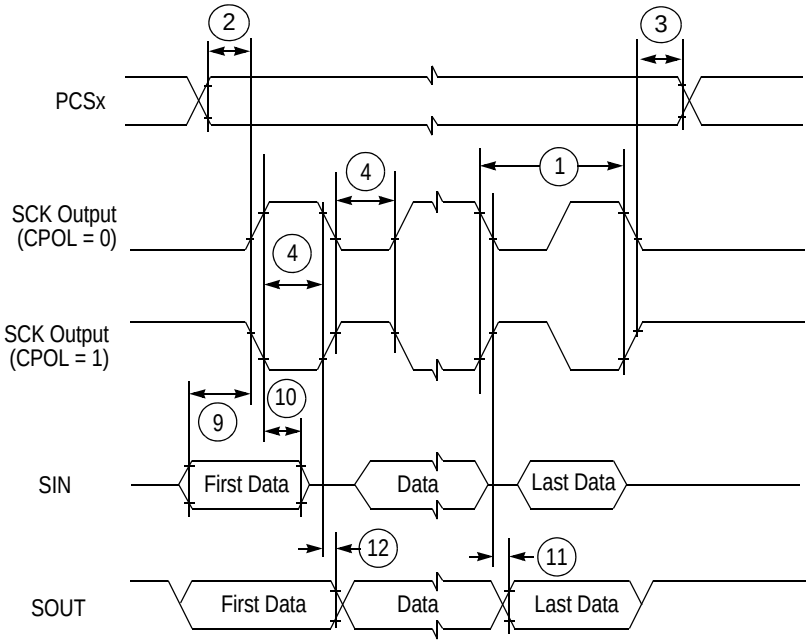


Figure 16. DSPI Classic SPI Timing — Master, CPHA = 0

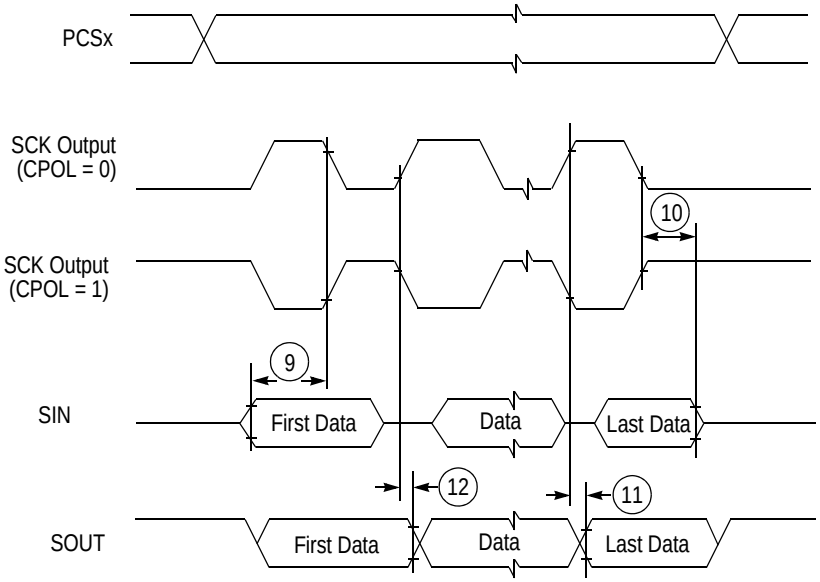


Figure 17. DSPI Classic SPI Timing — Master, CPHA = 1

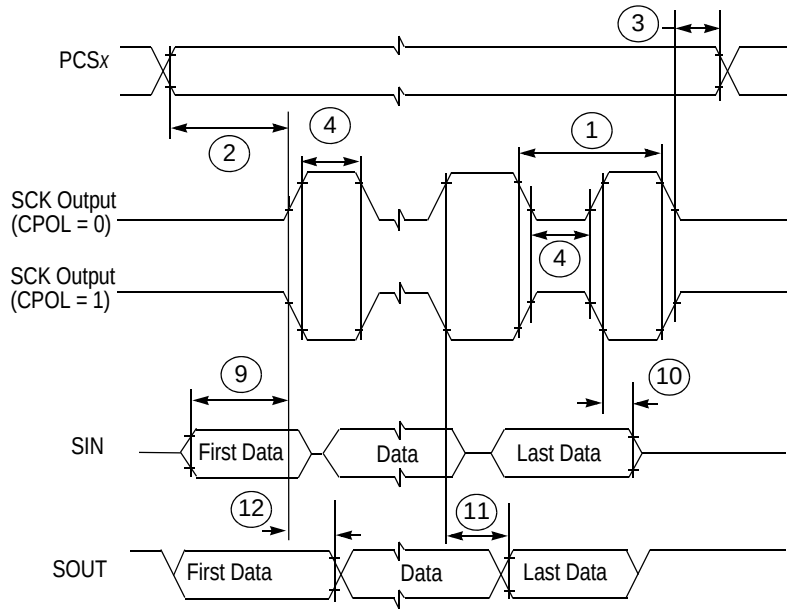


Figure 20. DSPI Modified Transfer Format Timing — Master, CPHA = 0

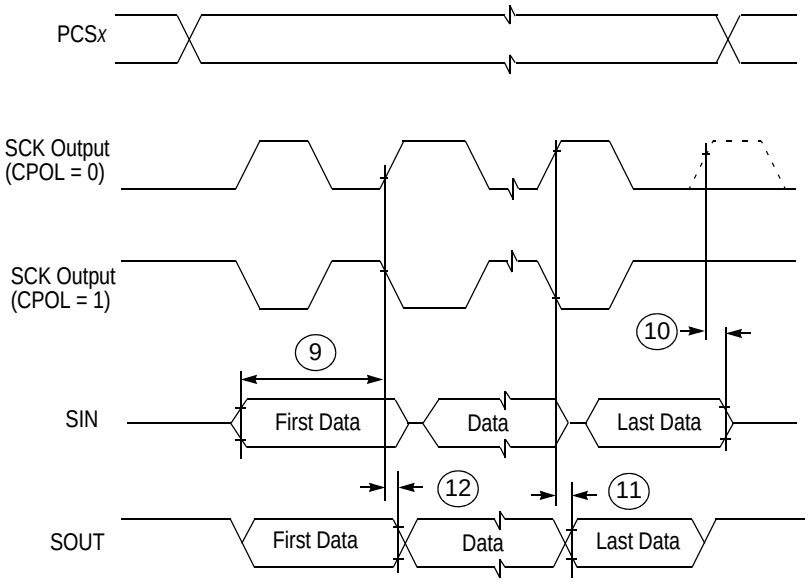


Figure 21. DSPI Modified Transfer Format Timing — Master, CPHA = 1

4.14.8.3 MII Async Inputs Signal Timing (CRS and COL)

Table 35. MII Async Inputs Signal Timing[1]

Spec	Characteristic	Min	Max	Unit
M9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

1 Output pads configured with SRC = 0b11.

Figure 28. MII Async Inputs Timing Diagram

4.14.8.4 MII Serial Management Channel Timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 36. MII Serial Management Channel Timing[1]

Spec	Characteristic	Min	Max	Unit
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	10	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

1 Output pads configured with SRC = 0b11.

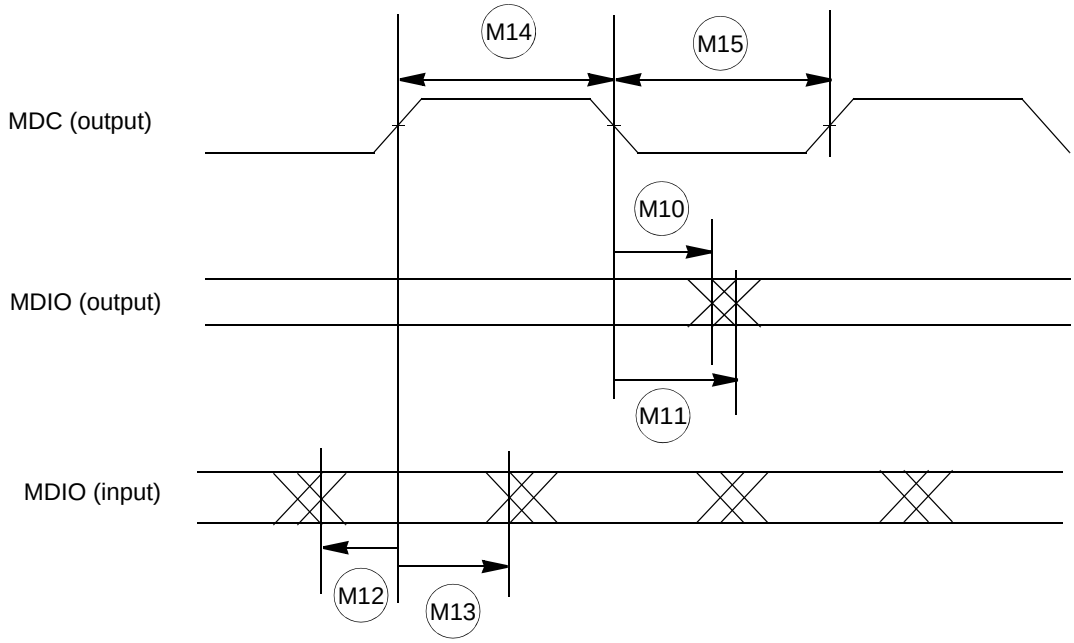


Figure 29. MII Serial Management Channel Timing Diagram

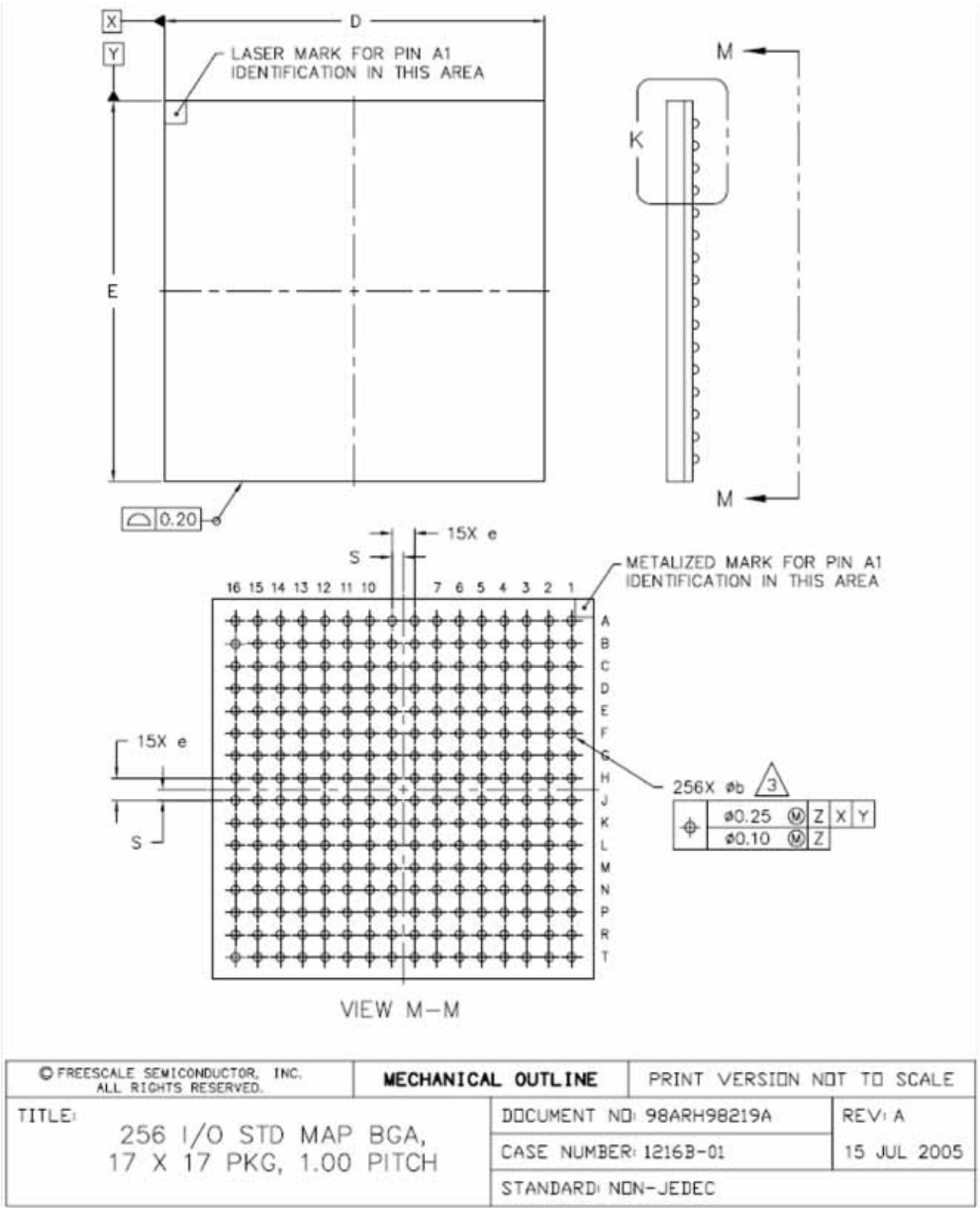


Figure 32. 256 MAPBGA Package Mechanical Drawing