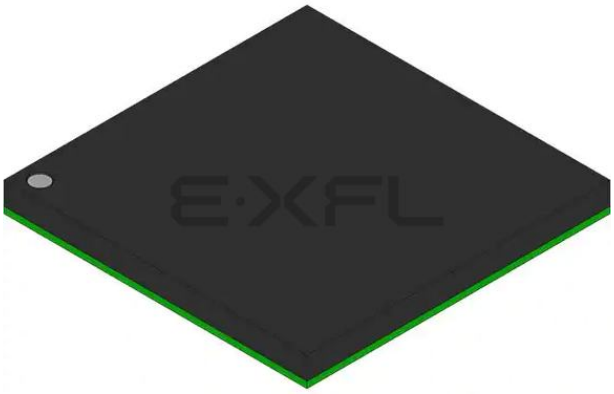

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z650
Core Size	32-Bit Single-Core
Speed	116MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	155
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	592K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 36x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BGA
Supplier Device Package	208-BGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5668gf1avmg

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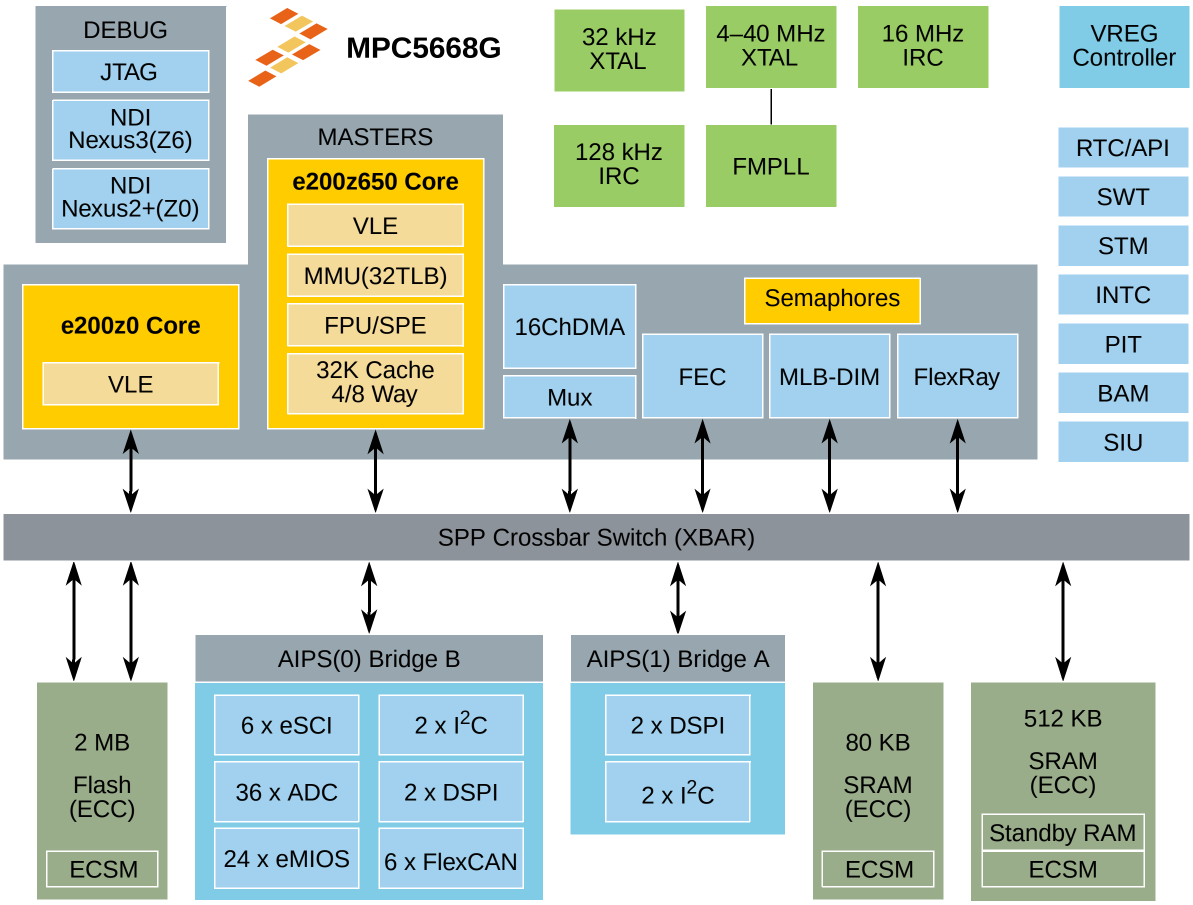
Table 1. MPC5668G/MPC5668E Comparison

Feature	MPC5668G		MPC5668E	
Package	**208 MAPBGA**	**256 MAPBGA**	**208 MAPBGA**	**256 MAPBGA**
RAM with ECC	592 KB		128 KB	
MPU	No		16 entry	
DMA	16-channel		32-channel	
Ethernet (FEC)	Yes		No	
MediaLB (MLB-DIM)	Yes		No	
FlexRay	Yes (128 Message Buffers)		No	
ADC (10-bit)	36 internal channels Supports 32 external channels		64 internal channels Supports 32 external channels	
Total Timer I/O (eMIOS200)	24 channels, 16-bit		32 channels, 16-bit	
Cross Trigger Unit (CTU)	No		Yes	
SCI (eSCI)	6		12	
SPI (DSPI)	4		4	
CAN (FlexCAN)	6		5	
I^2C	4		4	
Nexus3 Debug (e200Z6) Nexus2+ Debug (e200Z0)	—	Supported on 256BGA emulation package	—	Supported on 256BGA emulation package

2 MPC5668x Block Diagrams

Figure 1 shows a top-level block diagram of the MPC5668G device.



LEGEND

ADC – Analog to Digital Converter
BAM – Boot Assist Module
DSPI – Serial Peripherals Interface
ECC – Error Correction Code
ECSM – Error Correction Status Module
eMIOS – Timed Input Output
eDMA – Enhanced Direct Memory Access controller
eSCI – Serial Communications Interface
FEC – Fast Ethernet Controller
FlexCAN – Controller Area Network controller
FlexRay™ – FlexRay Bus Controller
FMPLL – Frequency Modulated Phase Locked Loop
I^2C – Inter IC Controller
INTC – Interrupt Controller
JTAG – Joint Test Action Group interface
MLB-DIM – Media Local Bus Device Interface Module
NDI – Nexus Debug Interface
PIT – Periodic Interrupt Timer
RTC – Real Time Clock
SIU – System Integration
STM – System Timer Module
SWT – Software Watchdog Timer
VREG – Voltage Regulator

Figure 1. MPC5668G Block Diagram

3 Pin Assignments

3.1 208-ball MAPBGA Pin Assignments

Figure 3 shows the 208-ball MAPBGA pin assignments.

208 MAPBGA Ball Map
(as viewed from top through the package)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	V_{SS}	PD0	PG1	PC12	PC9	PC7	PC2	PB13	PB10	PB8	RESET	V_{DDSYN}	XTAL	EXTAL	V_{SSSYN}	V_{SS}	A
B	PD2	PD1	PG0	PC11	PC10	PC8	PC3	PB14	PB11	V_{RC}	V_{RCCTL}	PB9	PB2	PB0	V_{DDA}	V_{RH}	B
C	PD3	PD4	PD14	PC14	PC13	PC5	PC6	PC1	PB15	PB12	PB6	PB4	PB3	PB1	V_{SSA}	V_{RL}	C
D	PD5	PD6	PD15	V_{DD}	PC15	V_{DDE1}	V_{SS}	PC4	PC0	V_{DD}	PB7	PB5	PA10	PA12	PA0	PA14	D
E	PD7	PD8	PE0	PE1									PA11	PA9	PA1	PA15	E
F	PD9	PD10	PE3	PE2									PA13	PA8	PA3	PA2	F
G	PD11	PD12	PE4	V_{SS}			V_{SS}	V_{SS}	V_{SS}	V_{SS}			V_{DD}	PA7	PA5	PA4	G
H	PD13	PF0	PE5	V_{DD}			V_{SS}	V_{SS}	V_{SS}	V_{SS}			V_{RCSEL}	PG2	PG6	PA6	H
J	PF1	PF2	TDI	PE8			V_{SS}	V_{SS}	V_{SS}	V_{SS}			V_{DDE3}	PG3	PG7	PG11	J
K	PK1	PK2	JCOMP	V_{DDEMLB}			V_{SS}	V_{SS}	V_{SS}	V_{SS}			V_{DD}	PG4	PG8	PG12	K
L	PK0	PE7	TMS	V_{DDE2}									V_{DD33}	PG5	PG9	PG13	L
M	PF4	PE6	TDO	PE9									TEST	PF13	PG10	PG14	M
N	PF6	PF3	PE10	PE11	V_{DD}	PE15	PE14	PH9	PH11	V_{DDE4}	PH15	PJ10	V_{SS}	PF12	PH3	PG15	N
P	PF8	PF5	TCK	PE12	PE13	PK10	PH8	PH10	PH12	PH13	PH14	PJ11	PF15	PF14	PH4	PH1	P
R	PF10	PF7	PF11	PK4	PK6	PK8	PJ0	PJ2	PJ4	PJ6	PJ9	PJ12	PJ14	PH5	PH6	PH2	R
T	V_{SS}	PF9	PK3	PK5	PK7	PK9	PJ1	PJ3	PJ5	PJ7	PJ8	PJ13	PJ15	PH0	PH7	V_{SS}	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 3. MPC5668x 208-ball MAPBGA (full diagram)

3.2 256-ball MAPBGA Pin Assignments

Figure 4 shows the 256-ball MAPBGA pin assignments.

256 MAPBGA Ball Map

(as viewed from top through the package)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	V_{SS}	PD0	PG1	PC12	PC9	PC7	PC2	PB13	PB10	PB8	RESET	V_{DDSYN}	XTAL	EXTAL	V_{SSSYN}	V_{SS}	A
B	PD2	PD1	PG0	PC11	PC10	PC8	PC3	PB14	PB11	V_{RC}	V_{RCCTL}	PB9	PB2	PB0	V_{DDA}	V_{RH}	B
C	PD3	PD4	PD14	PC14	PC13	PC5	PC6	PC1	PB15	PB12	PB6	PB4	PB3	PB1	V_{SSA}	V_{RL}	C
D	PD5	PD6	PD15	V_{DD}	PC15	V_{DDE1}	V_{SS}	PC4	PC0	V_{DD}	PB7	PB5	PA10	PA12	PA0	PA14	D
E	PD7	PD8	PE0	PE1	MDO0	V_{DDENEX}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	PA11	PA9	PA1	PA15	E
F	PD9	PD10	PE3	PE2	MDO1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	PA13	PA8	PA3	PA2	F
G	PD11	PD12	PE4	V_{SS}	MDO2	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	PA7	PA5	PA4	G
H	PD13	PF0	PE5	V_{DD}	MDO3	MDO4	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{RCSEL}	PG2	PG6	PA6	H
J	PF1	PF2	TDI	PE8	MDO6	MDO5	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDE3}	PG3	PG7	PG11	J
K	PK1	PK2	JCOMP	V_{DDEMLB}	MDO7	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDENEX}	V_{SS}	V_{DD}	PG4	PG8	PG12	K
L	PK0	PE7	TMS	V_{DDE2}	MDO8	V_{SS}	V_{DDENEX}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD33}	PG5	PG9	PG13	L
M	PF4	PE6	TDO	PE9	MDO9	MDO10	MDO11	MSEO1	MSEO0	MCKO	EVTI	EVTO	TEST	PF13	PG10	PG14	M
N	PF6	PF3	PE10	PE11	V_{DD}	PE15	PE14	PH9	PH11	V_{DDE4}	PH15	PJ10	V_{SS}	PF12	PH3	PG15	N
P	PF8	PF5	TCK	PE12	PE13	PK10	PH8	PH10	PH12	PH13	PH14	PJ11	PF15	PF14	PH4	PH1	P
R	PF10	PF7	PF11	PK4	PK6	PK8	PJ0	PJ2	PJ4	PJ6	PJ9	PJ12	PJ14	PH5	PH6	PH2	R
T	V_{SS}	PF9	PK3	PK5	PK7	PK9	PJ1	PJ3	PJ5	PJ7	PJ8	PJ13	PJ15	PH0	PH7	V_{SS}	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 4. MPC5668x 256-ball MAPBGA (full diagram)

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Voltage	Pad Type[5]	Status During Reset[6]	Status After Reset[7]	Package Pin Locations 208 BGA	Package Pin Locations 256 BGA
Port B (16)											
PB0	PB[0] AN[16]/ANW	16	00 01 10 11	Port B GPIO ADC Analog Input/Mux In — —	I/O I — —	V_{DDE1}	SHA	—	—	B14	B14
PB1	PB[1] AN[17]/ANX	17	00 01 10 11	Port B GPIO ADC Analog Input/Mux In — —	I/O I — —	V_{DDE1}	SHA	—	—	C14	C14
PB2	PB[2] AN[18]/ANY	18	00 01 10 11	Port B GPIO ADC Analog Input/Mux In — —	I/O I — —	V_{DDE1}	SHA	—	—	B13	B13
PB3	PB[3] AN[19]/ANZ	19	00 01 10 11	Port B GPIO ADC Analog Input/Mux In — —	I/O I — —	V_{DDE1}	SHA	—	—	C13	C13
PB4	PB[4] AN[20]	20	00 01 10 11	Port B GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	C12	C12
PB5	PB[5] AN[21]	21	00 01 10 11	Port B GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	D12	D12
PB6	PB[6] AN[22]	22	00 01 10 11	Port B GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	C11	C11
PB7	PB[7] AN[23]	23	00 01 10 11	Port B GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	D11	D11
PB8	PB[8] AN[24] PCS_A[2]	24	00 01 10 11	Port B GPIO ADC Analog Input DSPI_A Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	A10	A10
PB9	PB[9] AN[25] PCS_A[3]	25	00 01 10 11	Port B GPIO ADC Analog Input DSPI_A Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	B12	B12

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Voltage	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PC4	PC[4] AN[36]	36	00 01 10 11	Port C GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	D8	D8
PC5	PC[5] AN[37] Z6NMI	37	00 01 10 11	Port C GPIO ADC Analog Input Z6 Core Non-Maskable Interrupt —	I/O I I —	V_{DDE1}	SHA	—	—	C6	C6
PC6	PC[6] AN[38] Z0NMI	38	00 01 10 11	Port C GPIO ADC Analog Input Z0 Core Non-Maskable Interrupt —	I/O I I —	V_{DDE1}	SHA	—	—	C7	C7
PC7	PC[7] AN[39] FR_DBG3	39	00 01 10 11	Port C GPIO ADC Analog Input FlexRay Debug —	I/O I O —	V_{DDE1}	SHA	—	—	A6	A6
PC8	PC[8] AN[40] FR_DBG2	40	00 01 10 11	Port C GPIO ADC Analog Input FlexRay Debug —	I/O I O —	V_{DDE1}	SHA	—	—	B6	B6
PC9	PC[9] AN[41] FR_DBG1	41	00 01 10 11	Port C GPIO ADC Analog Input FlexRay Debug —	I/O I O —	V_{DDE1}	SHA	—	—	A5	A5
PC10	PC[10] AN[42] FR_DBG0	42	00 01 10 11	Port C GPIO ADC Analog Input FlexRay Debug —	I/O I O —	V_{DDE1}	SHA	—	—	B5	B5
PC11	PC[11] AN[43] SCL_C —	43	00 01 10 11	Port C GPIO ADC Analog Input I^2C_C Serial Clock —	I/O I I/O —	V_{DDE1}	SHA	—	—	B4	B4
PC12	PC[12] AN[44] SDA_C —	44	00 01 10 11	Port C GPIO ADC Analog Input I^2C_C Serial Data —	I/O I I/O —	V_{DDE1}	SHA	—	—	A4	A4
PC13	PC[13] AN[45] — MA[0]	45	00 01 10 11	Port C GPIO ADC Analog Input — ADC Ext. Mux Address Select	I/O I — O	V_{DDE1}	SHA	—	—	C5	C5
PC14	PC[14] AN[46] MA[1] —	46	00 01 10 11	Port C GPIO ADC Analog Input ADC Ext. Mux Address Select —	I/O I — O	V_{DDE1}	SHA	—	—	C4	C4

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Voltage	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PE14	PE[14] SCL_A PCS_D[2]	78	00 01 10 11	Port E GPIO I^2C_A Serial Clock DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE2}	SH	—	—	N7	N7
PE15	PE[15] SDA_A PCS_D[5]	79	00 01 10 11	Port E GPIO I^2C_A Serial Data DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE2}	SH	—	—	N6	N6
Port F (16)											
PF0	PF[0] SCK_A	80	00 01 10 11	Port F GPIO DSPI_A Serial Clock — —	I/O I/O — —	V_{DDE2}	MH	—	—	H2	H2
PF1	PF[1] SOUT_A	81	00 01 10 11	Port F GPIO DSPI_A Serial Data Out — —	I/O O — —	V_{DDE2}	MH	—	—	J1	J1
PF2	PF[2] SIN_A	82	00 01 10 11	Port F GPIO DSPI_A Serial Data In — —	I/O I — —	V_{DDE2}	SH	—	—	J2	J2
PF3	PF[3] PCS_A[0] PCS_B[5] PCS_C[4]	83	00 01 10 11	Port F GPIO DSPI_A Peripheral Chip Select DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I/O O O	V_{DDE2}	SH	—	—	N2	N2
PF4	PF[4] SCK_B PCS_A[1] PCS_C[2]	84	00 01 10 11	Port F GPIO DSPI_B Serial Clock DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I/O O O	V_{DDE2}	MH	—	—	M1	M1
PF5	PF[5] SOUT_B PCS_A[2] PCS_C[3]	85	00 01 10 11	Port F GPIO DSPI_B Serial Data Out DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	P2	P2
PF6	PF[6] SIN_B PCS_A[3] PCS_C[5]	86	00 01 10 11	Port F GPIO DSPI_B Serial Data In DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I O O	V_{DDE2}	SH	—	—	N1	N1
PF7	PF[7] PCS_B[0] PCS_C[5] PCS_D[4]	87	00 01 10 11	Port F GPIO DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE2}	SH	—	—	R2	R2

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Voltage	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PG13	PG[13] eMIOS[2] FEC_TXD[1] AN[61]	109	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	L16	L16
PG14	PG[14] eMIOS[1] FEC_TXD[2] AN[62]	110	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	M16	M16
PG15	PG[15] eMIOS[0] FEC_TXD[3] AN[63]	111	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	N16	N16
Port H (16)											
PH0	PH[0] eMIOS[31] FEC_COL	112	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Collision —	I/O I/O I —	V_{DDE3}	SH	—	—	T14	T14
PH1	PH[1] eMIOS[30] FEC_RX_DV	113	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data Valid —	I/O I/O I —	V_{DDE3}	SH	—	—	P16	P16
PH2	PH[2] eMIOS[29] FEC_TX_EN	114	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Transmit Enable —	I/O I/O O —	V_{DDE3}	MH	—	—	R16	R16
PH3	PH[3] eMIOS[28] FEC_RX_ER	115	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Error —	I/O I/O I —	V_{DDE3}	SH	—	—	N15	N15
PH4	PH[4] eMIOS[27] FEC_RXD[0]	116	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	P15	P15
PH5	PH[5] eMIOS[26] FEC_RXD[1]	117	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	R14	R14
PH6	PH[6] eMIOS[25] FEC_RXD[2]	118	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	R15	R15

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Voltage	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PJ12	PJ[12] eMIOS[03]	140	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	R12	R12
PJ13	PJ[13] eMIOS[02]	141	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	T12	T12
PJ14	PJ[14] eMIOS[01]	142	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	R13	R13
PJ15	PJ[15] eMIOS[00]	143	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	T13	T13
Port K (11)											
PK0	PK[0] MLBCLK SCK_B CLKOUT	144	00 01 10 11	Port K GPIO Media Local Bus Clock DSPI_B Serial Clock CLKOUT (Test Only)	I/O I I/O O	V_{DDEMLB}	F	—	—	L1	L1
PK1	PK[1] MLBSIG SOUT_B PCS_D[4]	145	00 01 10 11	Port K GPIO Media Local Bus Signal DSPI_B Serial Data Out DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDEMLB}	F	—	—	K1	K1
PK2	PK[2] MLBDAT SIN_B PCS_D[5]	146	00 01 10 11	Port K GPIO Media Local Bus Data DSPI_B Serial Data In DSPI_D Peripheral Chip Select	I/O I/O I O	V_{DDEMLB}	F	—	—	K2	K2
PK3	PK[3] FR_A_RX MA[0] PCS_C[1]	147	00 01 10 11	Port K GPIO FlexRay A Receive Data ADC Ext. Mux Address Select DSPI_C Peripheral Chip Select	I/O I O O	V_{DDE2}	SH	—	—	T3	T3
PK4	PK[4] FR_A_TX MA[1] PCS_C[2]	148	00 01 10 11	Port K GPIO FlexRay A Transmit Data ADC Ext. Mux Address Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	R4	R4
PK5	PK[5] FR_A_TX_EN MA[2] PCS_C[3]	149	00 01 10 11	Port K GPIO FlexRay A Transmit Enable ADC Ext. Mux Address Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	T4	T4

3.3.1 Power and Ground Supply Summary

Table 3. MPC5668x Power/Ground

Pin Name	Function Description	Voltage[1]	Package Pin Locations	
			208	256
V_{DD}	Internal Logic Power	1.2 V	D4, D10, H4, G13, K13, N5	D4, D10, H4, G13, K13, N5
V_{DDE1}	External I/O Power	3.3–5.0 V	D6	D6
V_{DDE2}			L4	L4
V_{DDE3}			J13	J13
V_{DDE4}			N10	N10
V_{DDA}	Analog Power	3.3–5.0 V	B15	B15
V_{DD33}	3.3 V I/O Power	3.3 V	L13	L13
V_{DDEMLB}	Media Local Bus Power	2.5 or 3.3 V	K4	K4
V_{DDENEX}[2]	Nexus Power	3.3 V	—	E6, K11, L7
V_{RCSEL}	Voltage Regulator Select	V_{SSA} / V_{DDA}	H13	H13
V_{RC}	Voltage Regulator Control Voltage	3.3–5.0 V	B10	B10
V_{RCCTL}	Voltage Regulator Control Output	—[3]	B11	B11
V_{DDSYN}	Clock Synthesizer Power	3.3 V	A12	A12
V_{RH}	Analog High Voltage Reference	3.3–5.0 V	B16	B16
V_{RL}	Analog Low Voltage Reference	0 V	C16	C16
V_{SS}	Ground	0 V	A1, A16, D7, G4, G[7:10], H[7:10], J[7:10], K[7:10], N13, T1, T16	A1, A16, D7, E[7:12], F[7:12], G4, G[6:12], H[7:12], J[7:12], K[6:10], K12, L[8:10], L12, N13, T1, T16
V_{SSA}	Analog Ground	0 V	C15	C15
V_{SSSYN}	Clock Synthesizer Ground	0 V	A15	A15

1 Nominal voltages.

2 Dedicated Nexus power pin on 256-pin package only. On the 208-pin package, VDDENEX is tied to VSS internal to the package substrate and is not available externally.

3 Base current to external NPN power transistor. Voltage may vary.

4 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5668x.

4.1 Maximum Ratings

Table 4. Absolute Maximum Ratings[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	1.2 V Core Supply Voltage[2]	V_{DD}	–0.3	1.32[3]	V
2	3.3 V Clock Synthesizer Voltage[2, 4]	V_{DDSYN}	–0.3	3.6	V
3	3.3 V I/O Buffer Voltage [2, 4]	V_{DD33}	–0.3	3.6	V
4	3.3–5.0 V Voltage Regulator Control Voltage [2, 5, 6]	V_{RC}	–0.3	5.5	V
5	3.3–5.0 V Analog Supply Voltage (reference to V_{SSA}) [2, 5]	V_{DDA}	–0.3	5.5	V
6	3.3–5.0 V External I/O Supply Voltage [2, 5, 7]	V_{DDE1}[8] V_{DDE2}[8] V_{DDE3}[8] V_{DDE4}[8]	–0.3 –0.3 –0.3 –0.3	5.5 5.5 5.5 5.5	V
7	2.5–3.3 V External I/O Supply Voltage (MLB) [2, 4]	V_{DDEMLB}[8]	–0.3	3.6	V
8	3.3 V External I/O Supply Voltage (Nexus) [2, 4]	V_{DDENEX}[8]	–0.3	3.6	V
9	DC Input Voltage[9] V_{DDE1}, V_{DDE2}, V_{DDE3}, V_{DDE4} V_{DDEMLB}, V_{DDENEX}	V_{IN}	 –1.0[10] –1.0[9]	 V_{DDEx} + 0.3 V[11] V_{DDEx} + 0.3 V[10]	V
10	Analog Reference High Voltage	V_{RH}	–0.3	Minimum of 5.5 or V_{DDA} + 0.3	V
11	Analog Reference Low Voltage	V_{RL}	–0.3	5.5	V
12	V_{SS} to V_{SSA} Differential Voltage	$V_{SS} – V_{SSA}$	–100	100	mV
13	V_{SS} to V_{SSSYN} Differential Voltage	$V_{SS} – V_{SSSYN}$	–100	100	mV
14	Maximum DC Digital Input Current[12] (per pin, applies to all digital F, MH, SH, and IH pins)	I_{MAXD}	–2	2	mA
15	Maximum DC Analog Input Current[13] (per pin, applies to all analog AE and A pins)	I_{MAXA}	–3	3	mA
16	Storage Temperature Range	T_{STG}	–55.0	150.0	^oC
17	Maximum Solder Temperature[14]	T_{SDR}	—	235.0	^oC
18	Moisture Sensitivity Level[15]	MSL	—	3	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

3 2.0 V for 10 hours cumulative time, 1.2 V +10% for time remaining.

4 5.3 V for 10 hours cumulative time, 3.3 V +10% for time remaining.

5 6.4 V for 10 hours cumulative time, 5.0 V +10% for time remaining.

6 VRC cannot be 100mV higher than VDDA. VDDSYN and VDD33 cannot be 100mV higher than VRC.

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The supplied thermal resistances are provided based on JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined on the single-layer (1s) board and on the four-layer board with two signal layers and a power and a ground plane (2s2p) clearly demonstrate that the effective thermal resistance of the component is not a constant. It depends on the construction of the application board (number of planes), the effective size of the board which cools the component, how well the component is thermally and electrically connected to the planes, and the power being dissipated by adjacent components.

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between through vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the application board has one oz. (35 micron nominal thickness) internal planes, the components are well separated, and the overall power dissipation on the board is less than 0.02 W/cm^2.

The thermal performance of any component depends strongly on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D) \qquad \textit{Eqn. 2}$$

where:

T_J = junction temperature (^oC)

T_B = board temperature at the package perimeter ($^oC/W$)

$R_{\theta JB}$ = junction to board thermal resistance ($^oC/W$) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition, with the component soldered to a board with internal planes.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad \textit{Eqn. 3}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

4.8 Low Voltage Characteristics

Table 13. Low Voltage Monitors

Spec	Characteristic	Symbol	Min	Typical	Max	Unit
1	Power-on-Reset Assert Level[1]	V_{POR}	1.5	—	2.8	V
2	Low Voltage Monitor 3.3 V[2] Assert Level De-assert Level	 V_{LVI33A} V_{LVI33D}	 3.00 3.04	 3.05 3.12	 3.10 3.19	V
3	Low Voltage Monitor Synthesizer[3] Assert Level De-assert Level	 $V_{LVISYNA}$ $V_{LVISYND}$	 3.00 3.04	 3.05 3.12	 3.10 3.19	V
4	Low Voltage Monitor 3.0 V Low Threshold[1] VRCSEL = V_{SSA} Assert Level De-assert Level VRCSEL = V_{DDA} Assert Level De-assert Level	 $V_{LVI\_VDDA\_LOA}$ $V_{LVI\_VDDA\_LOD}$ $V_{LVI\_VDDA\_LOA}$ $V_{LVI\_VDDA\_LOD}$	 3.00 3.04 3.25 3.35	 3.05 3.12 3.35 3.45	 3.10 3.19 3.48 3.55	V
5	Low Voltage Monitor 5.0 V[1, 4] Assert Level De-assert Level	 $V_{LVI\_VDDA\_A}$ $V_{LVI\_VDDA\_D}$	 4.35 4.45	 4.475 4.575	 4.55 4.65	V
6	Low Voltage Monitor 5.0 V High Threshold[1, 5] Assert Level De-assert Level	 $V_{LVI\_VDDA\_HA}$ $V_{LVI\_VDDA\_HD}$	 4.50 4.50	 4.675 4.675	 4.80 4.80	V

1 Monitors V_{DDA}.
2 Monitors V_{DD33}.
3 Monitors V_{DDSYN}.
4 Disabled when $V_{RCSEL} = V_{SSA}$.

4.9 Oscillators Electrical Characteristics

Table 14. 3.3 V High Frequency External Oscillator

Spec	Characteristic	Symbol	Min	Max	Unit
1	Frequency Range	f_{ref}	4[1]	40	MHz
2	Duty Cycle of reference	t_{DC}	40	60	%
3	EXTAL Input High Voltage External crystal mode[2] External clock mode	V_{IHEXT}	 $V_{XTAL} + 0.4$ $0.65 \times V_{DDSYN}$	 $V_{DDSYN} + 0.3$ $V_{DDSYN} + 0.3$	V
4	EXTAL Input Low Voltage External crystal mode[3] External clock mode	V_{ILEXT}	 $V_{DDSYN} - 0.3$ $V_{DDSYN} - 0.3$	 $V_{XTAL} - 0.4$ $0.35 \times V_{DDSYN}$	V
5	XTAL Current[4]	I_{XTAL}	1	3	mA
6	Total On-chip stray capacitance on XTAL	C_{S_XTAL}	—	3	pF
7	Total On-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	3	pF

Table 22. Pad AC Specifications (5.0 V, 2.5 V)[1] (continued)

Spec	Pad Type[2]	SRC/DSC[3]	Output Delay[4,4] (ns)	Rise/Fall[5,6] (ns)	Load Drive (pF)
2	Medium	00	142/186	65/89	50
			195/253	91/122	200
		01	20/35	8.7/16.6	50
			41/64	24/35	200
		11	12/11	5.3/5.9	50
			32/34	21/23	200
3	Fast[8]	00	2.7	1.5	10
		01			20
		10			30
		11			50
4	Input	N/A	1.9/1.9	1.5/1.5	0.5

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at F_{SYS} = 116 MHz, V_{DD} = 1.08 – 1.32 V, V_{DDE} = 1.62 – 1.98 V, V_{DDEH} = 4.5 – 5.5 V, V_{RC33} and V_{DDPLL} = 3.0 – 3.6 V, $T_A = T_L$ to T_H.

2 Slow = SH or SHA; Medium = MH or MHA; Fast = F; Input = IHA. See Table 2.

3 SRC/DSC are bit fields in the Pad Configuration Registers. SRC—Slew Rate Control (slow and medium pad types only), DSC—Drive Strength Control (fast pad type only).

4 This parameter is supplied for reference and is not guaranteed by design and not tested.

5 This parameter is guaranteed by characterization before qualification rather than 100% tested.

6 Delay and rise/fall are measured to 20% or 80% of the respective signal.

7 Add a maximum of one system clock to the output delay for delay with respect to system clock.

8 Output delay is shown in. Add a maximum of one system clock to the output delay for delay with respect to system clock.

Table 23. De-rated Pad AC Specifications (3.3 V, 3.3 V)[1]

Spec	Pad Type[2]	SRC/DSC[3]	Out Delay[4,5] (ns)	Rise/Fall[6,] (ns)	Load Drive (pF)
1	Slow[7]	00	408/431	188/204	50
			533/592	250/288	200
		01	80/90	38/44	50
			146/167	82/96	200
		11	27/28	15/17	50
			81/92	57/67	200
2	Medium	00	184/240	79/107	50
			253/330	114/153	200
		01	28/47	11.8/21.8	50
			58/88	34/49	200
		11	18/17	7.6/8.9	50
			46/51	30/35	200

4.14.4 Nexus Debug Interface

Table 27. Nexus Debug Port Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time	t_{MCYC}	15.6	—	ns
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid[2]	t_{MDOV}	–0.1	0.25	t_{MCYC}
4	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC}
5	$\overline{\text{EVTO}}$ Pulse Width	t_{EVTOPW}	1		t_{MCYC}
6	TCK Cycle Time[3]	t_{TCYC}	40	—	ns
7	TCK Duty Cycle	t_{TDC}	40	60	%
8	TDI, TMS Data Setup Time	t_{NTDIS}, t_{NTMSS}	8	—	ns
9	TDI, TMS Data Hold Time	t_{NTDIH}, t_{NTMSH}	5	—	ns
10	TCK Low to TDO Data Valid	t_{JOV}	0	25	ns

1 JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DDE} = 3.0 – 5.5 V, T_A = T_L to T_H, and C_L = 30 pF with SRC = 0b11.

2 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

3 The system clock frequency needs to be three times faster than the TCK frequency.

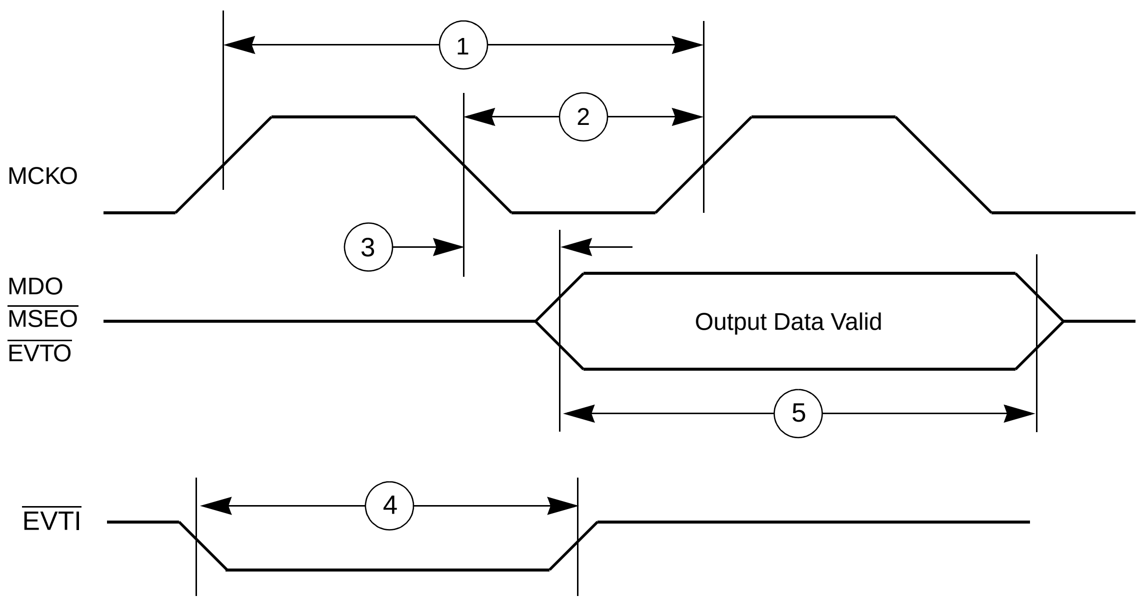


Figure 13. Nexus Output Timing

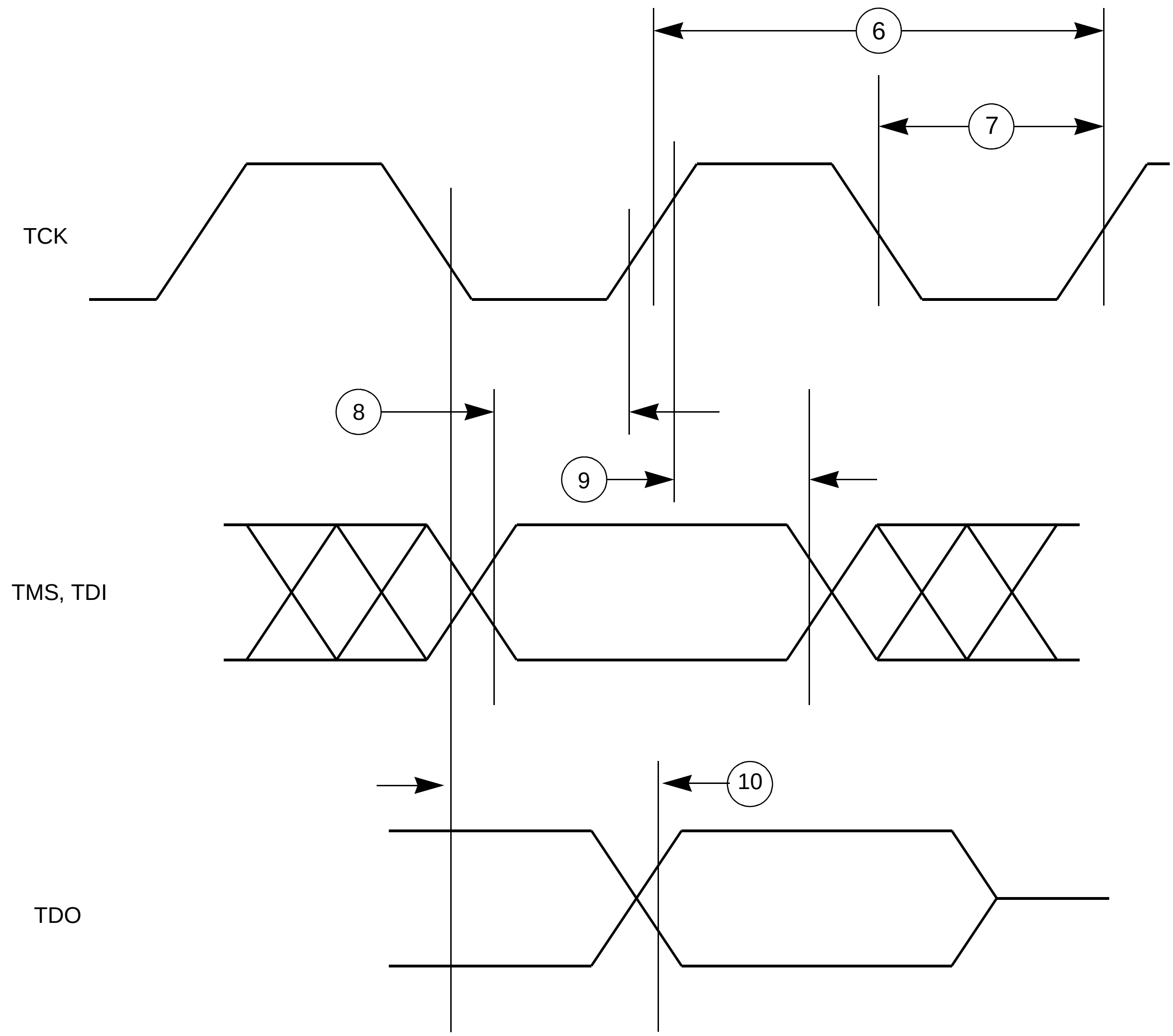


Figure 14. Nexus TDI, TMS, TDO Timing

4.14.5 Enhanced Modular I/O Subsystem (eMIOS)

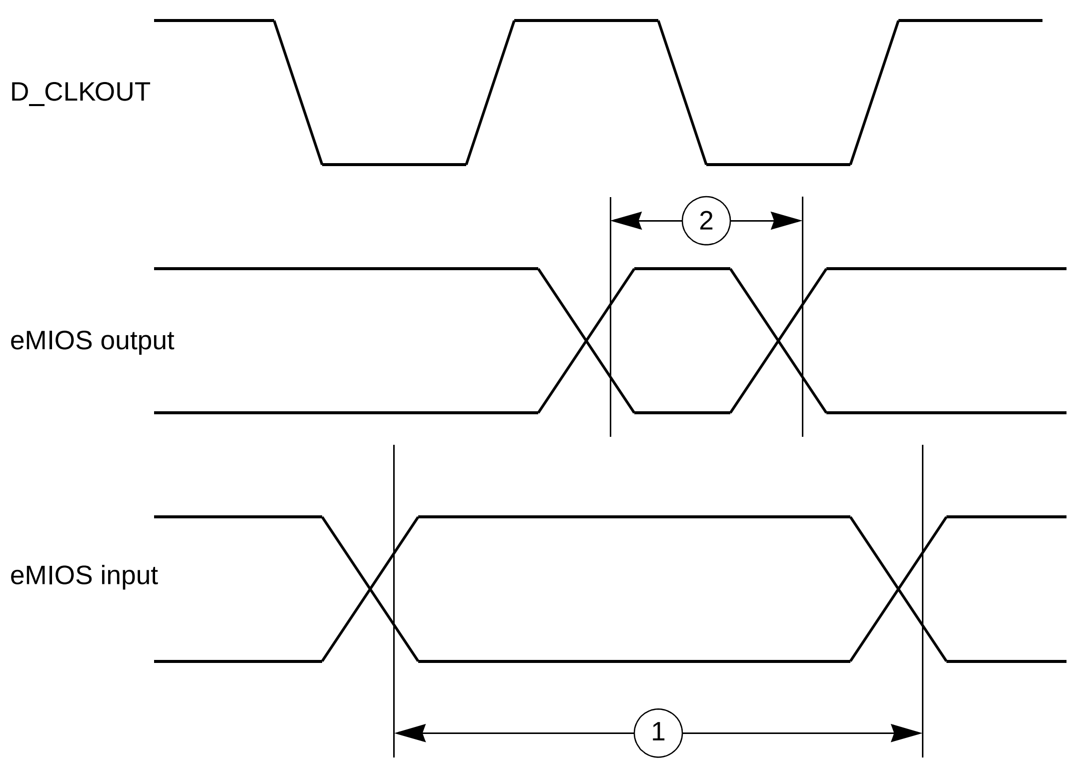
Table 28. eMIOS Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{CYC}
2	eMIOS Output Pulse Width	t_{MOPW}	1[2]	—	t_{CYC}

1 eMIOS timing specified at V_{DDE} = 3.0 – 5.5 V, $T_A = T_L$ to T_H, and CL = 30 pF with SRC = 0b11.

2 This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

Figure 15. eMIOS Timing



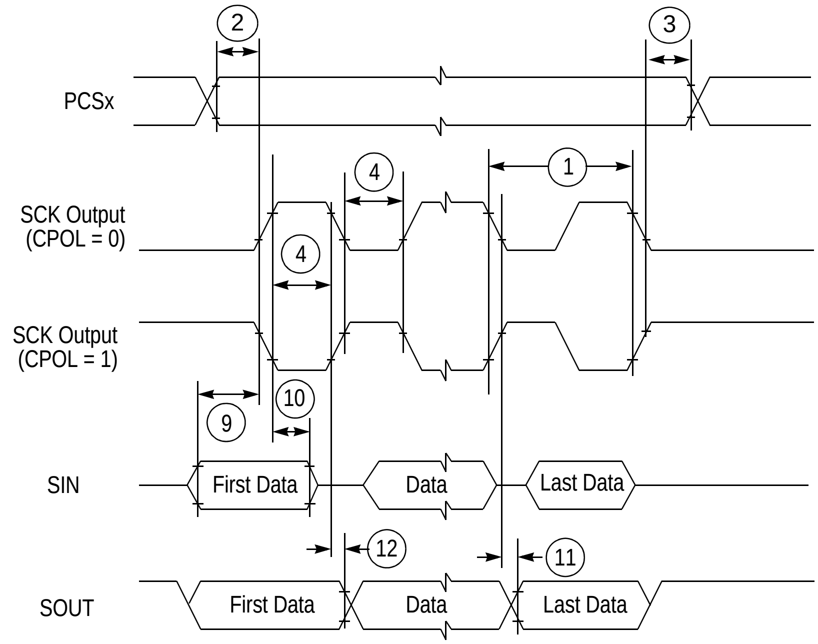


Figure 16. DSPI Classic SPI Timing — Master, CPHA = 0

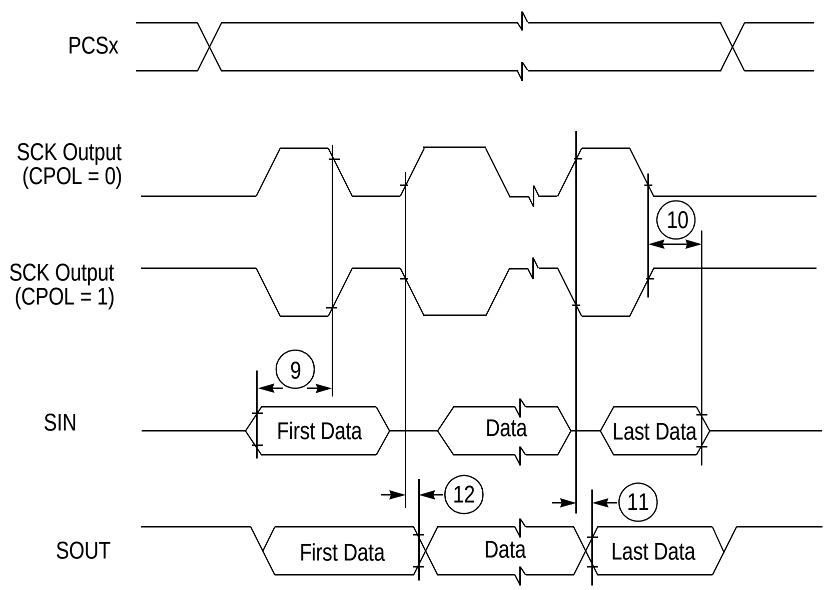


Figure 17. DSPI Classic SPI Timing — Master, CPHA = 1

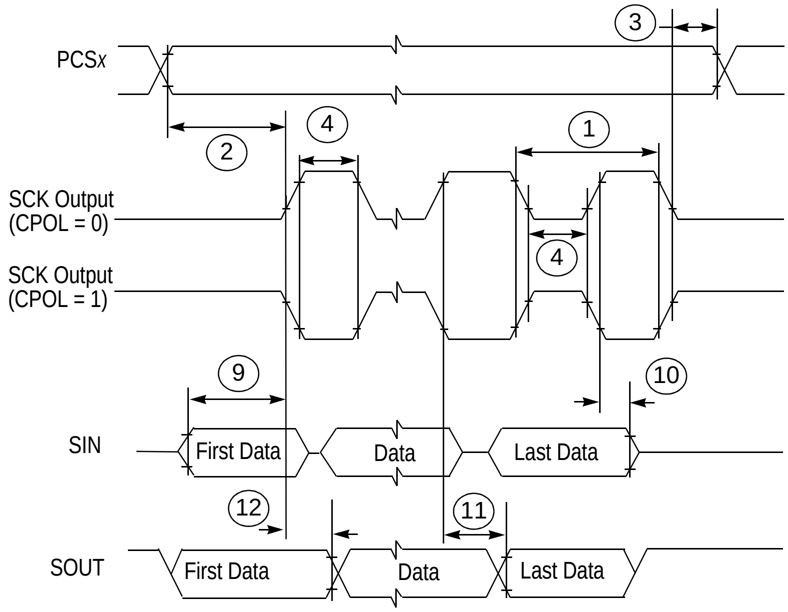


Figure 20. DSPI Modified Transfer Format Timing — Master, CPHA = 0

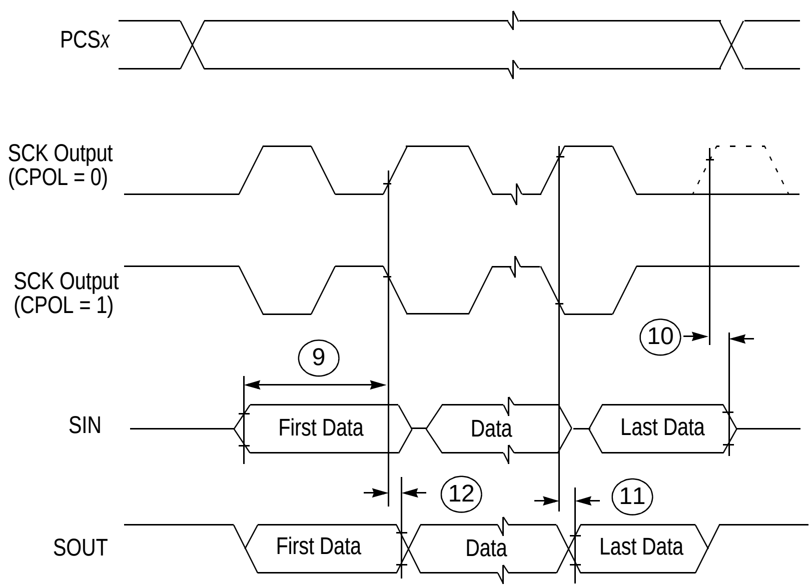


Figure 21. DSPI Modified Transfer Format Timing — Master, CPHA = 1

[1] The Controller can shut off MLBCLK to place MLB in a low-power state.

[2] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (ns p-p).

[3] The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

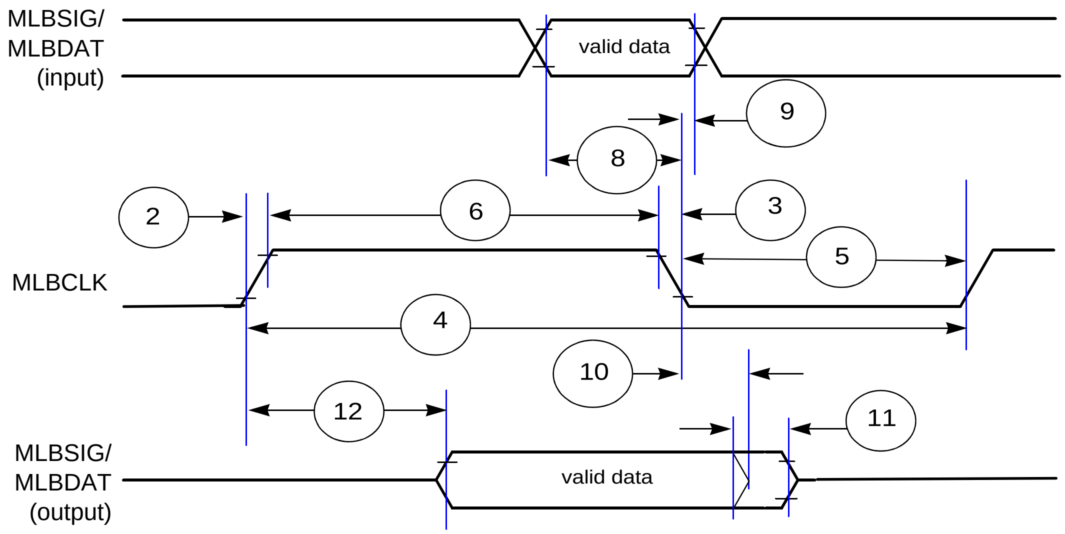


Figure 25. Media Local Bus (MLB) Timing

4.14.8 Fast Ethernet Interface

MII signals use CMOS signal levels compatible with devices operating at either 5.0 V or 3.3 V. Signals are not TTL compatible. They follow the CMOS electrical characteristics.

4.14.8.1 MII Receive Signal Timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the RX_CLK frequency.

Table 33. MII Receive Signal Timing

Spec	Characteristic	Min	Max	Unit
M1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period