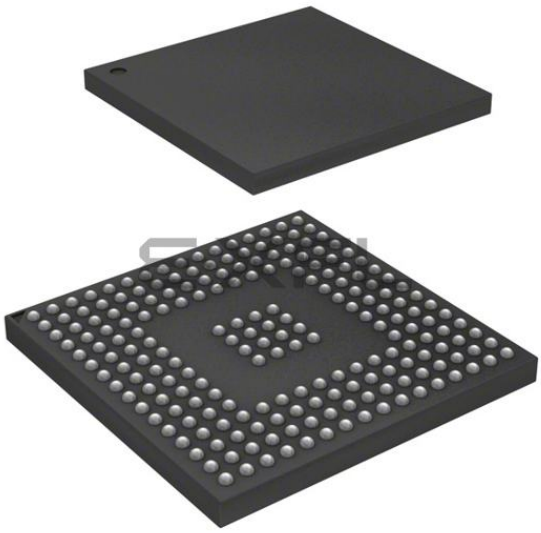

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z650
Core Size	32-Bit Single-Core
Speed	116MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	155
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	592K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 36x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BGA
Supplier Device Package	208-BGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5668gf1avmgr

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Table 1. MPC5668G/MPC5668E Comparison

Feature	MPC5668G		MPC5668E	
Package	**208 MAPBGA**	**256 MAPBGA**	**208 MAPBGA**	**256 MAPBGA**
RAM with ECC	592 KB		128 KB	
MPU	No		16 entry	
DMA	16-channel		32-channel	
Ethernet (FEC)	Yes		No	
MediaLB (MLB-DIM)	Yes		No	
FlexRay	Yes (128 Message Buffers)		No	
ADC (10-bit)	36 internal channels Supports 32 external channels		64 internal channels Supports 32 external channels	
Total Timer I/O (eMIOS200)	24 channels, 16-bit		32 channels, 16-bit	
Cross Trigger Unit (CTU)	No		Yes	
SCI (eSCI)	6		12	
SPI (DSPI)	4		4	
CAN (FlexCAN)	6		5	
I^2C	4		4	
Nexus3 Debug (e200Z6) Nexus2+ Debug (e200Z0)	—	Supported on 256BGA emulation package	—	Supported on 256BGA emulation package

3.3 Pin Muxing and Reset States

Table 2 shows the signals properties for each pin on MPC5668x. For all port pins that have an associated SIU_PCR*n* register to control pin properties, the supported functions column lists the functions associated with the programming of the SIU_PCR*n*[PA] bit in the order: general-purpose input/output (GPIO), function 1, function 2, and function 3 (see Figure 5). When an alternate function is not implemented for a value of SIU_PCR*n*[PA], a dash is shown in the Description column and the respective value in the PA bit field is reserved.

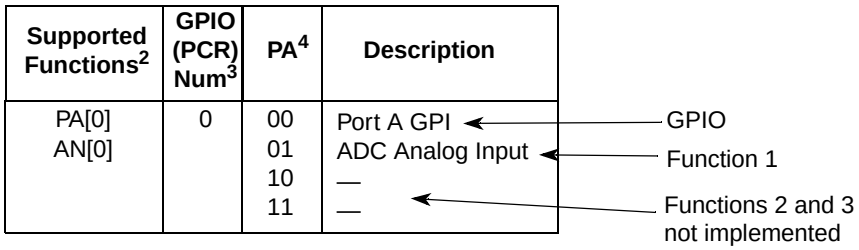


Figure 5. Supported Functions Example

Table 2. MPC5668x Signal Properties

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
Port A (16)											
PA0	PA[0] AN[0]	0	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	D15	D15
PA1	PA[1] AN[1]	1	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	E15	E15
PA2	PA[2] AN[2]	2	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	F16	F16
PA3	PA[3] AN[3]	3	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	F15	F15
PA4	PA[4] AN[4]	4	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	G16	G16
PA5	PA[5] AN[5]	5	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	G15	G15

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PC4	PC[4] AN[36]	36	00 01 10 11	Port C GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	D8	D8
PC5	PC[5] AN[37] Z6NMI	37	00 01 10 11	Port C GPIO ADC Analog Input Z6 Core Non-Maskable Interrupt —	I/O I I —	V_{DDE1}	SHA	—	—	C6	C6
PC6	PC[6] AN[38] Z0NMI	38	00 01 10 11	Port C GPIO ADC Analog Input Z0 Core Non-Maskable Interrupt —	I/O I I —	V_{DDE1}	SHA	—	—	C7	C7
PC7	PC[7] AN[39] FR_DBG3	39	00 01 10 11	Port C GPIO ADC Analog Input FlexRay Debug —	I/O I O —	V_{DDE1}	SHA	—	—	A6	A6
PC8	PC[8] AN[40] FR_DBG2	40	00 01 10 11	Port C GPIO ADC Analog Input FlexRay Debug —	I/O I O —	V_{DDE1}	SHA	—	—	B6	B6
PC9	PC[9] AN[41] FR_DBG1	41	00 01 10 11	Port C GPIO ADC Analog Input FlexRay Debug —	I/O I O —	V_{DDE1}	SHA	—	—	A5	A5
PC10	PC[10] AN[42] FR_DBG0	42	00 01 10 11	Port C GPIO ADC Analog Input FlexRay Debug —	I/O I O —	V_{DDE1}	SHA	—	—	B5	B5
PC11	PC[11] AN[43] SCL_C —	43	00 01 10 11	Port C GPIO ADC Analog Input I^2C_C Serial Clock —	I/O I I/O —	V_{DDE1}	SHA	—	—	B4	B4
PC12	PC[12] AN[44] SDA_C —	44	00 01 10 11	Port C GPIO ADC Analog Input I^2C_C Serial Data —	I/O I I/O —	V_{DDE1}	SHA	—	—	A4	A4
PC13	PC[13] AN[45] — MA[0]	45	00 01 10 11	Port C GPIO ADC Analog Input — ADC Ext. Mux Address Select	I/O I — O	V_{DDE1}	SHA	—	—	C5	C5
PC14	PC[14] AN[46] MA[1] —	46	00 01 10 11	Port C GPIO ADC Analog Input ADC Ext. Mux Address Select —	I/O I — O	V_{DDE1}	SHA	—	—	C4	C4

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PD9	PD[9] CNRX_E RXD_L SDA_C	57	00 01 10 11	Port D GPIO FlexCAN_E Receive SCI_L Receive I^2C_C Serial Data	I/O I I I/O	V_{DDE2}	SH	—	—	F1	F1
PD10	PD[10] CNTX_F TXD_M SCL_D	58	00 01 10 11	Port D GPIO FlexCAN_F Transmit SCI_M Transmit I^2C_D Serial Clock	I/O O O I/O	V_{DDE2}	SH	—	—	F2	F2
PD11	PD[11] CNRX_F RXD_M SDA_D	59	00 01 10 11	Port D GPIO FlexCAN_F Receive SCI_M Receive I^2C_D Serial Data	I/O I I I/O	V_{DDE2}	SH	—	—	G1	G1
PD12	PD[12] TXD_A	60	00 01 10 11	Port D GPIO eSCI_A Transmit — —	I/O O — —	V_{DDE2}	SH	—	—	G2	G2
PD13	PD[13] RXD_A	61	00 01 10 11	Port D GPIO eSCI_A Receive — —	I/O I — —	V_{DDE2}	SH	—	—	H1	H1
PD14	PD[14] TXD_B	62	00 01 10 11	Port D GPIO eSCI_B Transmit — —	I/O O — —	V_{DDE2}	SH	—	—	C3	C3
PD15	PD[15] RXD_B	63	00 01 10 11	Port D GPIO eSCI_B Receive — —	I/O I — —	V_{DDE2}	SH	—	—	D3	D3
Port E (16)											
PE0	PE[0] TXD_C eMIOS[31]	64	00 01 10 11	Port E GPIO eSCI_C Transmit eMIOS Channel —	I/O O I/O —	V_{DDE2}	SH	—	—	E3	E3
PE1	PE[1] RXD_C eMIOS[30]	65	00 01 10 11	Port E GPIO eSCI_C Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	E4	E4
PE2	PE[2] TXD_D eMIOS[29]	66	00 01 10 11	Port E GPIO eSCI_D Transmit eMIOS Channel —	I/O O I/O	V_{DDE2}	SH	—	—	F4	F4

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PE14	PE[14] SCL_A PCS_D[2]	78	00 01 10 11	Port E GPIO I^2C_A Serial Clock DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE2}	SH	—	—	N7	N7
PE15	PE[15] SDA_A PCS_D[5]	79	00 01 10 11	Port E GPIO I^2C_A Serial Data DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE2}	SH	—	—	N6	N6
Port F (16)											
PF0	PF[0] SCK_A	80	00 01 10 11	Port F GPIO DSPI_A Serial Clock — —	I/O I/O — —	V_{DDE2}	MH	—	—	H2	H2
PF1	PF[1] SOUT_A	81	00 01 10 11	Port F GPIO DSPI_A Serial Data Out — —	I/O O — —	V_{DDE2}	MH	—	—	J1	J1
PF2	PF[2] SIN_A	82	00 01 10 11	Port F GPIO DSPI_A Serial Data In — —	I/O I — —	V_{DDE2}	SH	—	—	J2	J2
PF3	PF[3] PCS_A[0] PCS_B[5] PCS_C[4]	83	00 01 10 11	Port F GPIO DSPI_A Peripheral Chip Select DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I/O O O	V_{DDE2}	SH	—	—	N2	N2
PF4	PF[4] SCK_B PCS_A[1] PCS_C[2]	84	00 01 10 11	Port F GPIO DSPI_B Serial Clock DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I/O O O	V_{DDE2}	MH	—	—	M1	M1
PF5	PF[5] SOUT_B PCS_A[2] PCS_C[3]	85	00 01 10 11	Port F GPIO DSPI_B Serial Data Out DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	P2	P2
PF6	PF[6] SIN_B PCS_A[3] PCS_C[5]	86	00 01 10 11	Port F GPIO DSPI_B Serial Data In DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I O O	V_{DDE2}	SH	—	—	N1	N1
PF7	PF[7] PCS_B[0] PCS_C[5] PCS_D[4]	87	00 01 10 11	Port F GPIO DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE2}	SH	—	—	R2	R2

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PG2	PG[2] PCS_D[1] SCL_C AN[50]	98	00 01 10 11	Port G GPIO DSPI_D Peripheral Chip Select I^2C_C Serial Clock ADC Analog Input	I/O O I/O I	V_{DDE3}	SHA	—	—	H14	H14
PG3	PG[3] PCS_D[2] SDA_C AN[51]	99	00 01 10 11	Port G GPIO DSPI_D Peripheral Chip Select I^2C_C Serial Data ADC Analog Input	I/O O I/O I	V_{DDE3}	SHA	—	—	J14	J14
PG4	PG[4] PCS_D[3] SCL_B AN[52]	100	00 01 10 11	Port G GPIO DSPI_D Peripheral Chip Select I^2C_B Serial Clock ADC Analog Input	I/O O I/O I	V_{DDE3}	SHA	—	—	K14	K14
PG5	PG[5] PCS_D[4] SDA_B AN[53]	101	00 01 10 11	Port G GPIO DSPI_D Peripheral Chip Select I^2C_B Serial Data ADC Analog Input	I/O O I/O I	V_{DDE3}	SHA	—	—	L14	L14
PG6	PG[6] PCS_C[1] FEC_MDC AN[54]	102	00 01 10 11	Port G GPIO DSPI_C Peripheral Chip Select Ethernet Mgmt. Data Clock ADC Analog Input	I/O O O I	V_{DDE3}	MHA	—	—	H15	H15
PG7	PG[7] PCS_C[2] FEC_MDIO AN[55]	103	00 01 10 11	Port G GPIO DSPI_C Peripheral Chip Select Ethernet Mgmt. Data I/O ADC Analog Input	I/O O I/O I	V_{DDE3}	MHA	—	—	J15	J15
PG8	PG[8] eMIOS[7] FEC_TX_CLK AN[56]	104	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Clock ADC Analog Input	I/O I/O I I	V_{DDE3}	SHA	—	—	K15	K15
PG9	PG[9] eMIOS[6] FEC_CRS AN[57]	105	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Carrier Sense ADC Analog Input	I/O I/O I I	V_{DDE3}	SHA	—	—	L15	L15
PG10	PG[10] eMIOS[5] FEC_TX_ER AN[58]	106	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Error ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	M15	M15
PG11	PG[11] eMIOS[4] FEC_RX_CLK AN[59]	107	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Receive Clock ADC Analog Input	I/O I/O I I	V_{DDE3}	SHA	—	—	J16	J16
PG12	PG[12] eMIOS[3] FEC_TXD[0] AN[60]	108	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	K16	K16

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PH7	PH[7] eMIOS[24] FEC_RXD[3]	119	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	T15	T15
PH8	PH[8] eMIOS[23]	120	00 01 10 11	Port H GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	P7	P7
PH9	PH[9] eMIOS[22]	121	00 01 10 11	Port H GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	N8	N8
PH10	PH[10] eMIOS[21]	122	00 01 10 11	Port H GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	P8	P8
PH11	PH[11] eMIOS[20]	123	00 01 10 11	Port H GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	N9	N9
PH12	PH[12] eMIOS[19]	124	00 01 10 11	Port H GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	P9	P9
PH13	PH[13] eMIOS[18]	125	00 01 10 11	Port H GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	P10	P10
PH14	PH[14] eMIOS[17]	126	00 01 10 11	Port H GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	P11	P11
PH15	PH[15] eMIOS[16]	127	00 01 10 11	Port H GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	N11	N11
Port J (16)											
PJ0	PJ[0] eMIOS[15] PCS_A[4]	128	00 01 10 11	Port J GPIO eMIOS Channel DSPI_A Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	R7	R7

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PJ1	PJ[1] eMIOS[14] PCS_A[5]	129	00 01 10 11	Port J GPIO eMIOS Channel DSPI_A Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T7	T7
PJ2	PJ[2] eMIOS[13] PCS_B[1]	130	00 01 10 11	Port J GPIO eMIOS Channel DSPI_B Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	R8	R8
PJ3	PJ[3] eMIOS[12] PCS_B[2]	131	00 01 10 11	Port J GPIO eMIOS Channel DSPI_B Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T8	T8
PJ4	PJ[4] eMIOS[11] PCS_C[3]	132	00 01 10 11	Port J GPIO eMIOS Channel DSPI_C Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	R9	R9
PJ5	PJ[5] eMIOS[10] PCS_C[4]	133	00 01 10 11	Port J GPIO eMIOS Channel DSPI_C Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T9	T9
PJ6	PJ[6] eMIOS[09] PCS_D[5]	134	00 01 10 11	Port J GPIO eMIOS Channel DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	R10	R10
PJ7	PJ[7] eMIOS[08] PCS_D[1]	135	00 01 10 11	Port J GPIO eMIOS Channel DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T10	T10
PJ8	PJ[8] eMIOS[07]	136	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	T11	T11
PJ9	PJ[9] eMIOS[06]	137	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	R11	R11
PJ10	PJ[10] eMIOS[05]	138	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	N12	N12
PJ11	PJ[11] eMIOS[04]	139	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	P12	P12

4 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5668x.

4.1 Maximum Ratings

Table 4. Absolute Maximum Ratings[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	1.2 V Core Supply Voltage[2]	V_{DD}	–0.3	1.32[3]	V
2	3.3 V Clock Synthesizer Voltage[2, 4]	V_{DDSYN}	–0.3	3.6	V
3	3.3 V I/O Buffer Voltage [2, 4]	V_{DD33}	–0.3	3.6	V
4	3.3–5.0 V Voltage Regulator Control Voltage [2, 5, 6]	V_{RC}	–0.3	5.5	V
5	3.3–5.0 V Analog Supply Voltage (reference to V_{SSA}) [2, 5]	V_{DDA}	–0.3	5.5	V
6	3.3–5.0 V External I/O Supply Voltage [2, 5, 7]	V_{DDE1}[8] V_{DDE2}[8] V_{DDE3}[8] V_{DDE4}[8]	–0.3 –0.3 –0.3 –0.3	5.5 5.5 5.5 5.5	V
7	2.5–3.3 V External I/O Supply Voltage (MLB) [2, 4]	V_{DDEMLB}[8]	–0.3	3.6	V
8	3.3 V External I/O Supply Voltage (Nexus) [2, 4]	V_{DDENEX}[8]	–0.3	3.6	V
9	DC Input Voltage[9] V_{DDE1}, V_{DDE2}, V_{DDE3}, V_{DDE4} V_{DDEMLB}, V_{DDENEX}	V_{IN}	 –1.0[10] –1.0[9]	 V_{DDEx} + 0.3 V[11] V_{DDEx} + 0.3 V[10]	V
10	Analog Reference High Voltage	V_{RH}	–0.3	Minimum of 5.5 or V_{DDA} + 0.3	V
11	Analog Reference Low Voltage	V_{RL}	–0.3	5.5	V
12	V_{SS} to V_{SSA} Differential Voltage	$V_{SS} – V_{SSA}$	–100	100	mV
13	V_{SS} to V_{SSSYN} Differential Voltage	$V_{SS} – V_{SSSYN}$	–100	100	mV
14	Maximum DC Digital Input Current[12] (per pin, applies to all digital F, MH, SH, and IH pins)	I_{MAXD}	–2	2	mA
15	Maximum DC Analog Input Current[13] (per pin, applies to all analog AE and A pins)	I_{MAXA}	–3	3	mA
16	Storage Temperature Range	T_{STG}	–55.0	150.0	°C
17	Maximum Solder Temperature[14]	T_{SDR}	—	235.0	°C
18	Moisture Sensitivity Level[15]	MSL	—	3	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

3 2.0 V for 10 hours cumulative time, 1.2 V +10% for time remaining.

4 5.3 V for 10 hours cumulative time, 3.3 V +10% for time remaining.

5 6.4 V for 10 hours cumulative time, 5.0 V +10% for time remaining.

6 VRC cannot be 100mV higher than VDDA. VDDSYN and VDD33 cannot be 100mV higher than VRC.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The supplied thermal resistances are provided based on JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined on the single-layer (1s) board and on the four-layer board with two signal layers and a power and a ground plane (2s2p) clearly demonstrate that the effective thermal resistance of the component is not a constant. It depends on the construction of the application board (number of planes), the effective size of the board which cools the component, how well the component is thermally and electrically connected to the planes, and the power being dissipated by adjacent components.

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between through vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the application board has one oz. (35 micron nominal thickness) internal planes, the components are well separated, and the overall power dissipation on the board is less than 0.02 W/cm^2.

The thermal performance of any component depends strongly on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D) \quad \textit{Eqn. 2}$$

where:

T_J = junction temperature (^oC)

T_B = board temperature at the package perimeter ($^oC/W$)

$R_{\theta JB}$ = junction to board thermal resistance ($^oC/W$) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition, with the component soldered to a board with internal planes.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 3}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for either hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 4}$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

Table 8. DC Electrical Specifications

Spec	Characteristic	Symbol	Min	Max	Unit
6	3.3–5.0 V External I/O Supply Voltage[2] V_{DDE1} V_{DDE2} V_{DDE3} V_{DDE4}		 3.0 3.0 3.0 3.0	 5.5 5.5 5.5 5.5	V
7	2.5 V – 3.3 V External I/O Supply Voltage (MLB)	V_{DDEMLB}[3]	2.375	3.6	V
8	3.3 V External I/O Supply Voltage (Nexus)	V_{DDENEX}	3.0	3.6	V
9	Pad Input High Voltage Hysteresis enabled Hysteresis disabled (IHA/SH/SHA/MH/MHA)[4, 5] Hysteresis disabled (F)	V_{IH}	 0.65 × V_{DDE} 0.55 × V_{DDE} 0.55 × V_{DDE}	V_{DDE} + 0.3	V
10	Pad Input Low Voltage Hysteresis enabled Hysteresis disabled (IHA/SH/SHA/MH/MHA)[4, 5] Hysteresis disabled (F)	V_{IL}	V_{SS} – 0.3	 0.35 × V_{DDE} 0.40 × V_{DDE} 0.40 × V_{DDE}	V
11	Pad Input Hysteresis	V_{HYS}	0.1 × V_{DDE}		V
12	Analog (IHA) Input Voltage	V_{INDC}	V_{SSA} – 0.3	V_{DDA} + 0.3	V
13	Pad Output High Voltage[6, 7, 8]	V_{OH}	0.8 × V_{DDE}	—	V
14	Pad Output Low Voltage[8]	V_{OL}	—	0.2 × V_{DDE}	V
15	Input Capacitance (Digital Pins: Pad type F, MH, SH)[4]	C_{IN}	—	7	pF
16	Input Capacitance (Analog Pins: Pad type IHA)[4, 5]	C_{IN_A}	—	10	pF
17	Input Capacitance (Shared digital/analog pins: MHA, SHA)[4]	C_{IN_M}	—	12	pF
18	I/O Weak Pull Up/Down Absolute Current[4, 9] Pad F: 2.375 V – 3.6 V Pad SH/MH/IHA: 3.0 V – 3.6 V Pad SH/MH/IHA: 4.5 V – 5.5 V	I_{ACT}	 25 10 35	 180 95 200	µA
19	I/O Input Leakage Current[10]	I_{INACT_D}	–2.5	2.5	µA
20	DC Injection Current (per pin)	I_{IC}	–1.0	1.0	mA
21	Analog Input Current, Channel Off[11] (Analog pins IHA)[4, 5]	I_{INACT_A}	–150	150	nA
22	Analog Reference High Voltage	V_{RH}	V_{DDA} – 500	V_{DDA}	mV
23	Analog Reference Low Voltage	V_{RL}	V_{SSA}	V_{SSA} + 500	mV
24	V_{SS} to V_{SSA} Differential Voltage	$V_{SS} – V_{SSA}$	–100	100	mV
25	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} – V_{SS}$	–100	100	mV
26	Slew rate on V_{DDA}, V_{DDEx}, V_{DDSYN}, V_{DD33}, and V_{RC} power supply pins	V_{Ramp}	—	100	V/ms
27	Capacitive Supply Load (V_{DD})	V_{Load}	8	—	µF
28	Capacitive Supply Load (V_{DD33}, V_{DDSYN})	V_{Load}	1	—	µF

1 When V_{RCSEL} = V_{SSA} (low), V_{DDSYN} and V_{DD33} are externally supplied. When V_{RCSEL} = V_{DDA} (high), V_{DDSYN} and V_{DD33} are generated by internal voltage regulators. When V_{RCSEL} = V_{SSA} (low), V_{DDSYN} and V_{DD33} cannot be 100 mV higher than V_{RC}.

2 $V_{DDE1} – V_{DDE4}$ are separate power segments and may be powered independently with no differential voltage constraints between the power segments. $V_{DDE1} – V_{DDE3}$ pad power segments contain ADC analog input channels and thus the input analog signal level may be clamped to the V_{DDE} level, resulting in inaccurate ADC results if the V_{DDE} voltage level is less than V_{DDA}.

3 When $V_{RCSEL} = V_{DDA}$ (high), the internally generated V_{DD33} voltage may be used to power V_{DDEMLB} as long as the PK[0:2] pads remain in the disabled default state with their output buffers, input buffers, and pull devices disabled.

4 The pad type is indicated by one or more of the following abbreviations: A–analog, F—fast speed, H–high voltage, I—input-only, M–medium speed, S–slow speed. For example, pad type SH designates a slow high-voltage pad.

5 The IHA pads are related to V_{DDA}.

6 Characterization Based Capability:
IOH_F = {12, 20, 30, 40} mA and IOL_F = {24, 40, 50, 65} mA for {00, 01,10, 11} drive mode with V_{DDE} = 3.0 V;
IOH_F = {7, 13, 18, 25} mA and IOL_F = {18, 30, 35, 50} mA for {00, 01, 10, 11} drive mode with V_{DDE} = 2.25 V;
IOH_F = {3, 7, 10, 15} mA and IOL_F = {12, 20, 27, 35} mA for {00, 01, 10, 11} drive mode with V_{DDE} = 1.62 V.

7 Characterization Based Capability:
IOH_S = {6, 11.6} mA and IOL_S = {9.2, 17.7} mA for {slow, medium} I/O with V_{DDEH} = 4.5 V;
IOH_S = {2.8, 5.4} mA and IOL_S = {4.2, 8.1} mA for {slow, medium} I/O with V_{DDEH} = 3.0 V

8 All V_{OL}/V_{OH} values 100% tested with ±2 mA load.

9 Absolute value of current, measured at V_{IL} and V_{IH}.

10 Weak pull up/down inactive. Measured at V_{DDE} = 5.25 V. Applies to pad types: SH and MH. Leakage specification guaranteed only when power supplies are within specified operating conditions.

11 Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to pad types: pad_a and pad_ae.

4.6 Operating Current Specifications

Table 9. Operating Currents

Spec	Characteristic	Symbol	Typ[1] 25 °C Ambient	Max[1] –40–150 °C Junction	Unit
Equations	$I_{TOTAL} = I_{DDE} + I_{DDA} + I_{RH} + I_{DD33} + I_{DDSYN} + I_{RC} + I_{DD}$ $I_{DDE} = I_{DDE1} + I_{DDE2} + I_{DDE3} + I_{DDE4} + I_{DDEMLB}$	—	—	—	—
1	V_{DDE} Current $V_{DDE(1,2,3,4)}$ @ 3.0 V – 5.5 V V_{DDEMLB} @ 2.375 V – 3.6 V Static[2] Dynamic[3]	I_{DDE}	 0 Note 3	 30 25	 µA mA
2	V_{DDA} Current V_{DDA} @ 3.0 V – 5.5 V Run mode Sleep mode – Optional 32 kHz osc enabled	I_{DDA}	 1 20 +5	 30 50 +15	 mA µA µA
3	V_{RH} Current V_{RH} @ 3.0 V – 5.5 V Run mode Sleep mode	I_{RH}	 300 1	 700 30	 µA µA
4	V_{DD33} Current V_{DD33} @ 3.0 V – 3.6 V Run mode Sleep mode	I_{DD33}	 10 10	 20 20	 mA µA

Table 14. 3.3 V High Frequency External Oscillator (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
8	Crystal manufacturer's recommended capacitive load	C_L	See crystal specification	See crystal specification	pF
9	Discrete load capacitance to be connected to EXTAL	C_{L_EXTAL}	—	$2\times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$[5]	pF
10	Discrete load capacitance to be connected to XTAL	C_{L_XTAL}	—	$2\times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$[5]	pF
11	Startup Time	$t_{startup}$	—	10	ms

1 When PLL frequency modulation is active, reference frequencies less than 8 MHz will distort the modulated waveform and the effects of this on emissions is not characterized.

2 This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case, $V_{extal} - V_{xtal} \geq 400$ mV criteria has to be met for oscillator's comparator to produce output clock.

3 This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case, $V_{xtal} - V_{extal} \geq 400$ mV criteria has to be met for oscillator's comparator to produce output clock.

4 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

5 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

Table 15. 5 V Low Frequency (32 kHz) External Oscillator

Spec	Characteristic	Symbol	Min	Max	Unit
1	Frequency Range	f_{ref32}	32	40	kHz
2	Duty Cycle of reference	t_{dc32}	40	60	%
3	XTAL32 Current[1]	I_{XTAL32}	—	3	µA
4	Crystal manufacturer's recommended capacitive load	C_{L32}	See crystal specification	See crystal specification	pF
5	Startup Time	$t_{Startup}$	—	2	s

1 I_{xtal32} is the oscillator bias current out of the XTAL32 pin with both EXTAL32 and XTAL32 pins grounded.

Table 16. 5 V High Frequency (16 MHz) Internal RC Oscillator

Spec	Characteristic	Symbol	Range	Min	Typ	Max	Unit
1	Frequency before trim[1]	f_{ut}	35%	10.4	16	21.6	MHz
2	Frequency after loading factory trim[2]	f_t	7%	14.9	16	17.1	MHz
3	Application trim resolution[3]	t_s	—	—	—	±0.5	%
4	Application frequency trim step[3]	f_s	—	—	300	—	kHz
5	Startup Time	$t_{Startup}$	—	—	—	500	ns

1 Across process, voltage, and temperature.

2 Across voltage and temperature.

3 Fixed voltage and temperature.

Table 17. 5V Low Frequency (128 kHz) Internal RC Oscillator

Spec	Characteristic	Symbol	Range	Min	Typ	Max	Unit
1	Frequency before trim[1]	F_{ut128}	35%	83.2	128	172.8	kHz
2	Frequency after loading factory trim[2]	F_{t128}	7%	119.0	128	137.0	kHz
3	Application trim resolution[3]	T_{s128}	—	—	—	±2	%
4	Application frequency trim step[3]	F_{s128}	—	—	4	—	kHz
5	Startup Time	S_{t128}	—	—	—	100	µs

1 Across process, voltage, and temperature.

2 Across voltage and temperature.

3 Fixed voltage and temperature.

4.10 FMPLL Electrical Characteristics

Table 18. FMPLL Electrical Specifications[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	System Frequency[2]	f_{SYS}	—	116	MHz
2	PLL Reference Frequency Range	f_{REF}	4	40	MHz
3	PLL Frequency	f_{PLL}	$\frac{f_{vco(min)}}{(ERFD+1)}$		MHz
4	Loss of Reference Frequency [3]	f_{LOR}	100	2000	kHz
5	Self Clocked Mode Frequency	f_{SCM}	16	64	MHz
6	PLL Lock Time[4]	t_{LPLL}	—	400	µs
7	Duty Cycle of Reference	t_{DC}	40	60	%
8	Frequency un-LOCK Range	f_{UL}	–4.0	4.0	% f_{SYS}
9	Frequency LOCK Range	f_{LCK}	–2.0	2.0	% f_{SYS}
10	CLKOUT Period Jitter,[5] Measured at f_{SYS} Max Cycle-to-cycle Jitter	C_{Jitter}	–5	5	%f_{SYS}
11	CLKOUT Jitter at ≥ 50 µs period	C_{Jitter}	–250	250	ns
12	Peak-to-Peak Frequency Modulation Range Limit [6,7] (f_{SYS}Max must not be exceeded)	C_{mod}	0	4	%f_{SYS}
13	FM Depth Tolerance[8]	C_{mod_err}	–0.50	0.50	%f_{SYS}
14	VCO Frequency[9]	f_{VCO}	192	600	MHz
15	Modulation Rate Limits[10]	f_{MOD}	0.400	1	MHz

1 V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H.

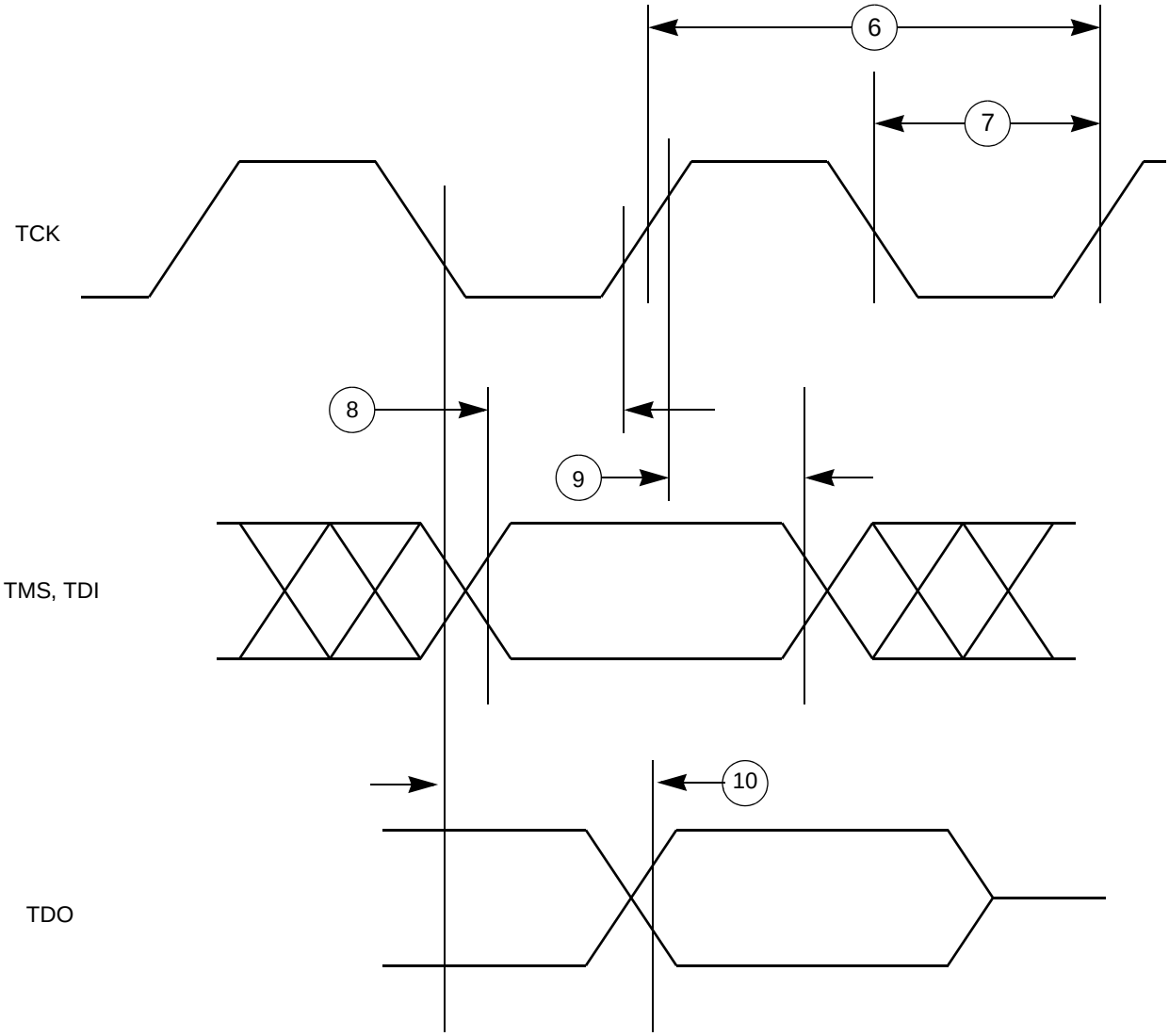


Figure 14. Nexus TDI, TMS, TDO Timing

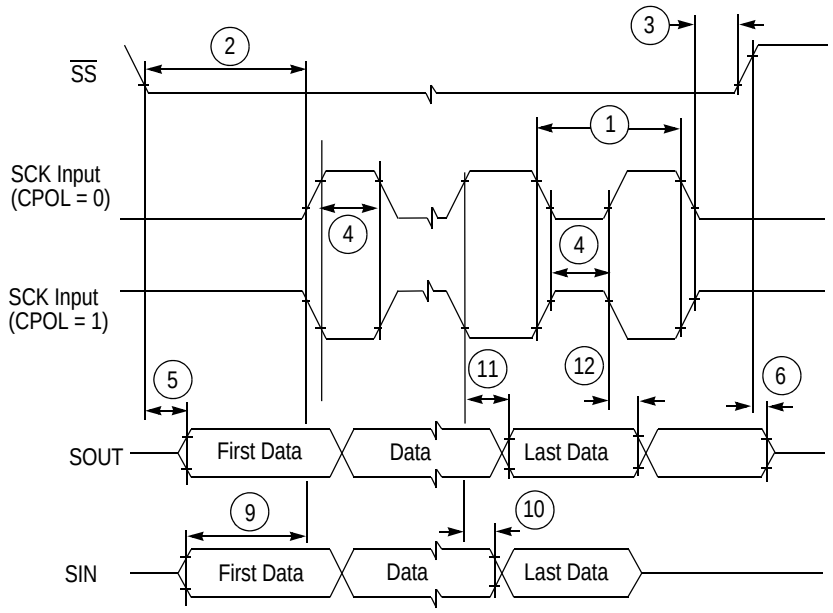


Figure 22. DSPI Modified Transfer Format Timing — Slave, CPHA = 0

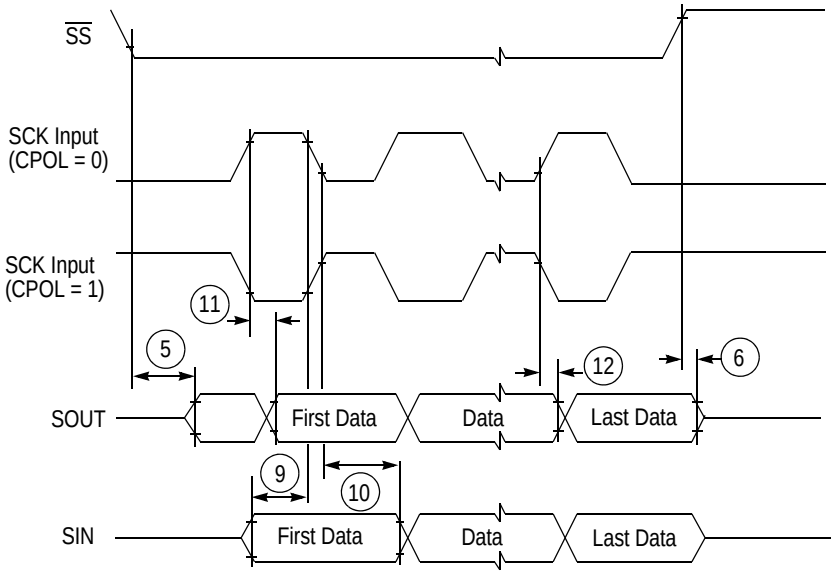


Figure 23. DSPI Modified Transfer Format Timing — Slave, CPHA = 1

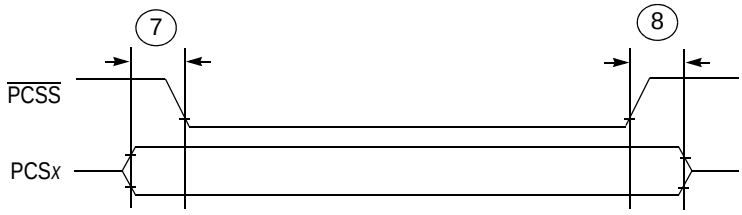


Figure 24. DSPI PCS Strobe ($\overline{\text{PCSS}}$) Timing

4.14.7 MLB Interface

4.14.7.1 Media Local Bus DC Electrical Characteristics

Table 30 provides the DC electrical characteristics for the Media Local Bus interface.

Table 30. Media Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Maximum Input Voltage	—	—	—	3.6	V	
Low Level Input Threshold	V_{IL}	—	—	0.7	V	
High Level Input Threshold	V_{IH}	1.8[1]	—	—	V	
Low Level Output Threshold	V_{OL}	—	—	0.4	V	I_{OL} = 6 mA
High Level Output Threshold	V_{OH}	2.0	—	—	V	I_{OH} = –6 mA
Input Leakage Current	I_L	—	—	±1	µA	$0 < V_{in} < V_{DDE4}$

1 Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

4.14.7.2 Media Local Bus (MLB) AC Electrical Characteristics

Table 31 and Table 32 provide the AC electrical characteristics for the Media Local Bus interface.

Table 31. MLB Timing for MLB Speed 256 Fs or 512 Fs

Spec	Parameter	Symbol	Min	Typ	Max	Unit	Comments
1	MLBCLK Operating Frequency[1]	f_{mck}	11.264 — — —	— 12.288 24.576 —	— — — 24.6272 25.600	MHz	256 Fs at 44.0 kHz 256 Fs at 48.0 kHz 512 Fs at 48.0 kHz 512 Fs at 48.1 kHz 512 Fs PLL unlocked
2	MLBCLK rise time	t_{mckr}	—	—	3	ns	V_{IL} to V_{IH}
3	MLBCLK fall time	t_{mckf}	—	—	3	ns	V_{IH} to V_{IL}
4	MLBCLK cycle time	t_{mckc}	—	81 40	—	ns	256 Fs 512 Fs
5	MLBCLK low time	t_{mckl}	31.5 30	37 35.5	—	ns	256 Fs 256 Fs PLL unlocked
			14.5 14	17 16.5	—	ns	512 Fs 512 Fs PLL unlocked
6	MLBCLK high time	t_{mckh}	31.5 30	38 36.5	—	ns	256xFs 256 Fs PLL unlocked
			14.5 14	17 16.5	—	ns	512 Fs 512 Fs PLL unlocked
7	MLBCLK pulse width variation[2]	t_{mpwv}	—	—	2	ns p-p	
8	MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	1	—	—	ns	
9	MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	0	—	—	ns	

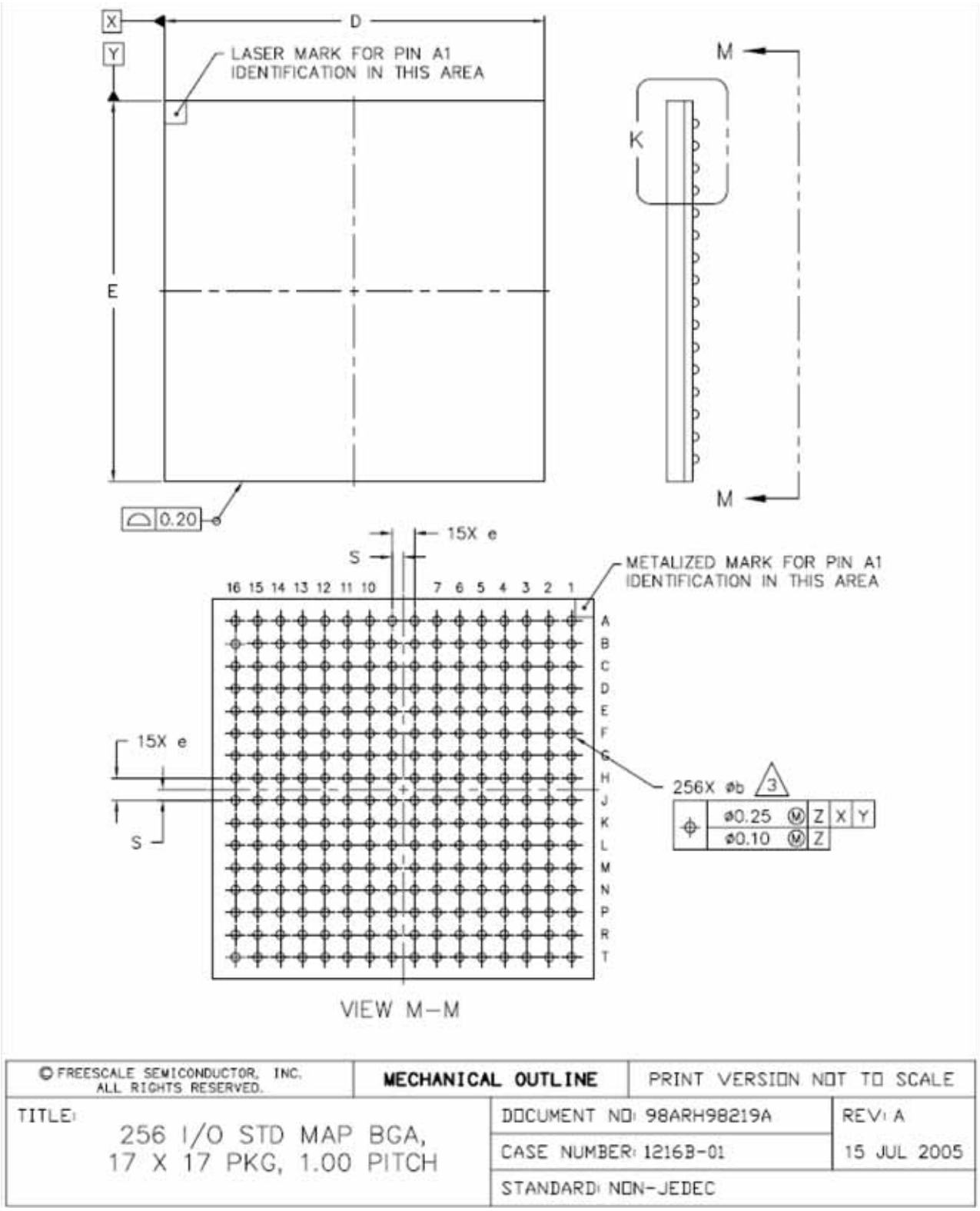
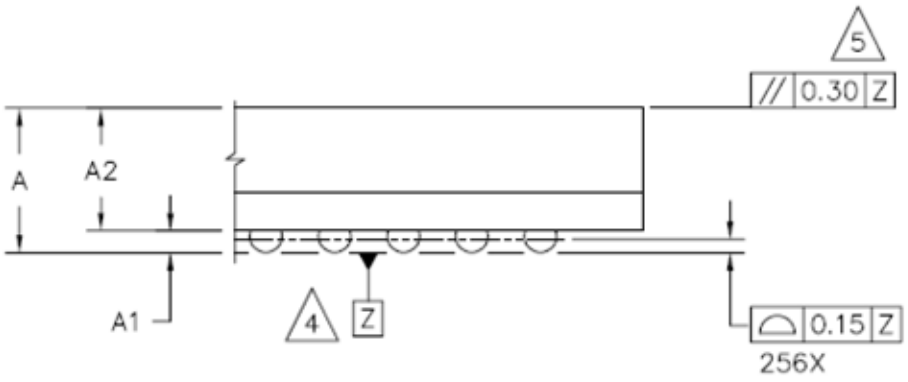


Figure 32. 256 MAPBGA Package Mechanical Drawing



DETAIL K
ROTATED 90° CLOCKWISE

DIM	MIN	MAX
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.40	0.60
D	17.00 BSC	
E	17.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

NOTES

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ARH98219A	REV: A
256 I/O STD MAP BGA, 17 X 17 PKG, 1.00 PITCH	CASE NUMBER: 1216B-01	15 JUL 2005
	STANDARD: NON-JEDEC	

Figure 33. 256 MAPBGA Package Detail