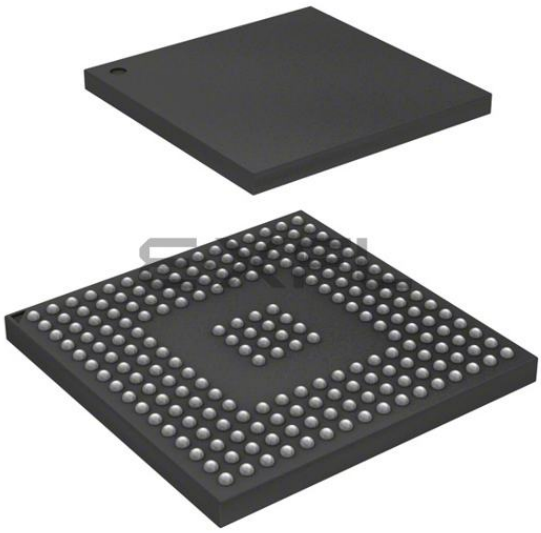

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z650
Core Size	32-Bit Single-Core
Speed	116MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	155
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	592K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 36x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BGA
Supplier Device Package	208-BGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5668gk0mmg

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Table 1. MPC5668G/MPC5668E Comparison

Feature	MPC5668G		MPC5668E	
Package	**208 MAPBGA**	**256 MAPBGA**	**208 MAPBGA**	**256 MAPBGA**
RAM with ECC	592 KB		128 KB	
MPU	No		16 entry	
DMA	16-channel		32-channel	
Ethernet (FEC)	Yes		No	
MediaLB (MLB-DIM)	Yes		No	
FlexRay	Yes (128 Message Buffers)		No	
ADC (10-bit)	36 internal channels Supports 32 external channels		64 internal channels Supports 32 external channels	
Total Timer I/O (eMIOS200)	24 channels, 16-bit		32 channels, 16-bit	
Cross Trigger Unit (CTU)	No		Yes	
SCI (eSCI)	6		12	
SPI (DSPI)	4		4	
CAN (FlexCAN)	6		5	
I^2C	4		4	
Nexus3 Debug (e200Z6) Nexus2+ Debug (e200Z0)	—	Supported on 256BGA emulation package	—	Supported on 256BGA emulation package

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PE3	PE[3] RXD_D eMIOS[28]	67	00 01 10 11	Port E GPIO eSCI_D Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	F3	F3
PE4	PE[4] TXD_E eMIOS[27]	68	00 01 10 11	Port E GPIO eSCI_E Transmit eMIOS Channel —	I/O O I/O	V_{DDE2}	SH	—	—	G3	G3
PE5	PE[5] RXD_E eMIOS[26]	69	00 01 10 11	Port E GPIO eSCI_E Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	H3	H3
PE6	PE[6] TXD_F eMIOS[25]	70	00 01 10 11	Port E GPIO eSCI_F Transmit eMIOS Channel —	I/O O I/O	V_{DDE2}	SH	—	—	M2	M2
PE7	PE[7] RXD_F eMIOS[24]	71	00 01 10 11	Port E GPIO eSCI_F Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	L2	L2
PE8	PE[8] TXD_G PCS_A[1]	72	00 01 10 11	Port E GPIO eSCI_G Transmit DSPI_A Peripheral Chip Select —	I/O O O	V_{DDE2}	SH	—	—	J4	J4
PE9	PE[9] RXD_G PCS_A[4]	73	00 01 10 11	Port E GPIO eSCI_G Receive DSPI_A Peripheral Chip Select —	I/O I O	V_{DDE2}	SH	—	—	M4	M4
PE10	PE[10] TXD_H PCS_B[3]	74	00 01 10 11	Port E GPIO eSCI_H Transmit DSPI_B Peripheral Chip Select —	I/O O O	V_{DDE2}	SH	—	—	N3	N3
PE11	PE[11] RXD_H PCS_B[2]	75	00 01 10 11	Port E GPIO eSCI_H Receive DSPI_B Peripheral Chip Select —	I/O I O	V_{DDE2}	SH	—	—	N4	N4
PE12	PE[12] TXD_J PCS_C[5]	76	00 01 10 11	Port E GPIO eSCI_J Transmit DSPI_C Peripheral Chip Select —	I/O O O	V_{DDE2}	SH	—	—	P4	P4
PE13	PE[13] RXD_J PCS_C[3]	77	00 01 10 11	Port E GPIO eSCI_J Receive DSPI_C Peripheral Chip Select —	I/O I O	V_{DDE2}	SH	—	—	P5	P5

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PE14	PE[14] SCL_A PCS_D[2]	78	00 01 10 11	Port E GPIO I^2C_A Serial Clock DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE2}	SH	—	—	N7	N7
PE15	PE[15] SDA_A PCS_D[5]	79	00 01 10 11	Port E GPIO I^2C_A Serial Data DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE2}	SH	—	—	N6	N6
Port F (16)											
PF0	PF[0] SCK_A	80	00 01 10 11	Port F GPIO DSPI_A Serial Clock — —	I/O I/O — —	V_{DDE2}	MH	—	—	H2	H2
PF1	PF[1] SOUT_A	81	00 01 10 11	Port F GPIO DSPI_A Serial Data Out — —	I/O O — —	V_{DDE2}	MH	—	—	J1	J1
PF2	PF[2] SIN_A	82	00 01 10 11	Port F GPIO DSPI_A Serial Data In — —	I/O I — —	V_{DDE2}	SH	—	—	J2	J2
PF3	PF[3] PCS_A[0] PCS_B[5] PCS_C[4]	83	00 01 10 11	Port F GPIO DSPI_A Peripheral Chip Select DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I/O O O	V_{DDE2}	SH	—	—	N2	N2
PF4	PF[4] SCK_B PCS_A[1] PCS_C[2]	84	00 01 10 11	Port F GPIO DSPI_B Serial Clock DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I/O O O	V_{DDE2}	MH	—	—	M1	M1
PF5	PF[5] SOUT_B PCS_A[2] PCS_C[3]	85	00 01 10 11	Port F GPIO DSPI_B Serial Data Out DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	P2	P2
PF6	PF[6] SIN_B PCS_A[3] PCS_C[5]	86	00 01 10 11	Port F GPIO DSPI_B Serial Data In DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I O O	V_{DDE2}	SH	—	—	N1	N1
PF7	PF[7] PCS_B[0] PCS_C[5] PCS_D[4]	87	00 01 10 11	Port F GPIO DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE2}	SH	—	—	R2	R2

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PG13	PG[13] eMIOS[2] FEC_TXD[1] AN[61]	109	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	L16	L16
PG14	PG[14] eMIOS[1] FEC_TXD[2] AN[62]	110	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	M16	M16
PG15	PG[15] eMIOS[0] FEC_TXD[3] AN[63]	111	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	N16	N16
Port H (16)											
PH0	PH[0] eMIOS[31] FEC_COL	112	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Collision —	I/O I/O I —	V_{DDE3}	SH	—	—	T14	T14
PH1	PH[1] eMIOS[30] FEC_RX_DV	113	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data Valid —	I/O I/O I —	V_{DDE3}	SH	—	—	P16	P16
PH2	PH[2] eMIOS[29] FEC_TX_EN	114	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Transmit Enable —	I/O I/O O —	V_{DDE3}	MH	—	—	R16	R16
PH3	PH[3] eMIOS[28] FEC_RX_ER	115	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Error —	I/O I/O I —	V_{DDE3}	SH	—	—	N15	N15
PH4	PH[4] eMIOS[27] FEC_RXD[0]	116	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	P15	P15
PH5	PH[5] eMIOS[26] FEC_RXD[1]	117	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	R14	R14
PH6	PH[6] eMIOS[25] FEC_RXD[2]	118	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	R15	R15

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PK6	PK[6] FR_B_RX PCS_B[1] PCS_C[4]	150	00 01 10 11	Port K GPIO FlexRay B Receive Data DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I O O	V_{DDE2}	SH	—	—	R5	R5
PK7	PK[7] FR_B_TX PCS_B[2] PCS_C[5]	151	00 01 10 11	Port K GPIO FlexRay B Transmit Data DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	T5	T5
PK8	PK[8] FR_B_TX_EN PCS_B[3] PCS_A[1]	152	00 01 10 11	Port K GPIO FlexRay B Transmit Enable DSPI_B Peripheral Chip Select DSPI_A Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	R6	R6
PK9	PK[9] CLKOUT PCS_D[1] PCS_A[2] BOOTCFG	153	00 01 10 11	Port K GPIO CLKOUT (User mode) DSPI_D Peripheral Chip Select DSPI_A Peripheral Chip Select Boot Configuration	I/O O O O I	V_{DDE2}	MH	BOOT CFG (Pull-down)	GPIO	T6	T6
PK10	PK[10] PCS_B[5] PCS_D[2] PCS_A[3]	154	00 01 10 11	Port K GPIO DSPI_B Peripheral Chip Select DSPI_D Peripheral Chip Select DSPI_A Peripheral Chip Select	I/O O O O	V_{DDE2}	SH	—	—	P6	P6
Nexus Pins (17)											
$\overline{\text{EVTI}}$	$\overline{\text{EVTI}}$	—	—	Nexus Event In	I	V_{DDENEX}	F	—	—	—	M11
$\overline{\text{EVTO}}$	$\overline{\text{EVTO}}$	—	—	Nexus Event Out	O	V_{DDENEX}	F	—	—	—	M12
$\overline{\text{MSEO0}}$	$\overline{\text{MSEO[0]}}$	—	—	Nexus Message Start/End Out	O	V_{DDENEX}	F	—	—	—	M9
$\overline{\text{MSEO1}}$	$\overline{\text{MSEO[1]}}$	—	—	Nexus Message Start/End Out	O	V_{DDENEX}	F	—	—	—	M8
MCKO	MCKO	—	—	Nexus Message Clock Out	O	V_{DDENEX}	F	—	—	—	M10
MDO0	MDO[0]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	E5
MDO1	MDO[1]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	F5
MDO2	MDO[2]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	G5
MDO3	MDO[3]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	H5
MDO4	MDO[4]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	H6
MDO5	MDO[5]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	J6
MDO6	MDO[6]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	J5
MDO7	MDO[7]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	K5
MDO8	MDO[8]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	L5
MDO9	MDO[9]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	M5
MDO10	MDO[10]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	M6

4 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5668x.

4.1 Maximum Ratings

Table 4. Absolute Maximum Ratings[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	1.2 V Core Supply Voltage[2]	V_{DD}	–0.3	1.32[3]	V
2	3.3 V Clock Synthesizer Voltage[2, 4]	V_{DDSYN}	–0.3	3.6	V
3	3.3 V I/O Buffer Voltage [2, 4]	V_{DD33}	–0.3	3.6	V
4	3.3–5.0 V Voltage Regulator Control Voltage [2, 5, 6]	V_{RC}	–0.3	5.5	V
5	3.3–5.0 V Analog Supply Voltage (reference to V_{SSA}) [2, 5]	V_{DDA}	–0.3	5.5	V
6	3.3–5.0 V External I/O Supply Voltage [2, 5, 7]	V_{DDE1}[8] V_{DDE2}[8] V_{DDE3}[8] V_{DDE4}[8]	–0.3 –0.3 –0.3 –0.3	5.5 5.5 5.5 5.5	V
7	2.5–3.3 V External I/O Supply Voltage (MLB) [2, 4]	V_{DDEMLB}[8]	–0.3	3.6	V
8	3.3 V External I/O Supply Voltage (Nexus) [2, 4]	V_{DDENEX}[8]	–0.3	3.6	V
9	DC Input Voltage[9] V_{DDE1}, V_{DDE2}, V_{DDE3}, V_{DDE4} V_{DDEMLB}, V_{DDENEX}	V_{IN}	 –1.0[10] –1.0[9]	 V_{DDEx} + 0.3 V[11] V_{DDEx} + 0.3 V[10]	V
10	Analog Reference High Voltage	V_{RH}	–0.3	Minimum of 5.5 or V_{DDA} + 0.3	V
11	Analog Reference Low Voltage	V_{RL}	–0.3	5.5	V
12	V_{SS} to V_{SSA} Differential Voltage	$V_{SS} – V_{SSA}$	–100	100	mV
13	V_{SS} to V_{SSSYN} Differential Voltage	$V_{SS} – V_{SSSYN}$	–100	100	mV
14	Maximum DC Digital Input Current[12] (per pin, applies to all digital F, MH, SH, and IH pins)	I_{MAXD}	–2	2	mA
15	Maximum DC Analog Input Current[13] (per pin, applies to all analog AE and A pins)	I_{MAXA}	–3	3	mA
16	Storage Temperature Range	T_{STG}	–55.0	150.0	°C
17	Maximum Solder Temperature[14]	T_{SDR}	—	235.0	°C
18	Moisture Sensitivity Level[15]	MSL	—	3	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

3 2.0 V for 10 hours cumulative time, 1.2 V +10% for time remaining.

4 5.3 V for 10 hours cumulative time, 3.3 V +10% for time remaining.

5 6.4 V for 10 hours cumulative time, 5.0 V +10% for time remaining.

6 VRC cannot be 100mV higher than VDDA. VDDSYN and VDD33 cannot be 100mV higher than VRC.

7 All functional non-supply I/O pins are clamped to V_{SS} and V_{DDEx}.

8 V_{DDEx} are separate power segments and may be powered independently with no differential voltage constraints between the power segments.

9 AC signal over and undershoot of the input voltages of up to ±2.0 V is permitted for a cumulative duration of 60 hours over the complete lifetime of the device (injection current does not need to be limited for this duration).

10 Internal structures will hold the input voltage above –1.0 V if the injection current limit of 2 mA is met.

11 Internal structures hold the input voltage below this maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (25 mA for all pins) and V_{DDE} is within Operating Voltage specifications.

12 Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

13 Total injection current for all analog input pins must not exceed 15 mA.

14 Solder profile per CDF-AEC-Q100.

15 Moisture sensitivity per JEDEC test method A112.

4.2 Thermal Characteristics

Table 5. Thermal Characteristics

Spec	Characteristic	Symbol	Unit	Value	
				208 MAPBGA	256 MAPBGA
1	Junction to Ambient[1, 2] Natural Convection (Single layer board)	$R_{\theta JA}$	°C/W	39	39
2	Junction to Ambient[1, 3] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	°C/W	24	24
3	Junction to Ambient[1, 3] (@200 ft./min., Single layer board)	$R_{\theta JMA}$	°C/W	31	31
4	Junction to Ambient[1, 3] (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	°C/W	20	20
5	Junction to Board[4]	$R_{\theta JB}$	°C/W	13	13
6	Junction to Case[5]	$R_{\theta JC}$	°C/W	6	6
7	Junction to Package Top[6] Natural Convection	Ψ_{JT}	°C/W	2	2

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

4.3 ESD Characteristics

Table 6. ESD Ratings[1, 2]

Characteristic	Symbol	Value	Unit
ESD for Human Body Model (HBM)		2000	V
HBM Circuit Description	R1	1500	Ohm
	C	100	pF
ESD for Field Induced Charge Model (FDCM)		750 (corner pins)	V
		250 (all other pins)	
Number of Pulses per pin: Positive Pulses (HBM) Negative Pulses (HBM)	 — —	 1 1	 — —
Interval of Pulses	—	1	second

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.4 VRC Electrical Specifications

Table 7. VRC Electrical Specifications

Spec	Characteristic	Symbol	Min	Max	Units
1	Current which can be sourced by V_{RCCTL}	I_V_{RCCTL}	6.25 µA	20 mA	—
2	Minimum Required Gain from external circuit: I_{DD} / I_V_{RCCTL} (@V_{DD} = 1.32 V)[1] –40°C 25°C 150°C	BETA	 50 50 50	 500	

1 Assumes “typical usage” currents which will vary with application.

4.5 DC Electrical Specifications

Table 8. DC Electrical Specifications

Spec	Characteristic	Symbol	Min	Max	Unit
1	Maximum Operating Temperature Range — Die Junction Temperature	T_J	–40.0	150.0	°C
2	3.3 V Clock Synthesizer Voltage[1]	V_{DDSYN}	3.0	3.6	V
3	3.3 V I/O Buffer Voltage[1]	V_{DD33}	3.0	3.6	V
4	3.3–5.0 V Voltage Regulator Reference Voltage[1] V_{RCSEL} = V_{SSA} V_{RCSEL} = V_{DDA}	V_{VRC}	 3.0 4.5	 3.6 5.5	V
5	3.3–5.0 V Analog Supply Voltage	V_{DDA}	maximum of 3.0 V or V_{VRC} – 0.1	5.5	V

Table 8. DC Electrical Specifications

Spec	Characteristic	Symbol	Min	Max	Unit
6	3.3–5.0 V External I/O Supply Voltage[2] V_{DDE1} V_{DDE2} V_{DDE3} V_{DDE4}		 3.0 3.0 3.0 3.0	 5.5 5.5 5.5 5.5	V
7	2.5 V – 3.3 V External I/O Supply Voltage (MLB)	V_{DDEMLB}[3]	2.375	3.6	V
8	3.3 V External I/O Supply Voltage (Nexus)	V_{DDENEX}	3.0	3.6	V
9	Pad Input High Voltage Hysteresis enabled Hysteresis disabled (IHA/SH/SHA/MH/MHA)[4, 5] Hysteresis disabled (F)	V_{IH}	 0.65 × V_{DDE} 0.55 × V_{DDE} 0.55 × V_{DDE}	V_{DDE} + 0.3	V
10	Pad Input Low Voltage Hysteresis enabled Hysteresis disabled (IHA/SH/SHA/MH/MHA)[4, 5] Hysteresis disabled (F)	V_{IL}	V_{SS} – 0.3	 0.35 × V_{DDE} 0.40 × V_{DDE} 0.40 × V_{DDE}	V
11	Pad Input Hysteresis	V_{HYS}	0.1 × V_{DDE}		V
12	Analog (IHA) Input Voltage	V_{INDC}	V_{SSA} – 0.3	V_{DDA} + 0.3	V
13	Pad Output High Voltage[6, 7, 8]	V_{OH}	0.8 × V_{DDE}	—	V
14	Pad Output Low Voltage[8]	V_{OL}	—	0.2 × V_{DDE}	V
15	Input Capacitance (Digital Pins: Pad type F, MH, SH)[4]	C_{IN}	—	7	pF
16	Input Capacitance (Analog Pins: Pad type IHA)[4, 5]	C_{IN_A}	—	10	pF
17	Input Capacitance (Shared digital/analog pins: MHA, SHA)[4]	C_{IN_M}	—	12	pF
18	I/O Weak Pull Up/Down Absolute Current[4, 9] Pad F: 2.375 V – 3.6 V Pad SH/MH/IHA: 3.0 V – 3.6 V Pad SH/MH/IHA: 4.5 V – 5.5 V	I_{ACT}	 25 10 35	 180 95 200	µA
19	I/O Input Leakage Current[10]	I_{INACT_D}	–2.5	2.5	µA
20	DC Injection Current (per pin)	I_{IC}	–1.0	1.0	mA
21	Analog Input Current, Channel Off[11] (Analog pins IHA)[4, 5]	I_{INACT_A}	–150	150	nA
22	Analog Reference High Voltage	V_{RH}	V_{DDA} – 500	V_{DDA}	mV
23	Analog Reference Low Voltage	V_{RL}	V_{SSA}	V_{SSA} + 500	mV
24	V_{SS} to V_{SSA} Differential Voltage	$V_{SS} – V_{SSA}$	–100	100	mV
25	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} – V_{SS}$	–100	100	mV
26	Slew rate on V_{DDA}, V_{DDEx}, V_{DDSYN}, V_{DD33}, and V_{RC} power supply pins	V_{Ramp}	—	100	V/ms
27	Capacitive Supply Load (V_{DD})	V_{Load}	8	—	µF
28	Capacitive Supply Load (V_{DD33}, V_{DDSYN})	V_{Load}	1	—	µF

1 When V_{RCSEL} = V_{SSA} (low), V_{DDSYN} and V_{DD33} are externally supplied. When V_{RCSEL} = V_{DDA} (high), V_{DDSYN} and V_{DD33} are generated by internal voltage regulators. When V_{RCSEL} = V_{SSA} (low), V_{DDSYN} and V_{DD33} cannot be 100 mV higher than V_{RC}.

Table 14. 3.3 V High Frequency External Oscillator (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
8	Crystal manufacturer's recommended capacitive load	C_L	See crystal specification	See crystal specification	pF
9	Discrete load capacitance to be connected to EXTAL	C_{L_EXTAL}	—	$2\times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$[5]	pF
10	Discrete load capacitance to be connected to XTAL	C_{L_XTAL}	—	$2\times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$[5]	pF
11	Startup Time	$t_{startup}$	—	10	ms

1 When PLL frequency modulation is active, reference frequencies less than 8 MHz will distort the modulated waveform and the effects of this on emissions is not characterized.

2 This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case, $V_{extal} - V_{xtal} \geq 400$ mV criteria has to be met for oscillator's comparator to produce output clock.

3 This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case, $V_{xtal} - V_{extal} \geq 400$ mV criteria has to be met for oscillator's comparator to produce output clock.

4 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

5 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

Table 15. 5 V Low Frequency (32 kHz) External Oscillator

Spec	Characteristic	Symbol	Min	Max	Unit
1	Frequency Range	f_{ref32}	32	40	kHz
2	Duty Cycle of reference	t_{dc32}	40	60	%
3	XTAL32 Current[1]	I_{XTAL32}	—	3	µA
4	Crystal manufacturer's recommended capacitive load	C_{L32}	See crystal specification	See crystal specification	pF
5	Startup Time	$t_{Startup}$	—	2	s

1 I_{xtal32} is the oscillator bias current out of the XTAL32 pin with both EXTAL32 and XTAL32 pins grounded.

Table 16. 5 V High Frequency (16 MHz) Internal RC Oscillator

Spec	Characteristic	Symbol	Range	Min	Typ	Max	Unit
1	Frequency before trim[1]	f_{ut}	35%	10.4	16	21.6	MHz
2	Frequency after loading factory trim[2]	f_t	7%	14.9	16	17.1	MHz
3	Application trim resolution[3]	t_s	—	—	—	±0.5	%
4	Application frequency trim step[3]	f_s	—	—	300	—	kHz
5	Startup Time	$t_{Startup}$	—	—	—	500	ns

1 Across process, voltage, and temperature.

2 Across voltage and temperature.

3 Fixed voltage and temperature.

Table 17. 5V Low Frequency (128 kHz) Internal RC Oscillator

Spec	Characteristic	Symbol	Range	Min	Typ	Max	Unit
1	Frequency before trim[1]	F_{ut128}	35%	83.2	128	172.8	kHz
2	Frequency after loading factory trim[2]	F_{t128}	7%	119.0	128	137.0	kHz
3	Application trim resolution[3]	T_{s128}	—	—	—	±2	%
4	Application frequency trim step[3]	F_{s128}	—	—	4	—	kHz
5	Startup Time	S_{t128}	—	—	—	100	µs

1 Across process, voltage, and temperature.

2 Across voltage and temperature.

3 Fixed voltage and temperature.

4.10 FMPLL Electrical Characteristics

Table 18. FMPLL Electrical Specifications[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	System Frequency[2]	f_{SYS}	—	116	MHz
2	PLL Reference Frequency Range	f_{REF}	4	40	MHz
3	PLL Frequency	f_{PLL}	$\frac{f_{vco(min)}}{(ERFD+1)}$		MHz
4	Loss of Reference Frequency [3]	f_{LOR}	100	2000	kHz
5	Self Clocked Mode Frequency	f_{SCM}	16	64	MHz
6	PLL Lock Time[4]	t_{LPLL}	—	400	µs
7	Duty Cycle of Reference	t_{DC}	40	60	%
8	Frequency un-LOCK Range	f_{UL}	–4.0	4.0	% f_{SYS}
9	Frequency LOCK Range	f_{LCK}	–2.0	2.0	% f_{SYS}
10	CLKOUT Period Jitter,[5] Measured at f_{SYS} Max Cycle-to-cycle Jitter	C_{Jitter}	–5	5	%f_{SYS}
11	CLKOUT Jitter at ≥ 50 µs period	C_{Jitter}	–250	250	ns
12	Peak-to-Peak Frequency Modulation Range Limit [6,7] (f_{SYS}Max must not be exceeded)	C_{mod}	0	4	%f_{SYS}
13	FM Depth Tolerance[8]	C_{mod_err}	–0.50	0.50	%f_{SYS}
14	VCO Frequency[9]	f_{VCO}	192	600	MHz
15	Modulation Rate Limits[10]	f_{MOD}	0.400	1	MHz

1 V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H.

4.14 AC Timing

4.14.1 Reset and Boot Configuration Pins

Table 24. Reset and Boot Configuration Timing

Spec	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	150	—	ns
2	BOOTCFG Setup Time after $\overline{\text{RESET}}$ Valid	t_{RCSU}	—	100	µs
3	BOOTCFG Hold Time from $\overline{\text{RESET}}$ Valid	t_{RCH}	0	—	µs

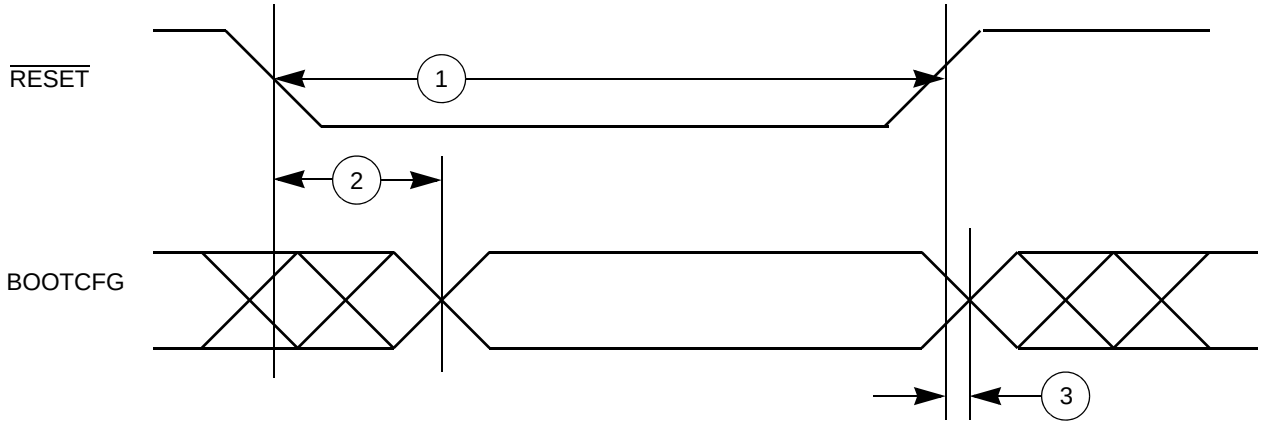


Figure 7. Reset and Boot Configuration Timing

4.14.2 External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) Pins

Table 25. IRQ/NMI Timing

Spec	Characteristic	Symbol	Min	Max	Unit
1	IRQ/NMI Pulse Width Low	t_{IPWL}	3	—	t_{SYS}
2	IRQ/NMI Pulse Width High	T_{IPWH}	3	—	t_{SYS}
3	IRQ/NMI Edge to Edge Time[1]	t_{ICYC}	6	—	t_{SYS}

[1] Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

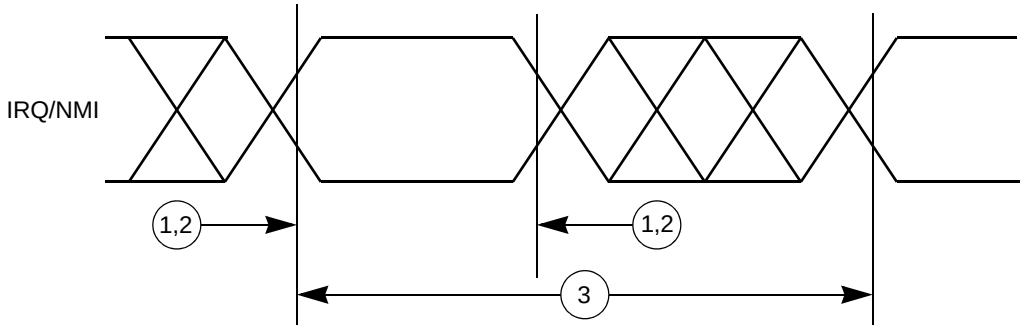


Figure 8. IRQ and NMI Timing

4.14.4 Nexus Debug Interface

Table 27. Nexus Debug Port Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time	t_{MCYC}	15.6	—	ns
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid[2]	t_{MDOV}	–0.1	0.25	t_{MCYC}
4	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC}
5	$\overline{\text{EVTO}}$ Pulse Width	t_{EVTOPW}	1		t_{MCYC}
6	TCK Cycle Time[3]	t_{TCYC}	40	—	ns
7	TCK Duty Cycle	t_{TDC}	40	60	%
8	TDI, TMS Data Setup Time	t_{NTDIS}, t_{NTMSS}	8	—	ns
9	TDI, TMS Data Hold Time	t_{NTDIH}, t_{NTMSH}	5	—	ns
10	TCK Low to TDO Data Valid	t_{JOV}	0	25	ns

1 JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DDE} = 3.0 – 5.5 V, $T_A = T_L$ to T_H, and C_L = 30 pF with SRC = 0b11.

2 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

3 The system clock frequency needs to be three times faster than the TCK frequency.

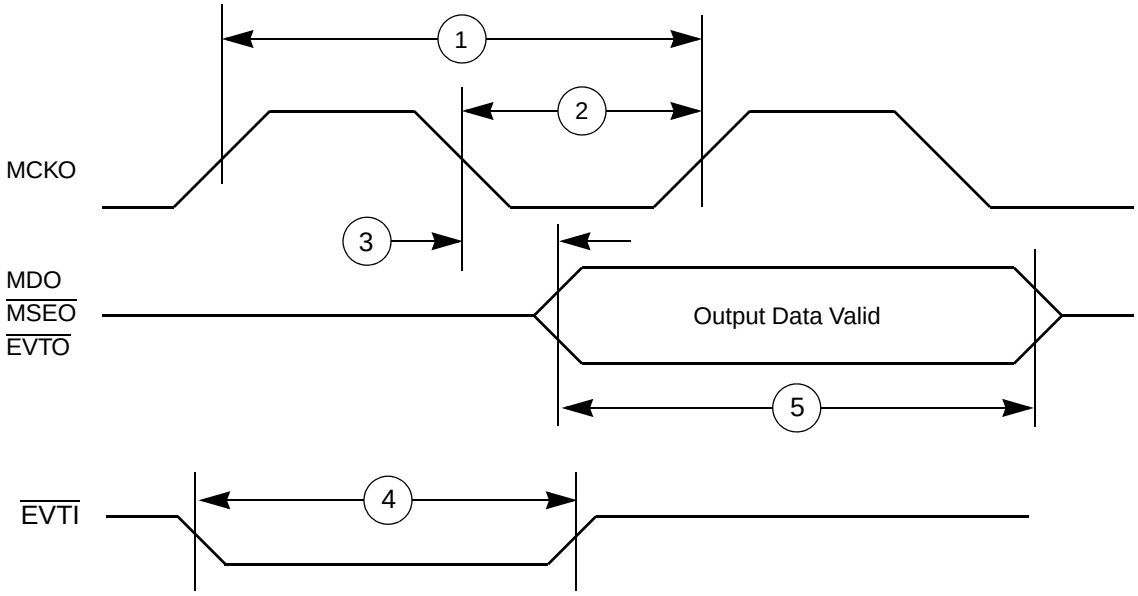


Figure 13. Nexus Output Timing

4.14.5 Enhanced Modular I/O Subsystem (eMIOS)

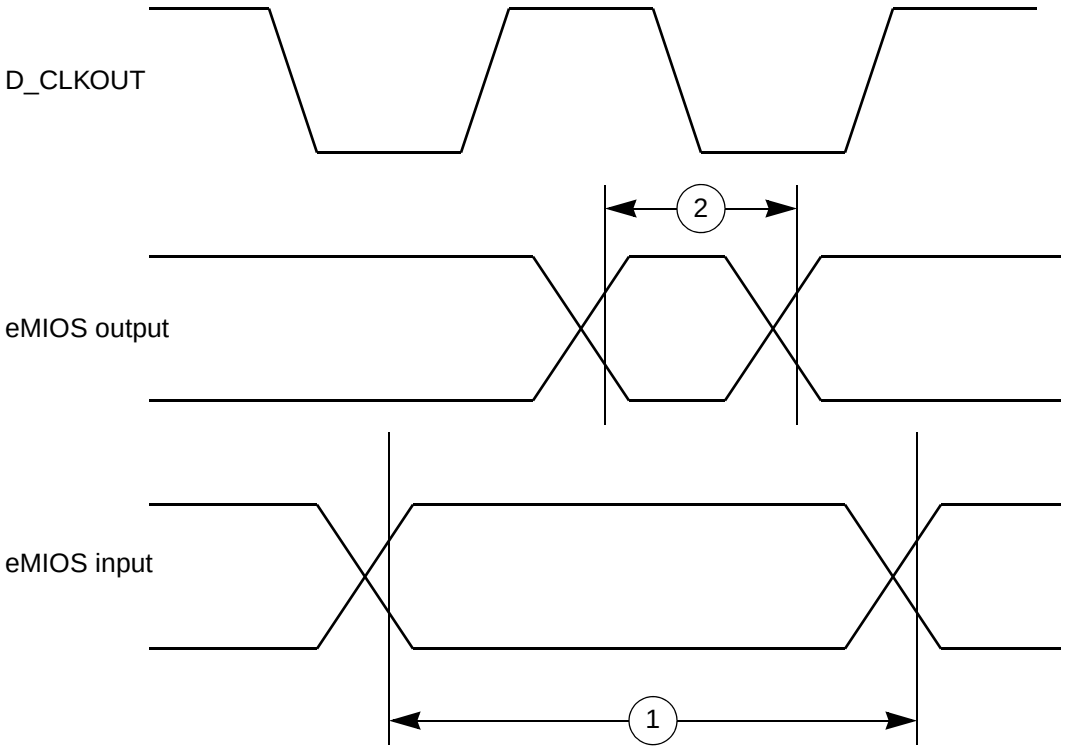
Table 28. eMIOS Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{CYC}
2	eMIOS Output Pulse Width	t_{MOPW}	1[2]	—	t_{CYC}

1 eMIOS timing specified at V_{DDE} = 3.0 – 5.5 V, $T_A = T_L$ to T_H, and CL = 30 pF with SRC = 0b11.

2 This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

Figure 15. eMIOS Timing



4.14.6 Deserial Serial Peripheral Interface (DSPI)

Table 29. DSPI Timing

Spec	Characteristic	Symbol	116 MHz[1]		Unit
			Min. Value	Max. Value	
1	DSPI Cycle Time Master (MTFE = 0) Slave (MTFE = 0) Master (MTFE = 1) Slave (MTFE = 1)	t_{SCK}	 100 100 50 50	 — — — —	 ns ns ns ns
2	PCS to SCK Delay[2]	t_{CSC}	7	—	ns
3	After SCK Delay[3]	t_{ASC}	14	—	ns
4	SCK Duty Cycle	t_{SDC}	$0.4 \times t_{SCK}$	$0.6 \times t_{SCK}$	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT valid)	t_A	—	25	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	PCSx to $\overline{PCSS}$ time	t_{PCSC}	0	—	ns
8	$\overline{PCSS}$ to PCSx time	t_{PASC}	0	—	ns
9	Data Setup Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[4] Master (MTFE = 1, CPHA = 1)	t_{SUI}	 25 5 10 25	 — — — —	 ns ns ns ns
10	Data Hold Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[4] Master (MTFE = 1, CPHA = 1)	t_{HI}	 –4 7 12 –4	 — — — —	 ns ns ns ns
11	Data Valid (after SCK edge) Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{SUO}	 — — — —	 8 28 15 8	 ns ns ns ns
12	Data Hold Time for Outputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{HO}	 –7 2 1 –7	 — — — —	 ns ns ns ns

1 116 MHz timing specified at CL = 50 pF with SRC = 0b11.

2 The maximum value is programmable in DSPI_CTAR*n*[PSSCK] and DSPI_CTAR*n*[CSSCK].

3 The maximum value is programmable in DSPI_CTAR*n*[PASC] and DSPI_CTAR*n*[ASC].

4 This number is calculated assuming the SMPL_PT bit field in DSPI_MCR is set to 0b10.

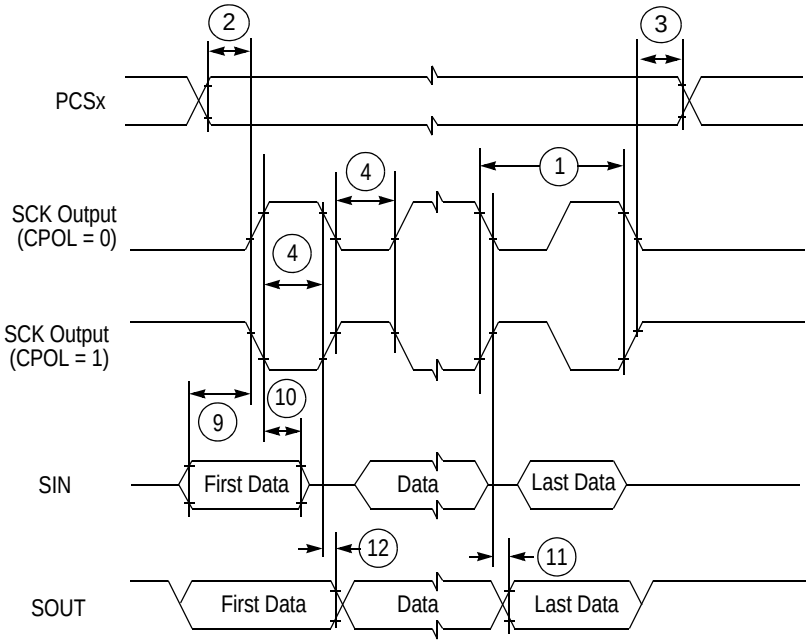


Figure 16. DSPI Classic SPI Timing — Master, CPHA = 0

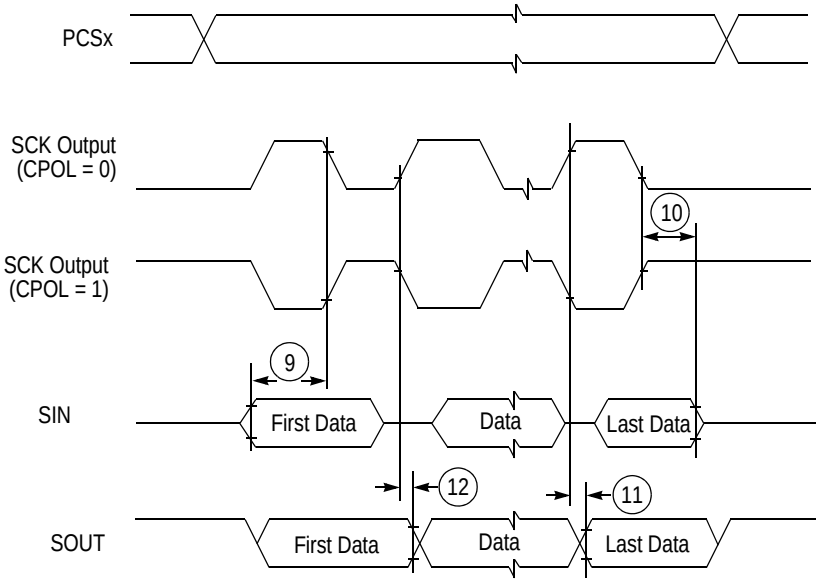


Figure 17. DSPI Classic SPI Timing — Master, CPHA = 1

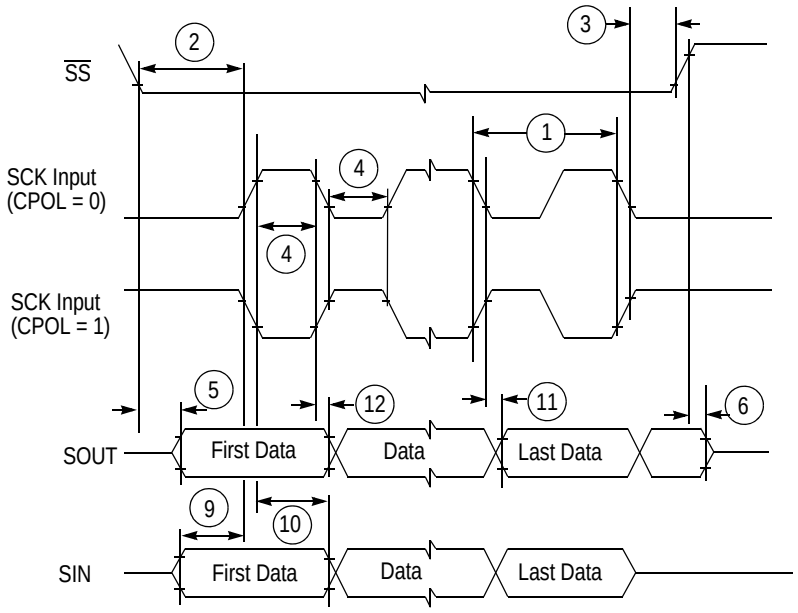


Figure 18. DSPI Classic SPI Timing — Slave, CPHA = 0

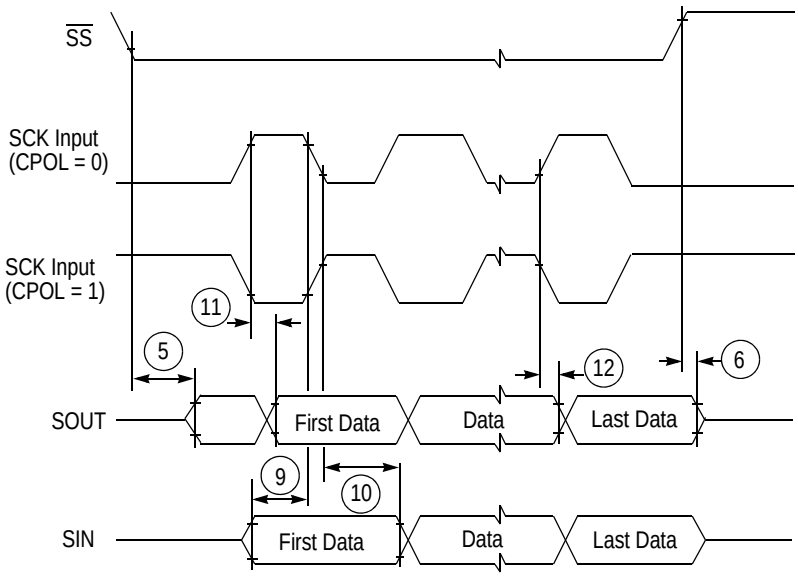


Figure 19. DSPI Classic SPI Timing — Slave, CPHA = 1

4.14.8.3 MII Async Inputs Signal Timing (CRS and COL)

Table 35. MII Async Inputs Signal Timing[1]

Spec	Characteristic	Min	Max	Unit
M9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

1 Output pads configured with SRC = 0b11.

Figure 28. MII Async Inputs Timing Diagram

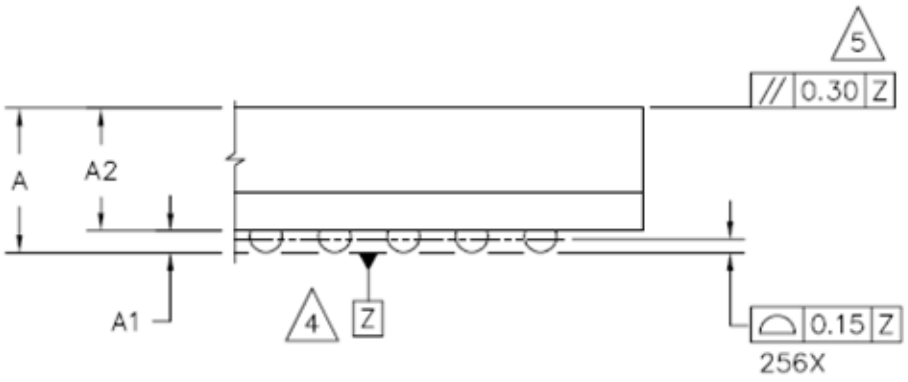
4.14.8.4 MII Serial Management Channel Timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 36. MII Serial Management Channel Timing[1]

Spec	Characteristic	Min	Max	Unit
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	10	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

1 Output pads configured with SRC = 0b11.



DETAIL K
ROTATED 90° CLOCKWISE

DIM	MIN	MAX
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.40	0.60
D	17.00 BSC	
E	17.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

NOTES

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

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256 I/O STD MAP BGA, 17 X 17 PKG, 1.00 PITCH	CASE NUMBER: 1216B-01	15 JUL 2005
	STANDARD: NON-JEDEC	

Figure 33. 256 MAPBGA Package Detail

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Document Number: MPC5668X
Rev. 6
2010, 2011