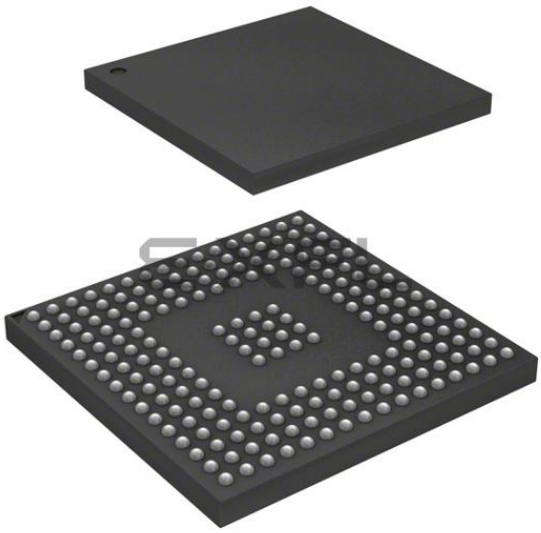

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Supplier Device Package	208-BGA (17x17)
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3 Pin Assignments

3.1 208-ball MAPBGA Pin Assignments

Figure 3 shows the 208-ball MAPBGA pin assignments.

Figure 3. MPC5668x 208-ball MAPBGA (full diagram)

3.3 Pin Muxing and Reset States

Table 2 shows the signals properties for each pin on MPC5668x. For all port pins that have an associated SIU_PCR*n* register to control pin properties, the supported functions column lists the functions associated with the programming of the SIU_PCR*n*[PA] bit in the order: general-purpose input/output (GPIO), function 1, function 2, and function 3 (see Figure 5). When an alternate function is not implemented for a value of SIU_PCR*n*[PA], a dash is shown in the Description column and the respective value in the PA bit field is reserved.

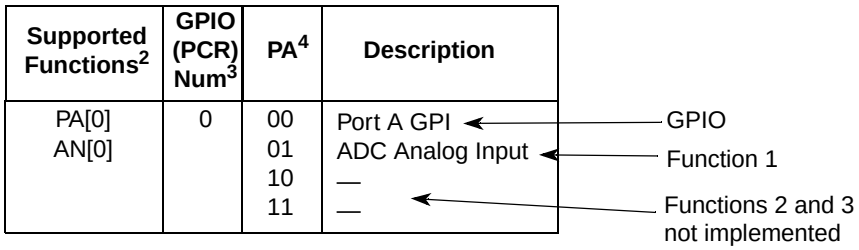


Figure 5. Supported Functions Example

Table 2. MPC5668x Signal Properties

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
Port A (16)											
PA0	PA[0] AN[0]	0	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	D15	D15
PA1	PA[1] AN[1]	1	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	E15	E15
PA2	PA[2] AN[2]	2	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	F16	F16
PA3	PA[3] AN[3]	3	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	F15	F15
PA4	PA[4] AN[4]	4	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	G16	G16
PA5	PA[5] AN[5]	5	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	G15	G15

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PA6	PA[6] AN[6]	6	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	H16	H16
PA7	PA[7] AN[7]	7	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	G14	G14
PA8	PA[8] AN[8]	8	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	F14	F14
PA9	PA[9] AN[9]	9	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	E14	E14
PA10	PA[10] AN[10]	10	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	D13	D13
PA11	PA[11] AN[11]	11	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	E13	E13
PA12	PA[12] AN[12]	12	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	D14	D14
PA13	PA[13] AN[13]	13	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	F13	F13
PA14	PA[14] AN[14] EXTAL32	14	00 01 10 11	Port A GPI ADC Analog Input External 32 kHz Crystal In —	I I I —	V_{DDA}	IHA	—	—	D16	D16
PA15	PA[15] AN[15] XTAL32	15	00 01 10 11	Port A GPI ADC Analog Input External 32 kHz Crystal Out —	I I O —	V_{DDA}	IHA	—	—	E16	E16

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PB10	PB[10] AN[26] PCS_B[4]	26	00 01 10 11	Port B GPIO ADC Analog Input DSPI_B Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	A9	A9
PB11	PB[11] AN[27] PCS_B[5]	27	00 01 10 11	Port B GPIO ADC Analog Input DSPI_B Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	B9	B9
PB12	PB[12] AN[28] PCS_C[1]	28	00 01 10 11	Port B GPIO ADC Analog Input DSPI_C Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	C10	C10
PB13	PB[13] AN[29] PCS_C[2]	29	00 01 10 11	Port B GPIO ADC Analog Input DSPI_C Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	A8	A8
PB14	PB[14] AN[30] PCS_D[3]	30	00 01 10 11	Port B GPIO ADC Analog Input DSPI_D Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	B8	B8
PB15	PB[15] AN[31] PCS_D[4]	31	00 01 10 11	Port B GPIO ADC Analog Input DSPI_D Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	C9	C9
Port C (16)											
PC0	PC[0] AN[32]	32	00 01 10 11	Port C GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	D9	D9
PC1	PC[1] AN[33]	33	00 01 10 11	Port C GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	C8	C8
PC2	PC[2] AN[34] EVTI	34	00 01 10 11	Port C GPIO ADC Analog Input Nexus Event In —	I/O I I —	V_{DDE1}	SHA	—	—	A7	A7
PC3	PC[3] AN[35] EVTO	35	00 01 10 11	Port C GPIO ADC Analog Input Nexus Event Out —	I/O I O —	V_{DDE1}	SHA	—	—	B7	B7

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PC15	PC[15] AN[47] MA[2] —	47	00 01 10 11	Port C GPIO ADC Analog Input ADC Ext. Mux Address Select —	I/O I O —	V_{DDE1}	SHA	—	—	D5	D5
Port D (16)											
PD0	PD[0] CNTX_A	48	00 01 10 11	Port D GPIO FlexCAN_A Transmit — —	I/O O — —	V_{DDE2}	SH	—	—	A2	A2
PD1	PD[1] CNRX_A	49	00 01 10 11	Port D GPIO FlexCAN_A Receive — —	I/O I — —	V_{DDE2}	SH	—	—	B2	B2
PD2	PD[2] CNTX_B	50	00 01 10 11	Port D GPIO FlexCAN_B Transmit — —	I/O O — —	V_{DDE2}	SH	—	—	B1	B1
PD3	PD[3] CNRX_B	51	00 01 10 11	Port D GPIO FlexCAN_B Receive — —	I/O I — —	V_{DDE2}	SH	—	—	C1	C1
PD4	PD[4] CNTX_C	52	00 01 10 11	Port D GPIO FlexCAN_C Transmit — —	I/O O — —	V_{DDE2}	SH	—	—	C2	C2
PD5	PD[5] CNRX_C	53	00 01 10 11	Port D GPIO FlexCAN_C Receive — —	I/O I — —	V_{DDE2}	SH	—	—	D1	D1
PD6	PD[6] CNTX_D TXD_K SCL_B	54	00 01 10 11	Port D GPIO FlexCAN_D Transmit SCI_K Transmit I^2C_B Serial Clock	I/O O O I/O	V_{DDE2}	SH	—	—	D2	D2
PD7	PD[7] CNRX_D RXD_K SDA_B	55	00 01 10 11	Port D GPIO FlexCAN_D Receive SCI_K Receive I^2C_B Serial Data	I/O I I I/O	V_{DDE2}	SH	—	—	E1	E1
PD8	PD[8] CNTX_E TXD_L SCL_C	56	00 01 10 11	Port D GPIO FlexCAN_E Transmit SCI_L Transmit I^2C_C Serial Clock	I/O O O I/O	V_{DDE2}	SH	—	—	E2	E2

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PE3	PE[3] RXD_D eMIOS[28]	67	00 01 10 11	Port E GPIO eSCI_D Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	F3	F3
PE4	PE[4] TXD_E eMIOS[27]	68	00 01 10 11	Port E GPIO eSCI_E Transmit eMIOS Channel —	I/O O I/O	V_{DDE2}	SH	—	—	G3	G3
PE5	PE[5] RXD_E eMIOS[26]	69	00 01 10 11	Port E GPIO eSCI_E Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	H3	H3
PE6	PE[6] TXD_F eMIOS[25]	70	00 01 10 11	Port E GPIO eSCI_F Transmit eMIOS Channel —	I/O O I/O	V_{DDE2}	SH	—	—	M2	M2
PE7	PE[7] RXD_F eMIOS[24]	71	00 01 10 11	Port E GPIO eSCI_F Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	L2	L2
PE8	PE[8] TXD_G PCS_A[1]	72	00 01 10 11	Port E GPIO eSCI_G Transmit DSPI_A Peripheral Chip Select —	I/O O O	V_{DDE2}	SH	—	—	J4	J4
PE9	PE[9] RXD_G PCS_A[4]	73	00 01 10 11	Port E GPIO eSCI_G Receive DSPI_A Peripheral Chip Select —	I/O I O	V_{DDE2}	SH	—	—	M4	M4
PE10	PE[10] TXD_H PCS_B[3]	74	00 01 10 11	Port E GPIO eSCI_H Transmit DSPI_B Peripheral Chip Select —	I/O O O	V_{DDE2}	SH	—	—	N3	N3
PE11	PE[11] RXD_H PCS_B[2]	75	00 01 10 11	Port E GPIO eSCI_H Receive DSPI_B Peripheral Chip Select —	I/O I O	V_{DDE2}	SH	—	—	N4	N4
PE12	PE[12] TXD_J PCS_C[5]	76	00 01 10 11	Port E GPIO eSCI_J Transmit DSPI_C Peripheral Chip Select —	I/O O O	V_{DDE2}	SH	—	—	P4	P4
PE13	PE[13] RXD_J PCS_C[3]	77	00 01 10 11	Port E GPIO eSCI_J Receive DSPI_C Peripheral Chip Select —	I/O I O	V_{DDE2}	SH	—	—	P5	P5

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PE14	PE[14] SCL_A PCS_D[2]	78	00 01 10 11	Port E GPIO I^2C_A Serial Clock DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE2}	SH	—	—	N7	N7
PE15	PE[15] SDA_A PCS_D[5]	79	00 01 10 11	Port E GPIO I^2C_A Serial Data DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE2}	SH	—	—	N6	N6
Port F (16)											
PF0	PF[0] SCK_A	80	00 01 10 11	Port F GPIO DSPI_A Serial Clock — —	I/O I/O — —	V_{DDE2}	MH	—	—	H2	H2
PF1	PF[1] SOUT_A	81	00 01 10 11	Port F GPIO DSPI_A Serial Data Out — —	I/O O — —	V_{DDE2}	MH	—	—	J1	J1
PF2	PF[2] SIN_A	82	00 01 10 11	Port F GPIO DSPI_A Serial Data In — —	I/O I — —	V_{DDE2}	SH	—	—	J2	J2
PF3	PF[3] PCS_A[0] PCS_B[5] PCS_C[4]	83	00 01 10 11	Port F GPIO DSPI_A Peripheral Chip Select DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I/O O O	V_{DDE2}	SH	—	—	N2	N2
PF4	PF[4] SCK_B PCS_A[1] PCS_C[2]	84	00 01 10 11	Port F GPIO DSPI_B Serial Clock DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I/O O O	V_{DDE2}	MH	—	—	M1	M1
PF5	PF[5] SOUT_B PCS_A[2] PCS_C[3]	85	00 01 10 11	Port F GPIO DSPI_B Serial Data Out DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	P2	P2
PF6	PF[6] SIN_B PCS_A[3] PCS_C[5]	86	00 01 10 11	Port F GPIO DSPI_B Serial Data In DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I O O	V_{DDE2}	SH	—	—	N1	N1
PF7	PF[7] PCS_B[0] PCS_C[5] PCS_D[4]	87	00 01 10 11	Port F GPIO DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE2}	SH	—	—	R2	R2

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
MDO11	MDO[11]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	M7
Miscellaneous Pins (9)											
EXTAL	EXTAL EXTCLK	—	—	Main Crystal Oscillator Input External Clock Input	I I	V_{DDSYN}	A	EXTAL		A14	A14
XTAL	XTAL	—	—	Main Crystal Oscillator Output	O	V_{DDSYN}	A	XTAL		A13	A13
TDI	TDI	—	—	JTAG Test Data Input	I	V_{DDE2}	SH	TDI (Pull Up)		J3	J3
TDO	TDO	—	—	JTAG Test Data Output	O	V_{DDE2}	MH	TDO (Pull Up[8])		M3	M3
TMS	TMS	—	—	JTAG Test Mode Select Input	I	V_{DDE2}	MH	TMS (Pull Up)		L3	L3
TCK	TCK	—	—	JTAG Test Clock Input	I	V_{DDE2}	SH	TCK (Pull Down)		P3	P3
JCOMP	JCOMP	—	—	JTAG Compliancy	I	V_{DDE2}	SH	JCOMP (Pull Down)		K3	K3
TEST	TEST	—	—	Test Mode Select	I	V_{DDE3}	IH	TEST[9]		M13	M13
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	—	—	External Reset	I/O	V_{DDE1}	MH	$\overline{\text{RESET}}$ (Pull Up)		A11	A11

1 The primary signal name is used as the pin label on the BGA map for identification purposes.

2 Each line in the Signal Name column corresponds to a separate signal function on the pin. For all device I/O pins, the primary, alternate, or GPIO signal functions are designated in the PA field of the System Integration Unit (SIU) PCR registers except where explicitly noted.

3 The GPIO number is the same as the corresponding pad configuration register (SIU_PCR*n*) number.

4 The PA bitfield in the SIU_PCR*n* register selects the signal function for the pin. A dash in the Description field of this table indicates that this value for PC is reserved on this pin, and should not be used.

5 The pad type is indicated by one or more of the following abbreviations: A–analog, F—fast speed, H–high voltage, I—input-only, M–medium speed, S–slow speed. For example, pad type SH designates a slow high-voltage pad.

6 The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. The terminology used in this column is: O – output, I – input, Up – weak pull up enabled, Down – weak pulldown enabled, Low – output driven low, High – output driven high. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin. The signal name to the left or right of the slash indicates the pin is enabled.

7 The Function After Reset of a GPI function is general purpose input. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin.

8 Pullup is enabled only when JCOMP is negated.

9 Tie to V_{SS} for normal operation.

3.3.1 Power and Ground Supply Summary

Table 3. MPC5668x Power/Ground

Pin Name	Function Description	Voltage[1]	Package Pin Locations	
			208	256
V_{DD}	Internal Logic Power	1.2 V	D4, D10, H4, G13, K13, N5	D4, D10, H4, G13, K13, N5
V_{DDE1}	External I/O Power	3.3–5.0 V	D6	D6
V_{DDE2}			L4	L4
V_{DDE3}			J13	J13
V_{DDE4}			N10	N10
V_{DDA}	Analog Power	3.3–5.0 V	B15	B15
V_{DD33}	3.3 V I/O Power	3.3 V	L13	L13
V_{DDEMLB}	Media Local Bus Power	2.5 or 3.3 V	K4	K4
V_{DDENEX}[2]	Nexus Power	3.3 V	—	E6, K11, L7
V_{RCSEL}	Voltage Regulator Select	V_{SSA} / V_{DDA}	H13	H13
V_{RC}	Voltage Regulator Control Voltage	3.3–5.0 V	B10	B10
V_{RCCTL}	Voltage Regulator Control Output	—[3]	B11	B11
V_{DDSYN}	Clock Synthesizer Power	3.3 V	A12	A12
V_{RH}	Analog High Voltage Reference	3.3–5.0 V	B16	B16
V_{RL}	Analog Low Voltage Reference	0 V	C16	C16
V_{SS}	Ground	0 V	A1, A16, D7, G4, G[7:10], H[7:10], J[7:10], K[7:10], N13, T1, T16	A1, A16, D7, E[7:12], F[7:12], G4, G[6:12], H[7:12], J[7:12], K[6:10], K12, L[8:10], L12, N13, T1, T16
V_{SSA}	Analog Ground	0 V	C15	C15
V_{SSSYN}	Clock Synthesizer Ground	0 V	A15	A15

1 Nominal voltages.

2 Dedicated Nexus power pin on 256-pin package only. On the 208-pin package, VDDENEX is tied to VSS internal to the package substrate and is not available externally.

3 Base current to external NPN power transistor. Voltage may vary.

7 All functional non-supply I/O pins are clamped to V_{SS} and V_{DDEx}.

8 V_{DDEx} are separate power segments and may be powered independently with no differential voltage constraints between the power segments.

9 AC signal over and undershoot of the input voltages of up to ±2.0 V is permitted for a cumulative duration of 60 hours over the complete lifetime of the device (injection current does not need to be limited for this duration).

10 Internal structures will hold the input voltage above –1.0 V if the injection current limit of 2 mA is met.

11 Internal structures hold the input voltage below this maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (25 mA for all pins) and V_{DDE} is within Operating Voltage specifications.

12 Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

13 Total injection current for all analog input pins must not exceed 15 mA.

14 Solder profile per CDF-AEC-Q100.

15 Moisture sensitivity per JEDEC test method A112.

4.2 Thermal Characteristics

Table 5. Thermal Characteristics

Spec	Characteristic	Symbol	Unit	Value	
				208 MAPBGA	256 MAPBGA
1	Junction to Ambient[1, 2] Natural Convection (Single layer board)	$R_{\theta JA}$	°C/W	39	39
2	Junction to Ambient[1, 3] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	°C/W	24	24
3	Junction to Ambient[1, 3] (@200 ft./min., Single layer board)	$R_{\theta JMA}$	°C/W	31	31
4	Junction to Ambient[1, 3] (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	°C/W	20	20
5	Junction to Board[4]	$R_{\theta JB}$	°C/W	13	13
6	Junction to Case[5]	$R_{\theta JC}$	°C/W	6	6
7	Junction to Package Top[6] Natural Convection	Ψ_{JT}	°C/W	2	2

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

4.3 ESD Characteristics

Table 6. ESD Ratings[1, 2]

Characteristic	Symbol	Value	Unit
ESD for Human Body Model (HBM)		2000	V
HBM Circuit Description	R1	1500	Ohm
	C	100	pF
ESD for Field Induced Charge Model (FDCM)		750 (corner pins)	V
		250 (all other pins)	
Number of Pulses per pin: Positive Pulses (HBM) Negative Pulses (HBM)	 — —	 1 1	 — —
Interval of Pulses	—	1	second

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.4 VRC Electrical Specifications

Table 7. VRC Electrical Specifications

Spec	Characteristic	Symbol	Min	Max	Units
1	Current which can be sourced by V_{RCCTL}	I_V_{RCCTL}	6.25 µA	20 mA	—
2	Minimum Required Gain from external circuit: I_{DD} / I_V_{RCCTL} (@V_{DD} = 1.32 V)[1] –40°C 25°C 150°C	BETA	 50 50 50	 500	

1 Assumes “typical usage” currents which will vary with application.

4.5 DC Electrical Specifications

Table 8. DC Electrical Specifications

Spec	Characteristic	Symbol	Min	Max	Unit
1	Maximum Operating Temperature Range — Die Junction Temperature	T_J	–40.0	150.0	°C
2	3.3 V Clock Synthesizer Voltage[1]	V_{DDSYN}	3.0	3.6	V
3	3.3 V I/O Buffer Voltage[1]	V_{DD33}	3.0	3.6	V
4	3.3–5.0 V Voltage Regulator Reference Voltage[1] V_{RCSEL} = V_{SSA} V_{RCSEL} = V_{DDA}	V_{VRC}	 3.0 4.5	 3.6 5.5	V
5	3.3–5.0 V Analog Supply Voltage	V_{DDA}	maximum of 3.0 V or V_{VRC} – 0.1	5.5	V

2 The maximum frequency value is with frequency modulation disabled. If frequency modulation is enabled, the maximum frequency value should be de-rated by the percentage of modulation enabled so that the maximum frequency is not exceeded.

3 "Loss of Reference Frequency" is the reference frequency detected internally, which transitions the PLL into self clocked mode.

4 This specification applies to the period required for the PLL to re-lock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, lock time will be additive with crystal startup time.

5 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{jitter} + C_{mod}.

6 Modulation depth selected must not result in f_{PLL} value greater than the f_{PLL} maximum specified value.

7 Maximum and minimum variations from programmed modulation depth are 2%, 3%, and 4% peak-to-peak. Use only these settings.

8 Depth tolerance is the programmed modulation depth ±0.25% of f_{SYS}.

9 See the Block Guide for VCO frequency synthesis equations.

10 Modulation rates less than 400 kHz will result in exceedingly long FM calibration durations. Modulation rates greater than 1 MHz will result in reduced calibration accuracy.

4.11 ADC Electrical Characteristics

Table 19. ADC Conversion Specifications (Operating)

Spec	Characteristic	Symbol	Min	Max	Unit
1	Analog High Reference Voltage	V_{RH}	V_{DDA} – 0.5	V_{DDA}	V
2	Analog Low Reference Voltage	V_{RL}	0	0.5	V
3	Analog Input Voltage	AV_{IN}	V_{RL}	V_{RH}	V
4	Sampling Frequency	F_S	—	1.53	MHz
5	Maximum ADC Clock Frequency	F_{MAX}	—	60	MHz
6	Sampling Time V_{DDA} = 3.0 V – 3.6 V V_{DDA} > 3.6 V – 5.5 V	t_S	 250 125	—	ns
7	Differential Non Linearity	DNL	–1.0	1.0	LSB
8	Integral Non Linearity	INL	–1.5	1.5	LSB
9	Offset Error	OFS	–1.0	1.0	LSB
10	Gain Error	GNE	–2.0	2.0	LSB
11	Total Unadjusted Error [1]	TUE	–2.0	2.0	LSB

1 TUE assumes no pin activity on pins adjacent to analog channel or output driver activity on corresponding V_{DDE} segment.

4.12 Flash Memory Electrical Characteristics

Table 20. Flash Program and Erase Specifications[1]

Spec	Characteristic	Symbol	Min	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time[4]	$t_{dwprogram}$	—	—	500	µs
2	Page (128 bits and 256 bits) Program Time[4]	$t_{pprogram}$	—	160	500	µs
3	16 KB Block Pre-program and Erase Time	$t_{16kpperase}$	—	1000	5000	ms
4	64 KB Block Pre-program and Erase Time	$t_{64kpperase}$	—	1800	5000	ms
5	128 KB Block Pre-program and Erase Time	$t_{128kpperase}$	—	2600	7500	ms

Table 23. De-rated Pad AC Specifications (3.3 V, 3.3 V)[1] (continued)

Spec	Pad Type[2]	SRC/DSC[3]	Out Delay[4,5] (ns)	Rise/Fall[6], (ns)	Load Drive (pF)
3	Fast[8]	00	2.5	1.2	10
		01		1.2	20
		10		1.2	30
		11		1.2	50
4	Input	N/A	3/3	1.5/1.5	0.5

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at F_{SYS} = 116 MHz, V_{DD} = 1.08 – 1.32 V, V_{DDE} = 3.0 – 3.6 V, V_{DDEH} = 3.0 – 3.6 V, V_{RC33} and V_{DDPLL} = 3.0 – 3.6 V, $T_A = T_L$ to T_H.

2 Slow = SH or SHA; Medium = MH or MHA; Fast = F; Input = IHA. See Table 2.

3 SRC/DSC are bit fields in the Pad Configuration Registers. SRC—Slew Rate Control (slow and medium pad types only), DSC—Drive Strength Control (fast pad type only).

4 This parameter is supplied for reference and is not guaranteed by design and not tested.

5 Delay and rise/fall are measured to 20% or 80% of the respective signal.

6 This parameter is guaranteed by characterization before qualification rather than 100% tested.

7 Add a maximum of one system clock to the output delay for delay with respect to system clock.

8 Output delay is shown in Figure 6. Add a maximum of one system clock to the output delay for delay with respect to system clock.

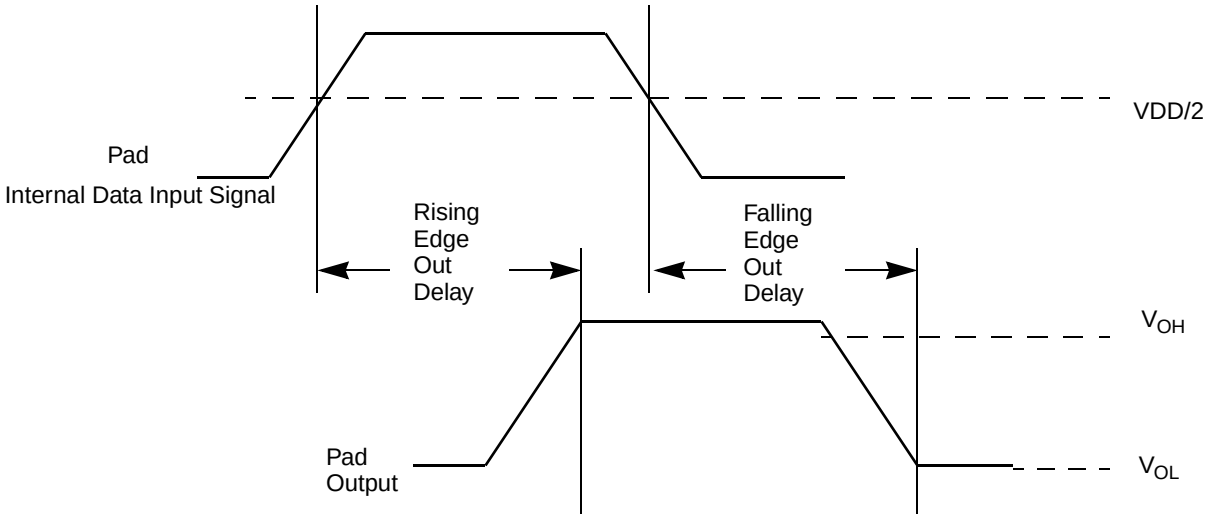


Figure 6. Pad Output Delay

4.14.3 JTAG (IEEE 1149.1) Interface

Table 26. JTAG Interface Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	TCK Cycle Time	t_{JCYC}	100	—	ns
2	TCK Clock Pulse Width (Measured at $V_{DDE}/2$)	t_{JDC}	40	60	ns
3	TCK Rise and Fall Times (40% – 70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI Data Setup Time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI Data Hold Time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK Low to TDO Data Valid	t_{TDOV}	—	25	ns
7	TCK Low to TDO Data Invalid	t_{TDOI}	0	—	ns
8	TCK Low to TDO High Impedance	t_{TDOHZ}	—	20	ns
9	JCOMP Assertion Time	t_{JCMPPW}	100	—	ns
10	JCOMP Setup Time to TCK Low	t_{JCMPS}	40	—	ns
11	TCK Falling Edge to Output Valid	t_{BSDV}	—	50	ns
12	TCK Falling Edge to Output Valid out of High Impedance	t_{BSDVZ}	—	50	ns
13	TCK Falling Edge to Output High Impedance	t_{BSDHZ}	—	50	ns
14	Boundary Scan Input Valid to TCK Rising Edge	t_{BSDST}	50	—	ns
15	TCK Rising Edge to Boundary Scan Input Invalid	t_{BSDHT}	50	—	ns

[1] These specifications apply to JTAG boundary scan only. JTAG timing specified at V_{DDE} = 3.0 – 5.5 V, $T_A = T_L$ to T_H, and C_L = 30 pF with SRC = 0b11.

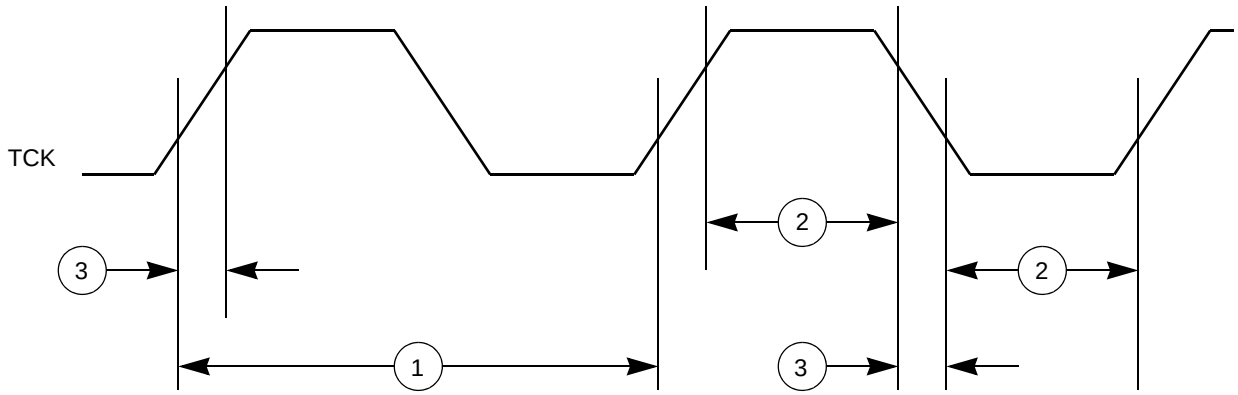


Figure 9. JTAG Test Clock Input Timing

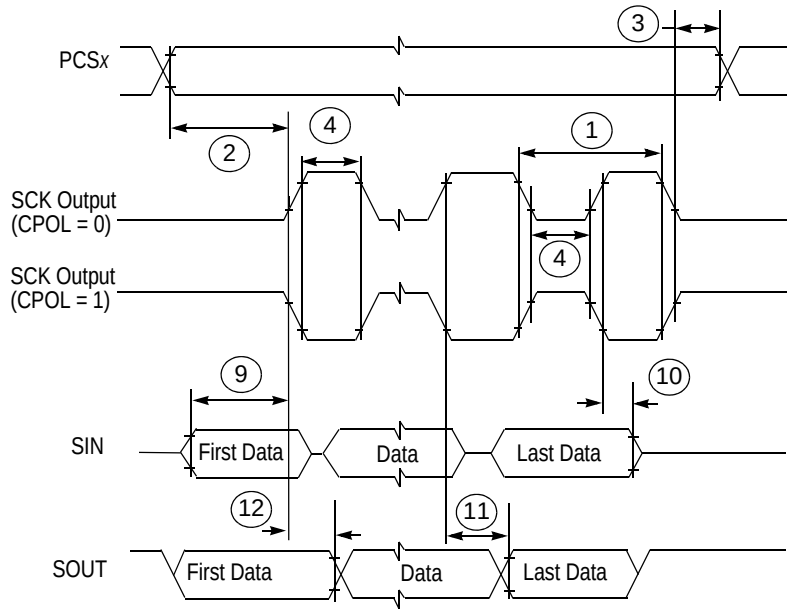


Figure 20. DSPI Modified Transfer Format Timing — Master, CPHA = 0

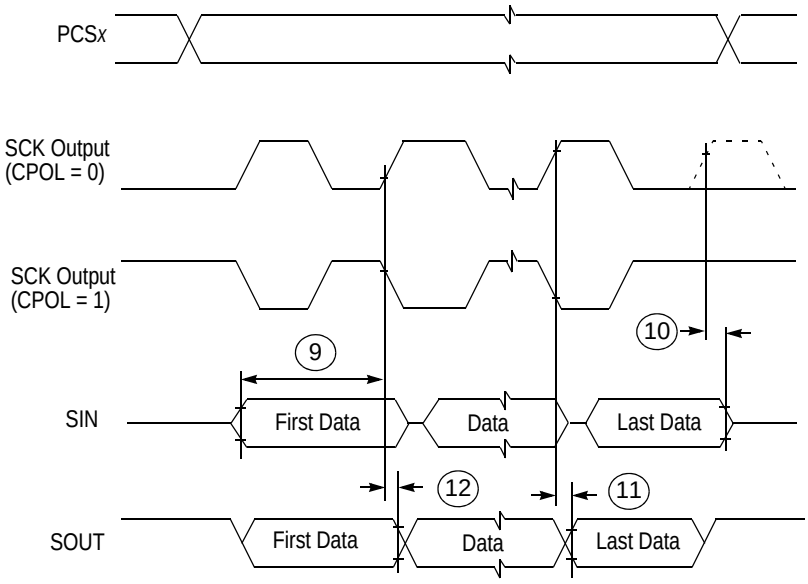


Figure 21. DSPI Modified Transfer Format Timing — Master, CPHA = 1

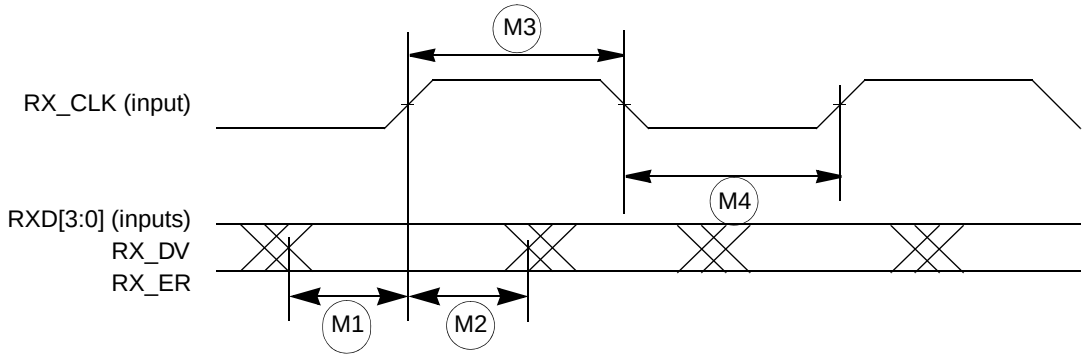


Figure 26. MII Receive Signal Timing Diagram

4.14.8.2 MII Transmit Signal Timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the Ethernet chapter for details of this option and how to enable it.

Table 34. MII Transmit Signal Timing[1]

Spec	Characteristic	Min	Max	Unit
M5	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
M6	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
M7	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	TX_CLK pulse width low	35%	65%	TX_CLK period

1 Output pads configured with SRC = 0b11.

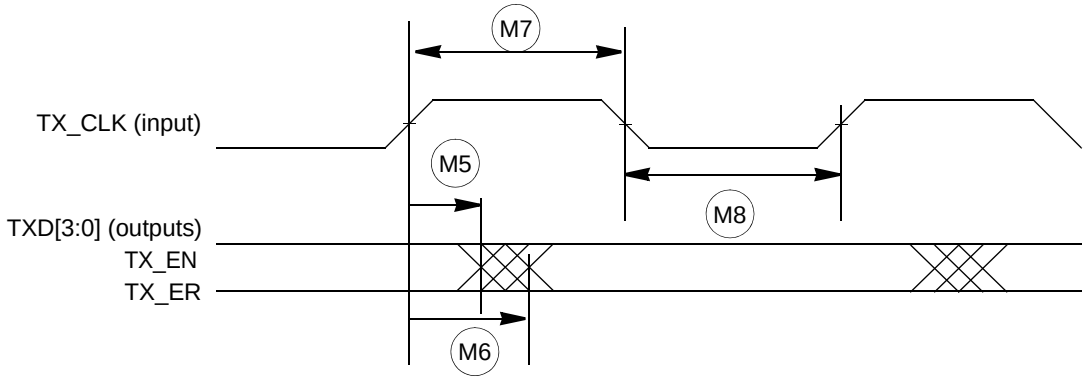


Figure 27. MII Transmit Signal Timing Diagram

4.14.8.3 MII Async Inputs Signal Timing (CRS and COL)

Table 35. MII Async Inputs Signal Timing[1]

Spec	Characteristic	Min	Max	Unit
M9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

1 Output pads configured with SRC = 0b11.

Figure 28. MII Async Inputs Timing Diagram

4.14.8.4 MII Serial Management Channel Timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 36. MII Serial Management Channel Timing[1]

Spec	Characteristic	Min	Max	Unit
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	10	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

1 Output pads configured with SRC = 0b11.

5 Package Characteristics

5.1 Package Mechanical Data

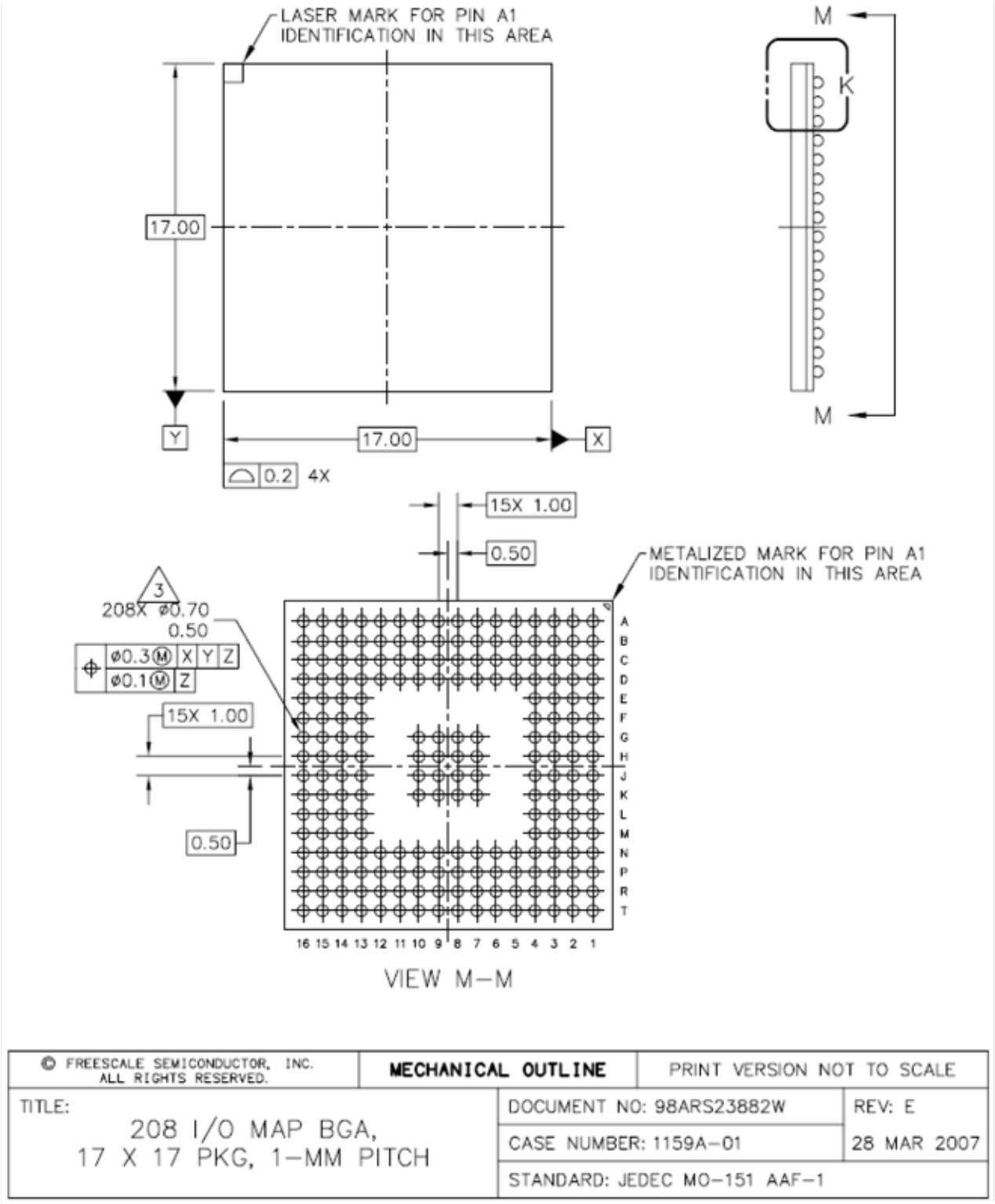
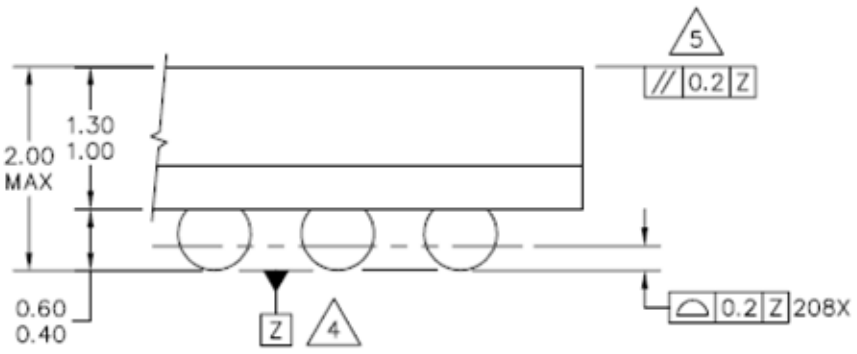


Figure 30. 208 MAPBGA Package Mechanical Drawing



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. PACKAGE CODE SUMMARY:
   MAP BGA: 5253
   MAP BGA PGE DIE: 5371

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TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	DOCUMENT NO: 98ARS23882W	REV: E
	CASE NUMBER: 1159A–01	28 MAR 2007
	STANDARD: JEDEC MO–151 AAF–1	

Figure 31. 208 MAPBGA Package Detail

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