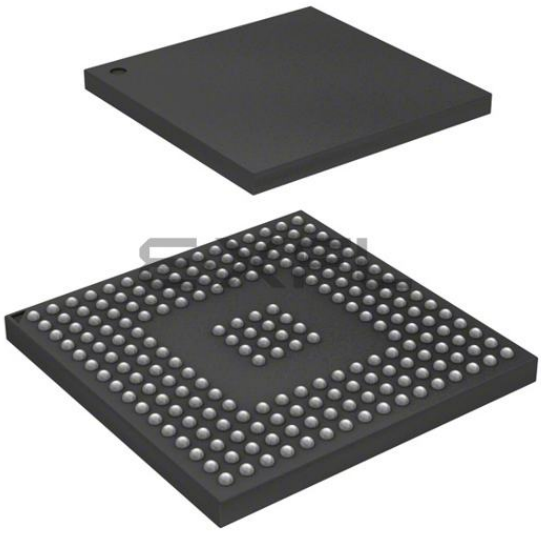

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3.2 256-ball MAPBGA Pin Assignments

Figure 4 shows the 256-ball MAPBGA pin assignments.

256 MAPBGA Ball Map

(as viewed from top through the package)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	V_{SS}	PD0	PG1	PC12	PC9	PC7	PC2	PB13	PB10	PB8	RESET	V_{DDSYN}	XTAL	EXTAL	V_{SSSYN}	V_{SS}	A
B	PD2	PD1	PG0	PC11	PC10	PC8	PC3	PB14	PB11	V_{RC}	V_{RCCTL}	PB9	PB2	PB0	V_{DDA}	V_{RH}	B
C	PD3	PD4	PD14	PC14	PC13	PC5	PC6	PC1	PB15	PB12	PB6	PB4	PB3	PB1	V_{SSA}	V_{RL}	C
D	PD5	PD6	PD15	V_{DD}	PC15	V_{DDE1}	V_{SS}	PC4	PC0	V_{DD}	PB7	PB5	PA10	PA12	PA0	PA14	D
E	PD7	PD8	PE0	PE1	MDO0	V_{DDENEX}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	PA11	PA9	PA1	PA15	E
F	PD9	PD10	PE3	PE2	MDO1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	PA13	PA8	PA3	PA2	F
G	PD11	PD12	PE4	V_{SS}	MDO2	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	PA7	PA5	PA4	G
H	PD13	PF0	PE5	V_{DD}	MDO3	MDO4	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{RCSEL}	PG2	PG6	PA6	H
J	PF1	PF2	TDI	PE8	MDO6	MDO5	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDE3}	PG3	PG7	PG11	J
K	PK1	PK2	JCOMP	V_{DDEMLB}	MDO7	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDENEX}	V_{SS}	V_{DD}	PG4	PG8	PG12	K
L	PK0	PE7	TMS	V_{DDE2}	MDO8	V_{SS}	V_{DDENEX}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD33}	PG5	PG9	PG13	L
M	PF4	PE6	TDO	PE9	MDO9	MDO10	MDO11	MSEO1	MSEO0	MCKO	EVTI	EVTO	TEST	PF13	PG10	PG14	M
N	PF6	PF3	PE10	PE11	V_{DD}	PE15	PE14	PH9	PH11	V_{DDE4}	PH15	PJ10	V_{SS}	PF12	PH3	PG15	N
P	PF8	PF5	TCK	PE12	PE13	PK10	PH8	PH10	PH12	PH13	PH14	PJ11	PF15	PF14	PH4	PH1	P
R	PF10	PF7	PF11	PK4	PK6	PK8	PJ0	PJ2	PJ4	PJ6	PJ9	PJ12	PJ14	PH5	PH6	PH2	R
T	V_{SS}	PF9	PK3	PK5	PK7	PK9	PJ1	PJ3	PJ5	PJ7	PJ8	PJ13	PJ15	PH0	PH7	V_{SS}	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 4. MPC5668x 256-ball MAPBGA (full diagram)

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PC4	PC[4] AN[36]	36	00 01 10 11	Port C GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	D8	D8
PC5	PC[5] AN[37] Z6NMI	37	00 01 10 11	Port C GPIO ADC Analog Input Z6 Core Non-Maskable Interrupt —	I/O I I —	V_{DDE1}	SHA	—	—	C6	C6
PC6	PC[6] AN[38] Z0NMI	38	00 01 10 11	Port C GPIO ADC Analog Input Z0 Core Non-Maskable Interrupt —	I/O I I —	V_{DDE1}	SHA	—	—	C7	C7
PC7	PC[7] AN[39] FR_DBG3	39	00 01 10 11	Port C GPIO ADC Analog Input FlexRay Debug —	I/O I O —	V_{DDE1}	SHA	—	—	A6	A6
PC8	PC[8] AN[40] FR_DBG2	40	00 01 10 11	Port C GPIO ADC Analog Input FlexRay Debug —	I/O I O —	V_{DDE1}	SHA	—	—	B6	B6
PC9	PC[9] AN[41] FR_DBG1	41	00 01 10 11	Port C GPIO ADC Analog Input FlexRay Debug —	I/O I O —	V_{DDE1}	SHA	—	—	A5	A5
PC10	PC[10] AN[42] FR_DBG0	42	00 01 10 11	Port C GPIO ADC Analog Input FlexRay Debug —	I/O I O —	V_{DDE1}	SHA	—	—	B5	B5
PC11	PC[11] AN[43] SCL_C —	43	00 01 10 11	Port C GPIO ADC Analog Input I^2C_C Serial Clock —	I/O I I/O —	V_{DDE1}	SHA	—	—	B4	B4
PC12	PC[12] AN[44] SDA_C —	44	00 01 10 11	Port C GPIO ADC Analog Input I^2C_C Serial Data —	I/O I I/O —	V_{DDE1}	SHA	—	—	A4	A4
PC13	PC[13] AN[45] — MA[0]	45	00 01 10 11	Port C GPIO ADC Analog Input — ADC Ext. Mux Address Select	I/O I — O	V_{DDE1}	SHA	—	—	C5	C5
PC14	PC[14] AN[46] MA[1] —	46	00 01 10 11	Port C GPIO ADC Analog Input ADC Ext. Mux Address Select —	I/O I — O	V_{DDE1}	SHA	—	—	C4	C4

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PE14	PE[14] SCL_A PCS_D[2]	78	00 01 10 11	Port E GPIO I^2C_A Serial Clock DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE2}	SH	—	—	N7	N7
PE15	PE[15] SDA_A PCS_D[5]	79	00 01 10 11	Port E GPIO I^2C_A Serial Data DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE2}	SH	—	—	N6	N6
Port F (16)											
PF0	PF[0] SCK_A	80	00 01 10 11	Port F GPIO DSPI_A Serial Clock — —	I/O I/O — —	V_{DDE2}	MH	—	—	H2	H2
PF1	PF[1] SOUT_A	81	00 01 10 11	Port F GPIO DSPI_A Serial Data Out — —	I/O O — —	V_{DDE2}	MH	—	—	J1	J1
PF2	PF[2] SIN_A	82	00 01 10 11	Port F GPIO DSPI_A Serial Data In — —	I/O I — —	V_{DDE2}	SH	—	—	J2	J2
PF3	PF[3] PCS_A[0] PCS_B[5] PCS_C[4]	83	00 01 10 11	Port F GPIO DSPI_A Peripheral Chip Select DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I/O O O	V_{DDE2}	SH	—	—	N2	N2
PF4	PF[4] SCK_B PCS_A[1] PCS_C[2]	84	00 01 10 11	Port F GPIO DSPI_B Serial Clock DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I/O O O	V_{DDE2}	MH	—	—	M1	M1
PF5	PF[5] SOUT_B PCS_A[2] PCS_C[3]	85	00 01 10 11	Port F GPIO DSPI_B Serial Data Out DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	P2	P2
PF6	PF[6] SIN_B PCS_A[3] PCS_C[5]	86	00 01 10 11	Port F GPIO DSPI_B Serial Data In DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I O O	V_{DDE2}	SH	—	—	N1	N1
PF7	PF[7] PCS_B[0] PCS_C[5] PCS_D[4]	87	00 01 10 11	Port F GPIO DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE2}	SH	—	—	R2	R2

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PG13	PG[13] eMIOS[2] FEC_TXD[1] AN[61]	109	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	L16	L16
PG14	PG[14] eMIOS[1] FEC_TXD[2] AN[62]	110	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	M16	M16
PG15	PG[15] eMIOS[0] FEC_TXD[3] AN[63]	111	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	N16	N16
Port H (16)											
PH0	PH[0] eMIOS[31] FEC_COL	112	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Collision —	I/O I/O I —	V_{DDE3}	SH	—	—	T14	T14
PH1	PH[1] eMIOS[30] FEC_RX_DV	113	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data Valid —	I/O I/O I —	V_{DDE3}	SH	—	—	P16	P16
PH2	PH[2] eMIOS[29] FEC_TX_EN	114	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Transmit Enable —	I/O I/O O —	V_{DDE3}	MH	—	—	R16	R16
PH3	PH[3] eMIOS[28] FEC_RX_ER	115	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Error —	I/O I/O I —	V_{DDE3}	SH	—	—	N15	N15
PH4	PH[4] eMIOS[27] FEC_RXD[0]	116	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	P15	P15
PH5	PH[5] eMIOS[26] FEC_RXD[1]	117	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	R14	R14
PH6	PH[6] eMIOS[25] FEC_RXD[2]	118	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	R15	R15

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PJ1	PJ[1] eMIOS[14] PCS_A[5]	129	00 01 10 11	Port J GPIO eMIOS Channel DSPI_A Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T7	T7
PJ2	PJ[2] eMIOS[13] PCS_B[1]	130	00 01 10 11	Port J GPIO eMIOS Channel DSPI_B Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	R8	R8
PJ3	PJ[3] eMIOS[12] PCS_B[2]	131	00 01 10 11	Port J GPIO eMIOS Channel DSPI_B Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T8	T8
PJ4	PJ[4] eMIOS[11] PCS_C[3]	132	00 01 10 11	Port J GPIO eMIOS Channel DSPI_C Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	R9	R9
PJ5	PJ[5] eMIOS[10] PCS_C[4]	133	00 01 10 11	Port J GPIO eMIOS Channel DSPI_C Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T9	T9
PJ6	PJ[6] eMIOS[09] PCS_D[5]	134	00 01 10 11	Port J GPIO eMIOS Channel DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	R10	R10
PJ7	PJ[7] eMIOS[08] PCS_D[1]	135	00 01 10 11	Port J GPIO eMIOS Channel DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T10	T10
PJ8	PJ[8] eMIOS[07]	136	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	T11	T11
PJ9	PJ[9] eMIOS[06]	137	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	R11	R11
PJ10	PJ[10] eMIOS[05]	138	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	N12	N12
PJ11	PJ[11] eMIOS[04]	139	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	P12	P12

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PJ12	PJ[12] eMIOS[03]	140	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	R12	R12
PJ13	PJ[13] eMIOS[02]	141	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	T12	T12
PJ14	PJ[14] eMIOS[01]	142	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	R13	R13
PJ15	PJ[15] eMIOS[00]	143	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	T13	T13
Port K (11)											
PK0	PK[0] MLBCLK SCK_B CLKOUT	144	00 01 10 11	Port K GPIO Media Local Bus Clock DSPI_B Serial Clock CLKOUT (Test Only)	I/O I I/O O	V_{DDEMLB}	F	—	—	L1	L1
PK1	PK[1] MLBSIG SOUT_B PCS_D[4]	145	00 01 10 11	Port K GPIO Media Local Bus Signal DSPI_B Serial Data Out DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDEMLB}	F	—	—	K1	K1
PK2	PK[2] MLBDAT SIN_B PCS_D[5]	146	00 01 10 11	Port K GPIO Media Local Bus Data DSPI_B Serial Data In DSPI_D Peripheral Chip Select	I/O I/O I O	V_{DDEMLB}	F	—	—	K2	K2
PK3	PK[3] FR_A_RX MA[0] PCS_C[1]	147	00 01 10 11	Port K GPIO FlexRay A Receive Data ADC Ext. Mux Address Select DSPI_C Peripheral Chip Select	I/O I O O	V_{DDE2}	SH	—	—	T3	T3
PK4	PK[4] FR_A_TX MA[1] PCS_C[2]	148	00 01 10 11	Port K GPIO FlexRay A Transmit Data ADC Ext. Mux Address Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	R4	R4
PK5	PK[5] FR_A_TX_EN MA[2] PCS_C[3]	149	00 01 10 11	Port K GPIO FlexRay A Transmit Enable ADC Ext. Mux Address Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	T4	T4

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for either hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 4}$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

Table 8. DC Electrical Specifications

Spec	Characteristic	Symbol	Min	Max	Unit
6	3.3–5.0 V External I/O Supply Voltage[2] V_{DDE1} V_{DDE2} V_{DDE3} V_{DDE4}		 3.0 3.0 3.0 3.0	 5.5 5.5 5.5 5.5	V
7	2.5 V – 3.3 V External I/O Supply Voltage (MLB)	V_{DDEMLB}[3]	2.375	3.6	V
8	3.3 V External I/O Supply Voltage (Nexus)	V_{DDENEX}	3.0	3.6	V
9	Pad Input High Voltage Hysteresis enabled Hysteresis disabled (IHA/SH/SHA/MH/MHA)[4, 5] Hysteresis disabled (F)	V_{IH}	 0.65 × V_{DDE} 0.55 × V_{DDE} 0.55 × V_{DDE}	V_{DDE} + 0.3	V
10	Pad Input Low Voltage Hysteresis enabled Hysteresis disabled (IHA/SH/SHA/MH/MHA)[4, 5] Hysteresis disabled (F)	V_{IL}	V_{SS} – 0.3	 0.35 × V_{DDE} 0.40 × V_{DDE} 0.40 × V_{DDE}	V
11	Pad Input Hysteresis	V_{HYS}	0.1 × V_{DDE}		V
12	Analog (IHA) Input Voltage	V_{INDC}	V_{SSA} – 0.3	V_{DDA} + 0.3	V
13	Pad Output High Voltage[6, 7, 8]	V_{OH}	0.8 × V_{DDE}	—	V
14	Pad Output Low Voltage[8]	V_{OL}	—	0.2 × V_{DDE}	V
15	Input Capacitance (Digital Pins: Pad type F, MH, SH)[4]	C_{IN}	—	7	pF
16	Input Capacitance (Analog Pins: Pad type IHA)[4, 5]	C_{IN_A}	—	10	pF
17	Input Capacitance (Shared digital/analog pins: MHA, SHA)[4]	C_{IN_M}	—	12	pF
18	I/O Weak Pull Up/Down Absolute Current[4, 9] Pad F: 2.375 V – 3.6 V Pad SH/MH/IHA: 3.0 V – 3.6 V Pad SH/MH/IHA: 4.5 V – 5.5 V	I_{ACT}	 25 10 35	 180 95 200	µA
19	I/O Input Leakage Current[10]	I_{INACT_D}	–2.5	2.5	µA
20	DC Injection Current (per pin)	I_{IC}	–1.0	1.0	mA
21	Analog Input Current, Channel Off[11] (Analog pins IHA)[4, 5]	I_{INACT_A}	–150	150	nA
22	Analog Reference High Voltage	V_{RH}	V_{DDA} – 500	V_{DDA}	mV
23	Analog Reference Low Voltage	V_{RL}	V_{SSA}	V_{SSA} + 500	mV
24	V_{SS} to V_{SSA} Differential Voltage	$V_{SS} – V_{SSA}$	–100	100	mV
25	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} – V_{SS}$	–100	100	mV
26	Slew rate on V_{DDA}, V_{DDEx}, V_{DDSYN}, V_{DD33}, and V_{RC} power supply pins	V_{Ramp}	—	100	V/ms
27	Capacitive Supply Load (V_{DD})	V_{Load}	8	—	µF
28	Capacitive Supply Load (V_{DD33}, V_{DDSYN})	V_{Load}	1	—	µF

1 When V_{RCSEL} = V_{SSA} (low), V_{DDSYN} and V_{DD33} are externally supplied. When V_{RCSEL} = V_{DDA} (high), V_{DDSYN} and V_{DD33} are generated by internal voltage regulators. When V_{RCSEL} = V_{SSA} (low), V_{DDSYN} and V_{DD33} cannot be 100 mV higher than V_{RC}.

2 $V_{DDE1} – V_{DDE4}$ are separate power segments and may be powered independently with no differential voltage constraints between the power segments. $V_{DDE1} – V_{DDE3}$ pad power segments contain ADC analog input channels and thus the input analog signal level may be clamped to the V_{DDE} level, resulting in inaccurate ADC results if the V_{DDE} voltage level is less than V_{DDA}.

3 When $V_{RCSEL} = V_{DDA}$ (high), the internally generated V_{DD33} voltage may be used to power V_{DDEMLB} as long as the PK[0:2] pads remain in the disabled default state with their output buffers, input buffers, and pull devices disabled.

4 The pad type is indicated by one or more of the following abbreviations: A–analog, F—fast speed, H–high voltage, I—input-only, M–medium speed, S–slow speed. For example, pad type SH designates a slow high-voltage pad.

5 The IHA pads are related to V_{DDA}.

6 Characterization Based Capability:
IOH_F = {12, 20, 30, 40} mA and IOL_F = {24, 40, 50, 65} mA for {00, 01,10, 11} drive mode with V_{DDE} = 3.0 V;
IOH_F = {7, 13, 18, 25} mA and IOL_F = {18, 30, 35, 50} mA for {00, 01, 10, 11} drive mode with V_{DDE} = 2.25 V;
IOH_F = {3, 7, 10, 15} mA and IOL_F = {12, 20, 27, 35} mA for {00, 01, 10, 11} drive mode with V_{DDE} = 1.62 V.

7 Characterization Based Capability:
IOH_S = {6, 11.6} mA and IOL_S = {9.2, 17.7} mA for {slow, medium} I/O with V_{DDEH} = 4.5 V;
IOH_S = {2.8, 5.4} mA and IOL_S = {4.2, 8.1} mA for {slow, medium} I/O with V_{DDEH} = 3.0 V

8 All V_{OL}/V_{OH} values 100% tested with ±2 mA load.

9 Absolute value of current, measured at V_{IL} and V_{IH}.

10 Weak pull up/down inactive. Measured at V_{DDE} = 5.25 V. Applies to pad types: SH and MH. Leakage specification guaranteed only when power supplies are within specified operating conditions.

11 Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to pad types: pad_a and pad_ae.

4.6 Operating Current Specifications

Table 9. Operating Currents

Spec	Characteristic	Symbol	Typ[1] 25 °C Ambient	Max[1] –40–150 °C Junction	Unit
Equations	$I_{TOTAL} = I_{DDE} + I_{DDA} + I_{RH} + I_{DD33} + I_{DDSYN} + I_{RC} + I_{DD}$ $I_{DDE} = I_{DDE1} + I_{DDE2} + I_{DDE3} + I_{DDE4} + I_{DDEMLB}$	—	—	—	—
1	V_{DDE} Current $V_{DDE(1,2,3,4)}$ @ 3.0 V – 5.5 V V_{DDEMLB} @ 2.375 V – 3.6 V Static[2] Dynamic[3]	I_{DDE}	 0 Note 3	 30 25	 µA mA
2	V_{DDA} Current V_{DDA} @ 3.0 V – 5.5 V Run mode Sleep mode – Optional 32 kHz osc enabled	I_{DDA}	 1 20 +5	 30 50 +15	 mA µA µA
3	V_{RH} Current V_{RH} @ 3.0 V – 5.5 V Run mode Sleep mode	I_{RH}	 300 1	 700 30	 µA µA
4	V_{DD33} Current V_{DD33} @ 3.0 V – 3.6 V Run mode Sleep mode	I_{DD33}	 10 10	 20 20	 mA µA

4.7 I/O Pad Current Specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 10 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 10.

Table 10. I/O Pad Average I_{DDE} Specifications[1]

Spec	Pad Type[2]	Symbol	Period (ns)	Load[3] (pF)	V_{DDE} (V)	Drive/Slew Rate Select	I_{DDE} Avg (mA)	I_{DDE} RMS (mA)
1	Slow	$I_{DRV\_SSR\_HV}$	37	50	5.5	11	14	
2			130	50	5.5	01	5.3	
3			650	50	5.5	00	1.1	
4			840	200	5.5	00	3	
6	Medium	$I_{DRV\_MSR\_HV}$	24	50	5.5	11	9	
7			62	50	5.5	01	2.5	
8			317	50	5.5	00	0.5	
9			425	200	5.5	00	1.5	
11	Fast	I_{DRV_FC}	10	50	3.6	11	50.4	101.6
12			10	30	3.6	10	14.2	57.3
13			10	20	3.6	01	16.4	43.6
14			10	10	3.6	00	9.8	15.9
15			10	50	2.75	11	22.9	45.3
16			10	30	2.75	10	6.7	25.3
17			10	20	2.75	01	4.5	17.3
18			10	10	2.75	00	3	9.6
19	Input	$I_{DRV\_I\_HV}$	7	0.5	5.5	N/A	N/A	N/A

1 These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

2 Slow = SH or SHA; Medium = MH or MHA; Fast = F; Input = IHA. See Table 2.

3 All loads are lumped.

Table 14. 3.3 V High Frequency External Oscillator (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
8	Crystal manufacturer's recommended capacitive load	C_L	See crystal specification	See crystal specification	pF
9	Discrete load capacitance to be connected to EXTAL	C_{L_EXTAL}	—	$2\times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$[5]	pF
10	Discrete load capacitance to be connected to XTAL	C_{L_XTAL}	—	$2\times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$[5]	pF
11	Startup Time	$t_{startup}$	—	10	ms

1 When PLL frequency modulation is active, reference frequencies less than 8 MHz will distort the modulated waveform and the effects of this on emissions is not characterized.

2 This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case, $V_{extal} - V_{xtal} \geq 400$ mV criteria has to be met for oscillator's comparator to produce output clock.

3 This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case, $V_{xtal} - V_{extal} \geq 400$ mV criteria has to be met for oscillator's comparator to produce output clock.

4 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

5 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

Table 15. 5 V Low Frequency (32 kHz) External Oscillator

Spec	Characteristic	Symbol	Min	Max	Unit
1	Frequency Range	f_{ref32}	32	40	kHz
2	Duty Cycle of reference	t_{dc32}	40	60	%
3	XTAL32 Current[1]	I_{XTAL32}	—	3	µA
4	Crystal manufacturer's recommended capacitive load	C_{L32}	See crystal specification	See crystal specification	pF
5	Startup Time	$t_{Startup}$	—	2	s

1 I_{xtal32} is the oscillator bias current out of the XTAL32 pin with both EXTAL32 and XTAL32 pins grounded.

Table 16. 5 V High Frequency (16 MHz) Internal RC Oscillator

Spec	Characteristic	Symbol	Range	Min	Typ	Max	Unit
1	Frequency before trim[1]	f_{ut}	35%	10.4	16	21.6	MHz
2	Frequency after loading factory trim[2]	f_t	7%	14.9	16	17.1	MHz
3	Application trim resolution[3]	t_s	—	—	—	±0.5	%
4	Application frequency trim step[3]	f_s	—	—	300	—	kHz
5	Startup Time	$t_{Startup}$	—	—	—	500	ns

1 Across process, voltage, and temperature.

2 Across voltage and temperature.

3 Fixed voltage and temperature.

4.14 AC Timing

4.14.1 Reset and Boot Configuration Pins

Table 24. Reset and Boot Configuration Timing

Spec	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	150	—	ns
2	BOOTCFG Setup Time after $\overline{\text{RESET}}$ Valid	t_{RCSU}	—	100	µs
3	BOOTCFG Hold Time from $\overline{\text{RESET}}$ Valid	t_{RCH}	0	—	µs

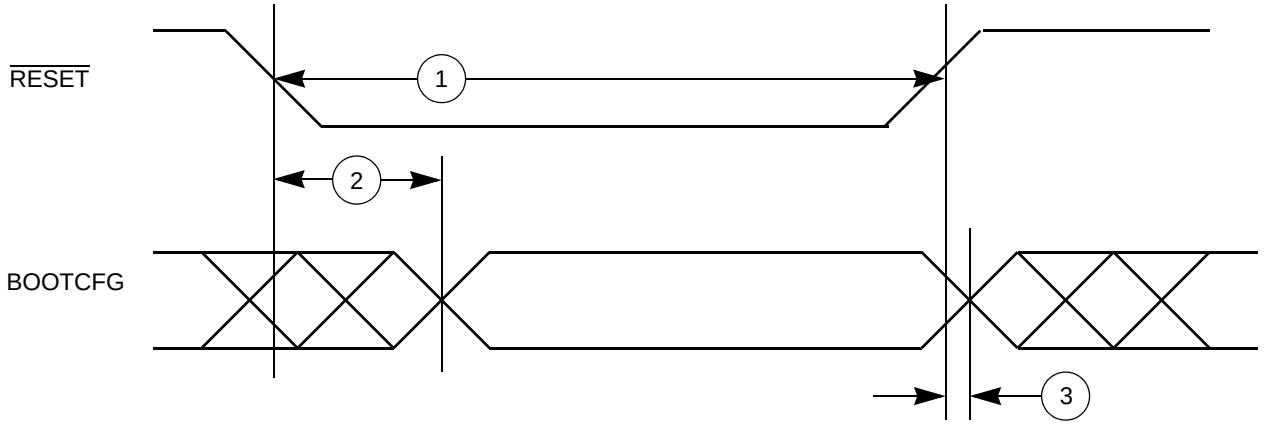

Figure 7. Reset and Boot Configuration Timing

4.14.2 External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) Pins

Table 25. IRQ/NMI Timing

Spec	Characteristic	Symbol	Min	Max	Unit
1	IRQ/NMI Pulse Width Low	t_{IPWL}	3	—	t_{SYS}
2	IRQ/NMI Pulse Width High	T_{IPWH}	3	—	t_{SYS}
3	IRQ/NMI Edge to Edge Time[1]	t_{ICYC}	6	—	t_{SYS}

[1] Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

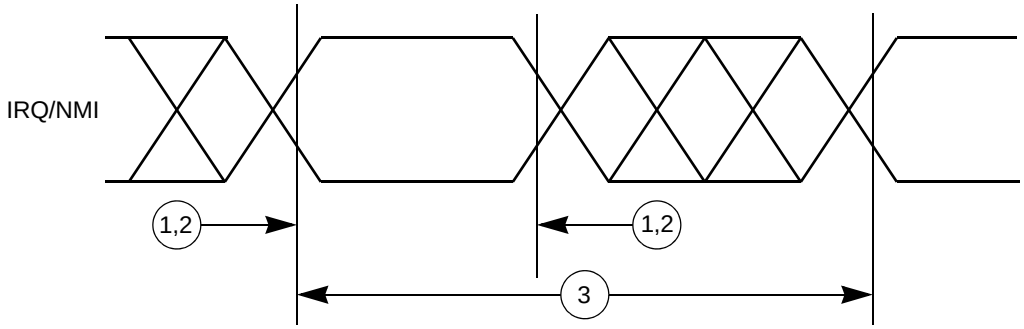

Figure 8. IRQ and NMI Timing

4.14.3 JTAG (IEEE 1149.1) Interface

Table 26. JTAG Interface Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	TCK Cycle Time	t_{JCYC}	100	—	ns
2	TCK Clock Pulse Width (Measured at $V_{DDE}/2$)	t_{JDC}	40	60	ns
3	TCK Rise and Fall Times (40% – 70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI Data Setup Time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI Data Hold Time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK Low to TDO Data Valid	t_{TDOV}	—	25	ns
7	TCK Low to TDO Data Invalid	t_{TDOI}	0	—	ns
8	TCK Low to TDO High Impedance	t_{TDOHZ}	—	20	ns
9	JCOMP Assertion Time	t_{JCMPPW}	100	—	ns
10	JCOMP Setup Time to TCK Low	t_{JCMPS}	40	—	ns
11	TCK Falling Edge to Output Valid	t_{BSDV}	—	50	ns
12	TCK Falling Edge to Output Valid out of High Impedance	t_{BSDVZ}	—	50	ns
13	TCK Falling Edge to Output High Impedance	t_{BSDHZ}	—	50	ns
14	Boundary Scan Input Valid to TCK Rising Edge	t_{BSDST}	50	—	ns
15	TCK Rising Edge to Boundary Scan Input Invalid	t_{BSDHT}	50	—	ns

[1] These specifications apply to JTAG boundary scan only. JTAG timing specified at V_{DDE} = 3.0 – 5.5 V, $T_A = T_L$ to T_H, and C_L = 30 pF with SRC = 0b11.

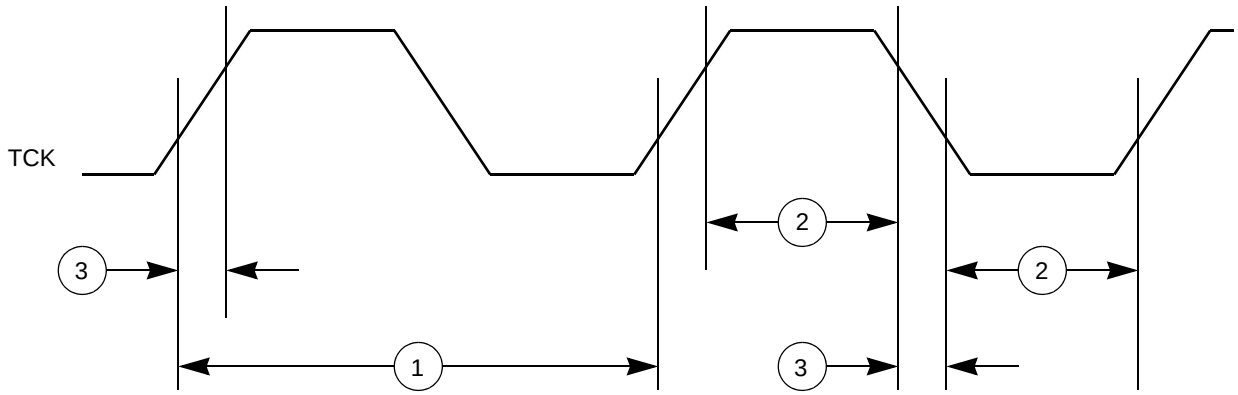

Figure 9. JTAG Test Clock Input Timing

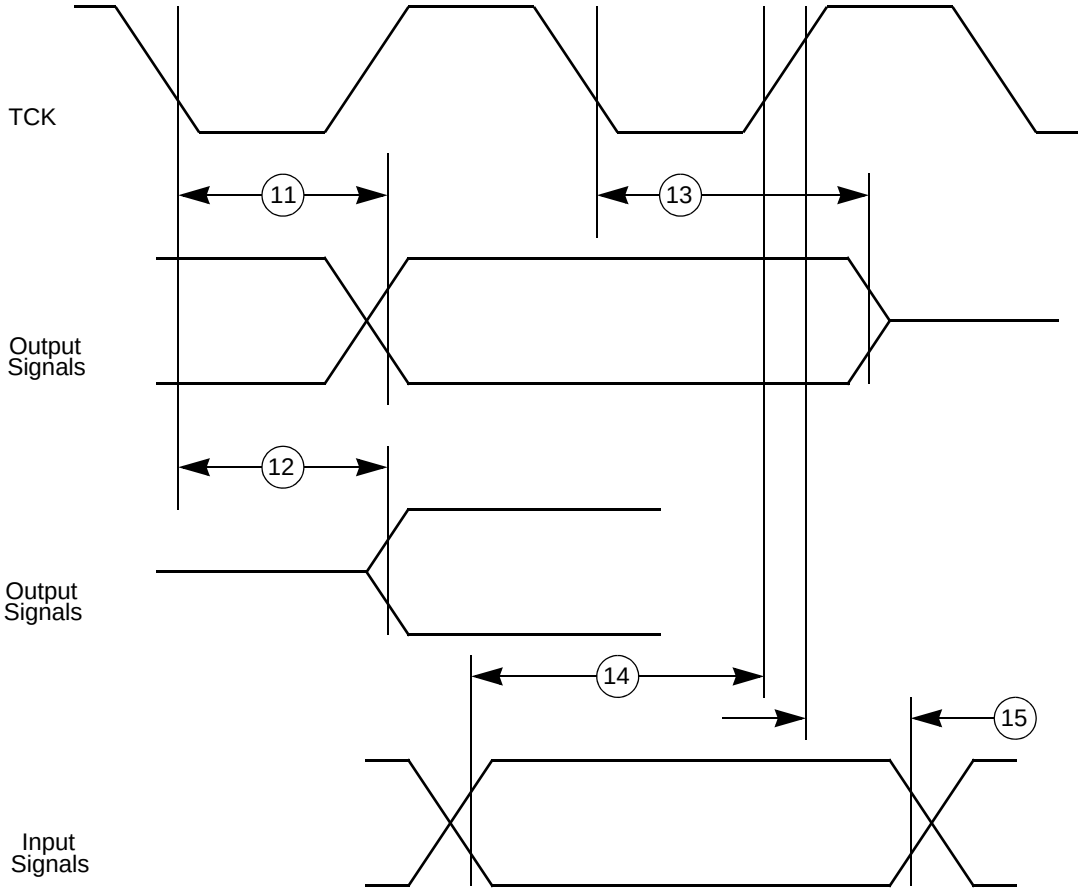

Figure 12. JTAG Boundary Scan Timing

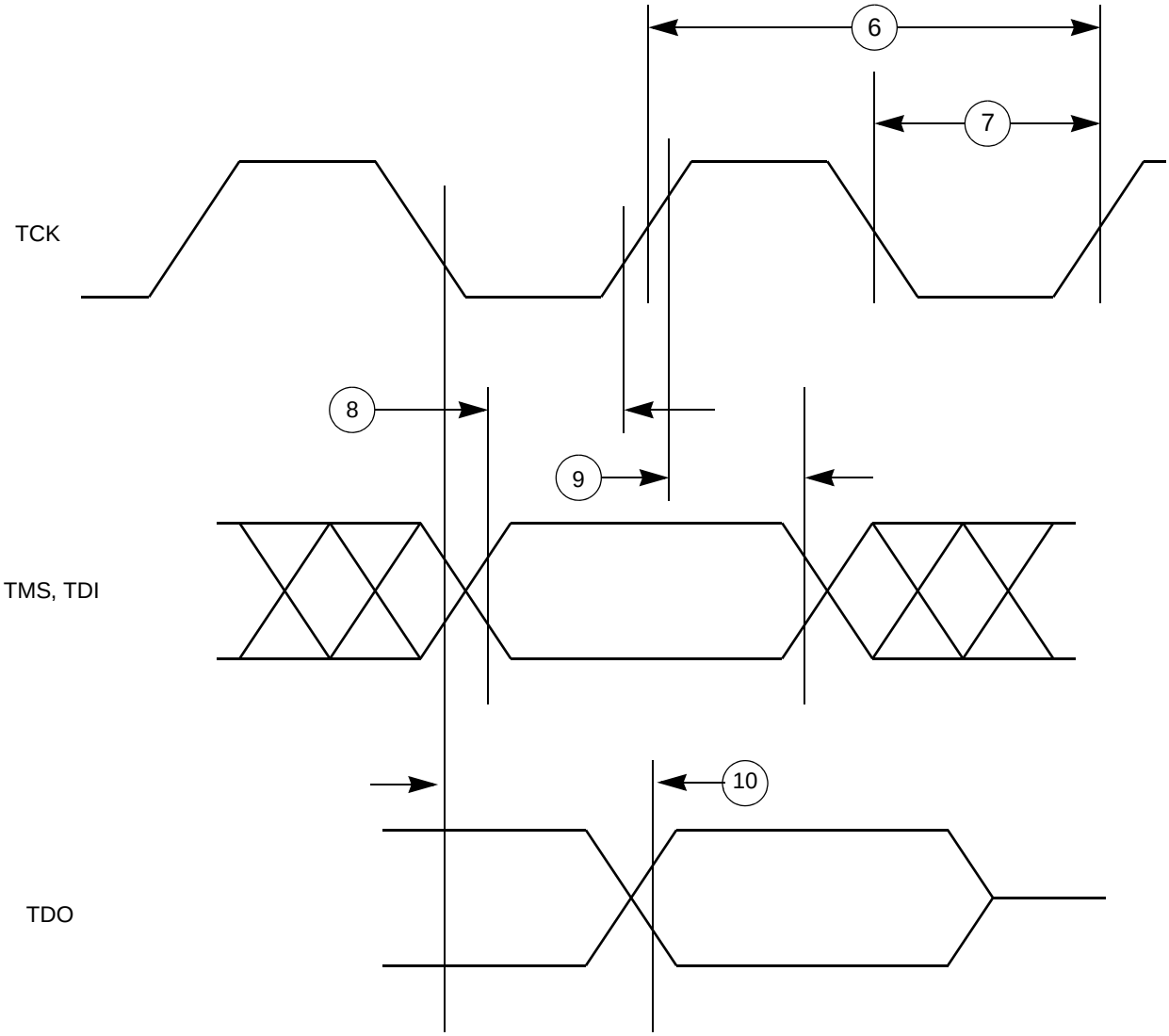

Figure 14. Nexus TDI, TMS, TDO Timing

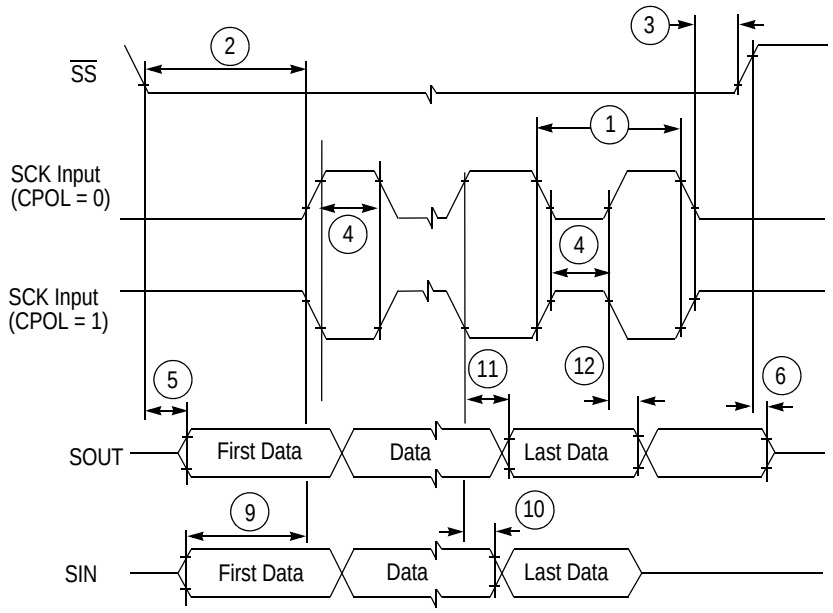

Figure 22. DSPI Modified Transfer Format Timing — Slave, CPHA = 0

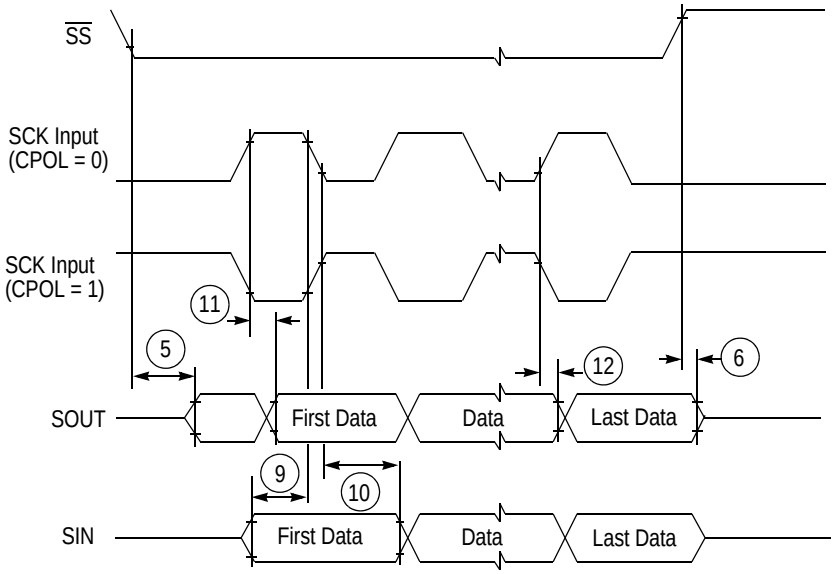

Figure 23. DSPI Modified Transfer Format Timing — Slave, CPHA = 1

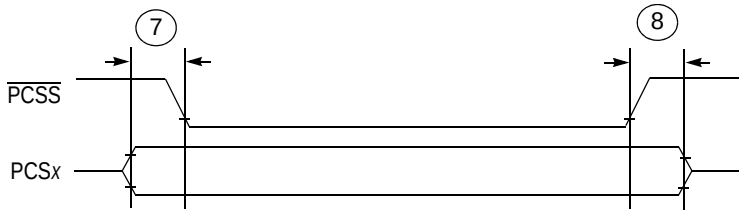

Figure 24. DSPI PCS Strobe ($\overline{\text{PCSS}}$) Timing

4.14.7 MLB Interface

4.14.7.1 Media Local Bus DC Electrical Characteristics

Table 30 provides the DC electrical characteristics for the Media Local Bus interface.

Table 30. Media Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Maximum Input Voltage	—	—	—	3.6	V	
Low Level Input Threshold	V_{IL}	—	—	0.7	V	
High Level Input Threshold	V_{IH}	1.8[1]	—	—	V	
Low Level Output Threshold	V_{OL}	—	—	0.4	V	I_{OL} = 6 mA
High Level Output Threshold	V_{OH}	2.0	—	—	V	I_{OH} = –6 mA
Input Leakage Current	I_L	—	—	±1	µA	$0 < V_{in} < V_{DDE4}$

1 Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

4.14.7.2 Media Local Bus (MLB) AC Electrical Characteristics

Table 31 and Table 32 provide the AC electrical characteristics for the Media Local Bus interface.

Table 31. MLB Timing for MLB Speed 256 Fs or 512 Fs

Spec	Parameter	Symbol	Min	Typ	Max	Unit	Comments
1	MLBCLK Operating Frequency[1]	f_{mck}	11.264 — — —	— 12.288 24.576 —	— — — 24.6272 25.600	MHz	256 Fs at 44.0 kHz 256 Fs at 48.0 kHz 512 Fs at 48.0 kHz 512 Fs at 48.1 kHz 512 Fs PLL unlocked
2	MLBCLK rise time	t_{mckr}	—	—	3	ns	V_{IL} to V_{IH}
3	MLBCLK fall time	t_{mckf}	—	—	3	ns	V_{IH} to V_{IL}
4	MLBCLK cycle time	t_{mckc}	—	81 40	—	ns	256 Fs 512 Fs
5	MLBCLK low time	t_{mckl}	31.5 30	37 35.5	—	ns	256 Fs 256 Fs PLL unlocked
			14.5 14	17 16.5	—	ns	512 Fs 512 Fs PLL unlocked
6	MLBCLK high time	t_{mckh}	31.5 30	38 36.5	—	ns	256xFs 256 Fs PLL unlocked
			14.5 14	17 16.5	—	ns	512 Fs 512 Fs PLL unlocked
7	MLBCLK pulse width variation[2]	t_{mpwv}	—	—	2	ns p-p	
8	MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	1	—	—	ns	
9	MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	0	—	—	ns	

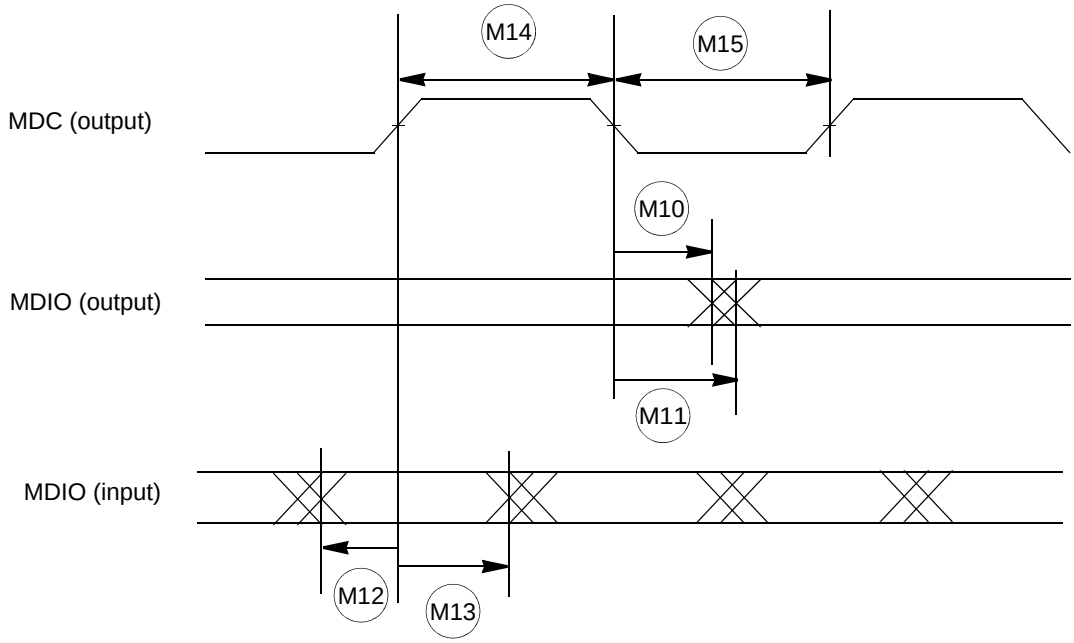

Figure 29. MII Serial Management Channel Timing Diagram

5 Package Characteristics

5.1 Package Mechanical Data

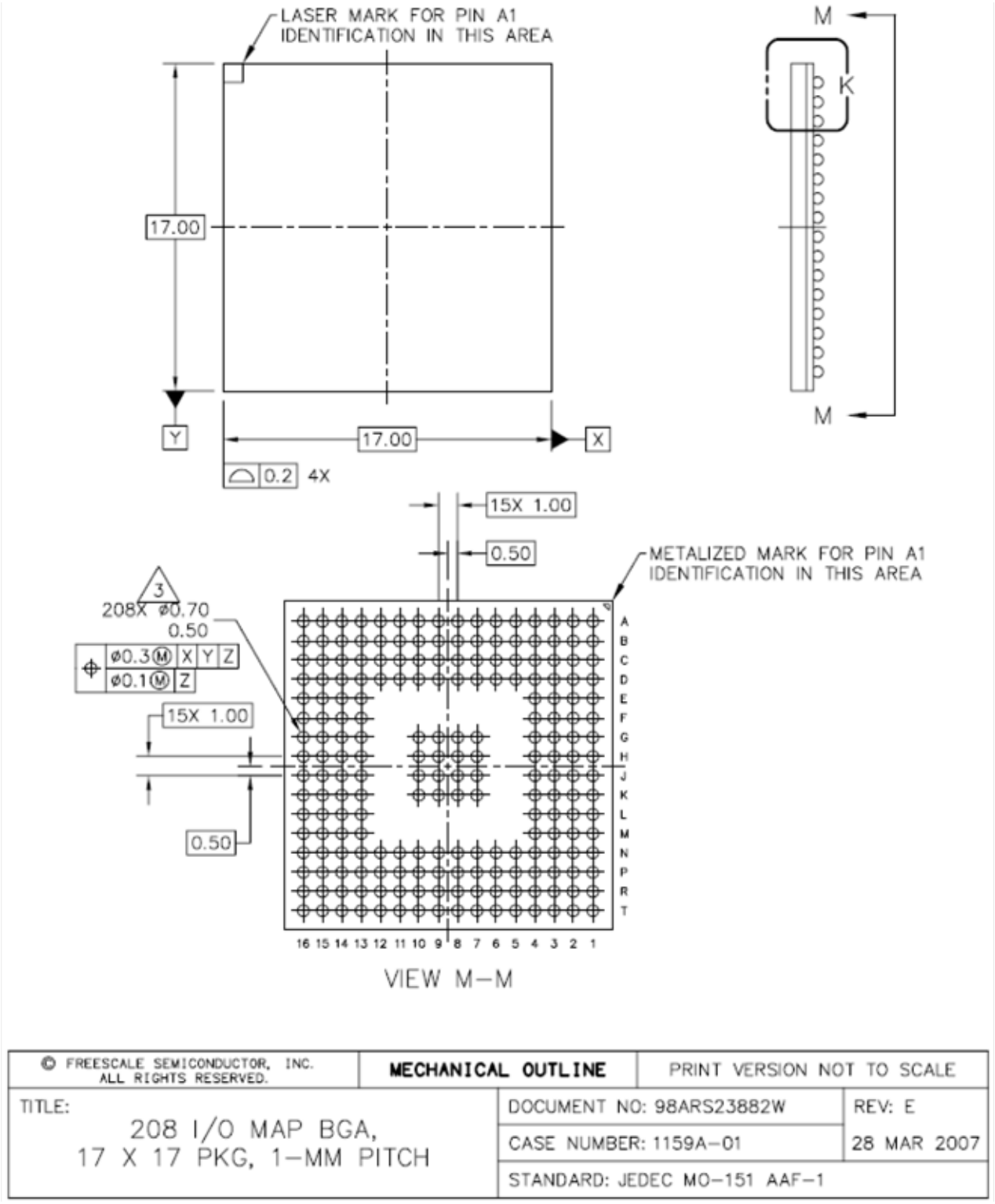

Figure 30. 208 MAPBGA Package Mechanical Drawing

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Document Number: MPC5668X
Rev. 6
2010, 2011