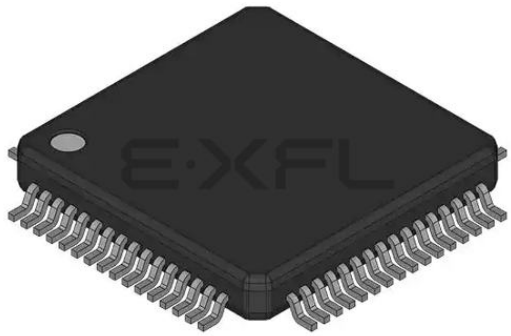

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	49
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12p64clh

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Chapter 3
Memory Map Control (S12PMMCV1)

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NOTE

Reserved register space shown in Table 1-2 is not allocated to any module. This register space is reserved for future use. Writing to these locations have no effect. Read access to these locations returns zero.

Figure 1-2 shows S12P CPU and BDM local address translation to the global memory map. It indicates also the location of the internal resources in the memory map. Table 1-3. shows the mapping of D-Flash and unpaged P-Flash memory. The whole 256K global memory space is visible through the P-Flash window located in the 64k local memory map located at 0x8000 - 0xBFFF using the PPAGE register.

Table 1-3. MC9S12P -Family mapping for D-Flash and unpaged P-Flash

	Local 64K memory map	Global 256K memory map
D-Flash	0x0400 - 0x13FF	0x0_4400 - 0x0_53FF
P-Flash	0x1400 - 0x27FF(1)	0x3_1400 -0x3_27FF(2)
	0x4000 - 0x7FFF	0x3_4000 - 0x3_7FFF
	0xC000 - 0xFFFF	0x3_C000 - 0x3_FFFF

1. 0x2FFF for MC9S12P64 because of 4K RAM size
2. 0x3_2FFF for MC9S12P64 because of 4K RAM size

Table 1-4. Derivatives

Feature	MC9S12P32	MC9S12P64	MC9S12P96	MC9S12P128
P-Flash size	32KB	64KB	96KB	128KB
PF_LOW PPAGES	0x3_8000 0x0E - 0x0F	0x3_0000 0x0C - 0x0F	0x2_8000 0x0A - 0x0F	0x2_0000 0x08 - 0x0F
RAMSIZE	2KB	4KB	6KB	
RAM_LOW	0x0_3800	0x0_3000	0x0_2800	

Table 1-8. Pin-Out Summary[1]

Package Pin			Function			Power Supply	Internal Pull Resistor		Description
QFP 80	LQFP 64	QFN 48	Pin	2nd Func.	3rd Func.		CTRL	Reset State	
1	1	1	PP3	KWP3	PWM3	VDDX	PERP/PPSP	Disabled	Port P I/O, interrupt, PWM channel
2	2	2	PP2	KWP2	PWM2	VDDX	PERP/PPSP	Disabled	Port P I/O, interrupt, PWM channel
3	3	3	PP1	KWP1	PWM1	VDDX	PERP/PPSP	Disabled	Port P I/O, interrupt, PWM channel
4	4	-	PP0	KWP0	PWM0	VDDX	PERP/PPSP	Disabled	Port P I/O, interrupt, PWM/ channel
5	5	4	PT0	IOC0	PWM0	VDDX	PERT/PPST	Disabled	Port T I/O, TIM channel
6	6	5	PT1	IOC1	—	VDDX	PERT/PPST	Disabled	Port T I/O, TIM channel
7	7	6	PT2	IOC2	—	VDDX	PERT/PPST	Disabled	Port T I/O, TIM channel
8	8	7	PT3	IOC3	—	VDDX	PERT/PPST	Disabled	Port T I/O, TIM channel
9	9	-	PJ0	KWJ0	—	VDDX	PERJ/PPSJ	Up	Port J I/O, interrupt
10	10	-	PJ1	KWJ1	—	VDDX	PERJ/PPSJ	Up	Port J I/O, interrupt
11	11	8	PT4	IOC4	PWM4	VDDX	PERT/PPST	Disabled	Port T I/O, PWM/TIM channel
12	12	9	PT5	IOC5	PWM5 or API_EXTCLK	VDDX	PERT/PPST	Disabled	Port T I/O, PWM/TIM channel, API output
13	13	10	PT6	IOC6		VDDX	PERT/PPST	Disabled	Port T I/O, channel of TIM
14	14	11	PT7	IOC7		VDDX	PERT/PPST	Disabled	Port T I/O, channel of TIM
15	15	12	BKGD	MODC	—	VDDX	Always on	Up	Background debug

Table 2-2. Block Memory Map (continued)

Port	Offset or Address	Register	Access	Reset Value	Section/Page
S	0x0248	PTS—Port S Data Register	R/W	0x00	2.3.24/2-77
	0x0249	PTIS—Port S Input Register	R	[4]	2.3.25/2-77
	0x024A	DDRS—Port S Data Direction Register	R/W	0x00	2.3.26/2-78
	0x024B	RDRS—Port S Reduced Drive Register	R/W	0x00	2.3.27/2-79
	0x024C	PERS—Port S Pull Device Enable Register	R/W	0xFF	2.3.28/2-79
	0x024D	PTPS—Port S Polarity Select Register	R/W	0x00	2.3.29/2-80
	0x024E	WOMS—Port S Wired-Or Mode Register	R/W	0x00	2.3.30/2-80
	0x024F	PIM Reserved	R	0x00	2.3.39/2-86
M	0x0250	PTM—Port M Data Register	R/W	0x00	2.3.32/2-81
	0x0251	PTIM—Port M Input Register	R	[4]	2.3.33/2-82
	0x0252	DDRM—Port M Data Direction Register	R/W	0x00	2.3.34/2-83
	0x0253	RDRM—Port M Reduced Drive Register	R/W	0x00	2.3.35/2-84
	0x0254	PERM—Port M Pull Device Enable Register	R/W	0x00	2.3.36/2-85
	0x0255	PPSM—Port M Polarity Select Register	R/W	0x00	2.3.37/2-85
	0x0256	WOMM—Port M Wired-Or Mode Register	R/W	0x00	2.3.38/2-86
	0x0257	PIM Reserved	R	0x00	2.3.39/2-86
P	0x0258	PTP—Port P Data Register	R/W	0x00	2.3.40/2-87
	0x0259	PTIP—Port P Input Register	R	[4]	2.3.41/2-88
	0x025A	DDRP—Port P Data Direction Register	R/W	0x00	2.3.42/2-88
	0x025B	RDRP—Port P Reduced Drive Register	R/W	0x00	2.3.43/2-89
	0x025C	PERP—Port P Pull Device Enable Register	R/W	0x00	2.3.44/2-90
	0x025D	PTPP—Port P Polarity Select Register	R/W	0x00	2.3.45/2-90
	0x025E	PIEP—Port P Interrupt Enable Register	R/W	0x00	2.3.46/2-91
	0x025F	PIFP—Port P Interrupt Flag Register	R/W	0x00	2.3.47/2-91
	0x0260 : 0x0267	PIM Reserved	R	0x00	2.3.48/2-92

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0020–0x023F Non-PIM Address Range	R	Non-PIM Address Range							
	W								
0x0240 PTT	R	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
	W								
0x0241 PTIT	R	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
	W								
0x0242 DDRT	R	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
	W								
0x0243 RDRT	R	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
	W								
0x0244 PERT	R	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
	W								
0x0245 PPST	R	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
	W								
0x0246 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0247 PTTRR	R	0	0	PTTRR5	PTTRR4	0	0	0	PTTRR0
	W								
0x0248 PTS	R	0	0	0	0	PTS3	PTS2	PTS1	PTS0
	W								
0x0249 PTIS	R	0	0	0	0	PTIS3	PTIS2	PTIS1	PTIS0
	W								
0x024A DDRS	R	0	0	0	0	DDRS3	DDRS2	DDRS1	DDRS0
	W								
0x024B RDRS	R	0	0	0	0	RDRS3	RDRS2	RDRS1	RDRS0
	W								
0x024C PERS	R	0	0	0	0	PERS3	PERS2	PERS1	PERS0
	W								
0x024D PPSS	R	0	0	0	0	PPSS3	PPSS2	PPSS1	PPSS0
	W								

= Unimplemented or Reserved

2.3.21 Port T Polarity Select Register (PPST)

Address 0x0245 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
Reset	0	0	0	0	0	0	0	0

Figure 2-19. Port T Polarity Select Register (PPST)

1. Read: Anytime
   Write: Anytime

Table 2-19. PPST Register Field Descriptions

Field	Description
7-0 PPST	**Port T pull device select**—Configure pull device polarity on input pin This bit selects a pull-up or a pull-down device if enabled on the associated port input pin. 1 A pull-down device is selected 0 A pull-up device is selected

2.3.22 PIM Reserved Register

Address 0x0246 Access: User read(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-20. PIM Reserved Register

1. Read: Always reads 0x00
   Write: Unimplemented

2.3.58 Port AD Data Register (PT1AD)

Address 0x0271 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PT1AD7	PT1AD6	PT1AD5	PT1AD4	PT1AD3	PT1AD2	PT1AD1	PT1AD0
Altern. Function	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
Reset	0	0	0	0	0	0	0	0

Figure 2-56. Port AD Data Register (PT1AD)

1. Read: Anytime. The data source is depending on the data direction value.
   Write: Anytime

Table 2-52. PT1AD Register Field Descriptions

Field	Description
7-0 PT1AD	**Port AD general purpose input/output data**—Data Register, ATD AN analog input When not used with the alternative function, the associated pin can be used as general purpose I/O. In general purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the buffered pin input state is read.

2.3.59 Port AD Data Direction Register (DDR0AD)

Address 0x0272 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	DDR0AD1	DDR0AD0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-57. Port AD Data Direction Register (DDR0AD)

1. Read: Anytime
   Write: Anytime

Table 2-53. DDR0AD Register Field Descriptions

Field	Description
1-0 DDR0AD	**Port AD data direction**— This bit determines whether the associated pin is an input or output. To use the digital input function the ATD Digital Input Enable Register (ATDDIEN) has to be set to logic level “1”. 1 Associated pin is configured as output 0 Associated pin is configured as input

3.1.2 Overview

The S12PMMC connects the CPU12's and the S12SBDM's bus interfaces to the MCU's on-chip ressources (memories and peripherals). It arbitrates the bus accesses and detemines all of the MCU's memory maps. Furthermore, the S12PMMC is responsible for constraining memory accesses on secured devices and for selecting the MCU's functional mode.

3.1.3 Features

The main features of this block are:

- Paging capability to support a global 256 KByte memory address space
- Bus arbitration between the masters CPU12, S12SBDM to different resources.
- MCU operation mode control
- MCU security control
- Separate memory map schemes for each master CPU12, S12SBDM
- Generation of system reset when CPU12 accesses an unimplemented address (i.e., an address which does not belong to any of the on-chip modules) in single-chip modes

3.1.4 Modes of Operation

The S12PMMC selects the MCU's functional mode. It also determines the devices behavior in secured and unsecured state.

3.1.4.1 Functional Modes

Two funtional modes are implementes on devices of the S12I product family:

- Normal Single Chip (NS)
  The mode used for running applications.
- Special Single Chip Mode (SS)
  A debug mode which causes the device to enter BDM Active Mode after each reset. Peripherals may also provide special debug features in this mode.

3.1.4.2 Security

S12I devives can be secured to prohibit external access to the on-chip P-Flash. The S12PMMC module determines the access permissions to the on-chip memories in secured and unsecured state.

3.1.5 Block Diagram

Figure 3-1 shows a block diagram of the S12PMMC.

Chapter 4
Interrupt Module (S12SINTV1)

Version Number	Revision Date	Effective Date	Author	Description of Changes
01.02	13 Sep 2007			updates for S12P family devices: - re-added XIRQ and IRQ references since this functionality is used on devices without D2D - added low voltage reset as possible source to the pin reset vector
01.03	21 Nov 2007			added clarification of “Wake-up from STOP or WAIT by XIRQ with X bit set” feature
01.04	20 May 2009			added footnote about availability of “Wake-up from STOP or WAIT by XIRQ with X bit set” feature

4.1 Introduction

The INT module decodes the priority of all system exception requests and provides the applicable vector for processing the exception to the CPU. The INT module supports:

- I bit and X bit maskable interrupt requests
- A non-maskable unimplemented op-code trap
- A non-maskable software interrupt (SWI) or background debug mode request
- Three system reset vector requests
- A spurious interrupt vector

Each of the I bit maskable interrupt requests is assigned to a fixed priority level.

4.1.1 Glossary

Table 4-2 contains terms and abbreviations used in the document.

Table 4-2. Terminology

Term	Meaning
CCR	Condition Code Register (in the CPU)
ISR	Interrupt Service Routine
MCU	Micro-Controller Unit

4.1.2 Features

- Interrupt vector base register (IVBR)
- One spurious interrupt vector (at address vector base[1] + 0x0080).

6.3.2.7.2 Debug State Control Register 2 (DBGSCR2)

Address: 0x0027

	7	6	5	4	3	2	1	0
R	0	0	0	0	SC3	SC2	SC1	SC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-10. Debug State Control Register 2 (DBGSCR2)

Read: If COMRV[1:0] = 01

Write: If COMRV[1:0] = 01 and DBG is not armed.

This register is visible at 0x0027 only with COMRV[1:0] = 01. The state control register 2 selects the targeted next state whilst in State2. The matches refer to the match channels of the comparator match control logic as depicted in Figure 6-1 and described in 6.3.2.8.1. Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 6-17. DBGSCR2 Field Descriptions

Field	Description
3–0 SC[3:0]	These bits select the targeted next state whilst in State2, based upon the match event.

Table 6-18. State2 —Sequencer Next State Selection

SC[3:0]	Description (Unspecified matches have no effect)
0000	Match0 to State1..... Match2 to State3.
0001	Match1 to State3
0010	Match2 to State3
0011	Match1 to State3..... Match0 Final State
0100	Match1 to State1..... Match2 to State3.
0101	Match2 to Final State
0110	Match2 to State1..... Match0 to Final State
0111	Either Match0 or Match1 to Final State
1000	Reserved
1001	Reserved
1010	Reserved
1011	Reserved
1100	Either Match0 or Match1 to Final State.....Match2 to State3
1101	Reserved
1110	Reserved
1111	Either Match0 or Match1 to Final State.....Match2 to State1

The priorities described in Table 6-36 dictate that in the case of simultaneous matches, a match leading to final state has priority followed by the match on the lower channel number (0,1,2)

6.4.2.1.4 Comparator A Data Bus Comparison NDB Dependency

Comparator A features an NDB control bit, which allows data bus comparators to be configured to either trigger on equivalence or trigger on difference. This allows monitoring of a difference in the contents of an address location from an expected value.

When matching on an equivalence (NDB=0), each individual data bus bit position can be masked out by clearing the corresponding mask bit (DBGADHM/DBGADLM) so that it is ignored in the comparison. A match occurs when all data bus bits with corresponding mask bits set are equivalent. If all mask register bits are clear, then a match is based on the address bus only, the data bus is ignored.

When matching on a difference, mask bits can be cleared to ignore bit positions. A match occurs when any data bus bit with corresponding mask bit set is different. Clearing all mask bits, causes all bits to be ignored and prevents a match because no difference can be detected. In this case address bus equivalence does not cause a match.

Table 6-35. NDB and MASK bit dependency

NDB	DBGADHM[n] / DBGADLM[n]	Comment
0	0	Do not compare data bus bit.
0	1	Compare data bus bit. Match on equivalence.
1	0	Do not compare data bus bit.
1	1	Compare data bus bit. Match on difference.

6.4.2.2 Range Comparisons

Using the AB comparator pair for a range comparison, the data bus can also be used for qualification by using the comparator A data registers. Furthermore the DBGACTL RW and RWE bits can be used to qualify the range comparison on either a read or a write access. The corresponding DBGBCTL bits are ignored. The SZE and SZ control bits are ignored in range mode. The comparator A TAG bit is used to tag range comparisons. The comparator B TAG bit is ignored in range modes. In order for a range comparison using comparators A and B, both COMPEA and COMPEB must be set; to disable range comparisons both must be cleared. The comparator A BRK bit is used to for the AB range, the comparator B BRK bit is ignored in range mode.

When configured for range comparisons and tagging, the ranges are accurate only to word boundaries.

6.4.2.2.1 Inside Range (CompA_Addr ≤ address ≤ CompB_Addr)

In the Inside Range comparator mode, comparator pair A and B can be configured for range comparisons. This configuration depends upon the control register (DBGC2). The match condition requires that a valid match for both comparators happens on the same bus cycle. A match condition on only one comparator is not valid. An aligned word access which straddles the range boundary is valid only if the aligned address is inside the range.

Table 7-5. CPMUCLKS Descriptions (continued)

Field	Description
3 PRE	**RTI Enable During Pseudo Stop Bit** — PRE enables the RTI during Pseudo Stop Mode. 0 RTI stops running during Pseudo Stop Mode. 1 RTI continues running during Pseudo Stop Mode if RTIOSCSEL=1. **Note:** If PRE=0 or RTIOSCSEL=0 then the RTI will go static while Stop Mode is active. The RTI counter will not be reset.
2 PCE	**COP Enable During Pseudo Stop Bit** — PCE enables the COP during Pseudo Stop Mode. 0 COP stops running during Pseudo Stop Mode 1 COP continues running during Pseudo Stop Mode if COPOSCSEL=1 **Note:** If PCE=0 or COPOSCSEL=0 then the COP will go static while Stop Mode is active. The COP counter will not be reset.
1 RTIOSCSEL	**RTI Clock Select**— RTIOSCSEL selects the clock source to the RTI. Either IRCCLK or OSCCLK. Changing the RTIOSCSEL bit re-starts the RTI time-out period. RTIOSCSEL can only be set to 1, if UPOSC=1. UPOSC= 0 clears the RTIOSCSEL bit. 0 RTI clock source is IRCCLK. 1 RTI clock source is OSCCLK.
0 COPOSCSEL	**COP Clock Select**— COPOSCSEL selects the clock source to the COP. Either IRCCLK or OSCCLK. Changing the COPOSCSEL bit re-starts the COP time-out period. COPOSCSEL can only be set to 1, if UPOSC=1. UPOSC= 0 clears the COPOSCSEL bit. 0 COP clock source is IRCCLK. 1 COP clock source is OSCCLK

Figure 8-24. Receive/Transmit Message Buffer — Extended Identifier Mapping (continued)

Register Name		Bit 7	6	5	4	3	2	1	Bit0
0x00X4 DSR0	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X5 DSR1	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X6 DSR2	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X7 DSR3	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X8 DSR4	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X9 DSR5	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XA DSR6	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XB DSR7	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XC DLR	R					DLC3	DLC2	DLC1	DLC0
	W								

= Unused, always read 'x'

Read:

- For transmit buffers, anytime when TXEx flag is set (see Section 8.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 8.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").
- For receive buffers, only when RXF flag is set (see Section 8.3.2.5, "MSCAN Receiver Flag Register (CANRFLG)").

Write:

Table 9-2. Multi-Channel Wrap Around Coding

WRAP3	WRAP2	WRAP1	WRAP0	Multiple Channel Conversions (MULT = 1) Wraparound to AN0 after Converting
0	1	1	0	AN6
0	1	1	1	AN7
1	0	0	0	AN8
1	0	0	1	AN9
1	0	1	0	AN9
1	0	1	1	AN9
1	1	0	0	AN9
1	1	0	1	AN9
1	1	1	0	AN9
1	1	1	1	AN9

1. If only AN0 should be converted use MULT=0.

9.3.2.2 ATD Control Register 1 (ATDCTL1)

Writes to this register will abort current conversion sequence.

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R W	ETRIGSEL	SRES1	SRES0	SMP_DIS	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
Reset	0	0	1	0	1	1	1	1

Figure 9-4. ATD Control Register 1 (ATDCTL1)

Read: Anytime

Write: Anytime

Table 9-3. ATDCTL1 Field Descriptions

Field	Description
7 ETRIGSEL	**External Trigger Source Select** — This bit selects the external trigger source to be either one of the AD channels or one of the ETRIG3-0 inputs. See device specification for availability and connectivity of ETRIG3-0 inputs. If a particular ETRIG3-0 input option is not available, writing a 1 to ETRISEL only sets the bit but has not effect, this means that one of the AD channels (selected by ETRIGCH3-0) is configured as the source for external trigger. The coding is summarized in Table 9-5.
6–5 SRES[1:0]	**A/D Resolution Select** — These bits select the resolution of A/D conversion results. See Table 9-4 for coding.

Module Base + 0x0004

	7	6	5	4	3	2	1	0
R	0	0	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-7. PWM Center Align Enable Register (PWMCAE)

Read: anytime

Write: anytime

NOTE

Write these bits only when the corresponding channel is disabled.

Table 10-8. PWMCAE Field Descriptions

Field	Description
5 CAE5	**Center Aligned Output Mode on Channel 5** 0 Channel 5 operates in left aligned output mode. 1 Channel 5 operates in center aligned output mode.
4 CAE4	**Center Aligned Output Mode on Channel 4** 0 Channel 4 operates in left aligned output mode. 1 Channel 4 operates in center aligned output mode.
3 CAE3	**Center Aligned Output Mode on Channel 3** 1 Channel 3 operates in left aligned output mode. 1 Channel 3 operates in center aligned output mode.
2 CAE2	**Center Aligned Output Mode on Channel 2** 0 Channel 2 operates in left aligned output mode. 1 Channel 2 operates in center aligned output mode.
1 CAE1	**Center Aligned Output Mode on Channel 1** 0 Channel 1 operates in left aligned output mode. 1 Channel 1 operates in center aligned output mode.
0 CAE0	**Center Aligned Output Mode on Channel 0** 0 Channel 0 operates in left aligned output mode. 1 Channel 0 operates in center aligned output mode.

10.3.2.6 PWM Control Register (PWMCTL)

The PWMCTL register provides for various control of the PWM module.

NOTE

In single-wire operation data from the TXD pin is inverted if RXPOL is set.

11.4.8 Loop Operation

In loop operation the transmitter output goes to the receiver input. The RXD pin is disconnected from the SCI.

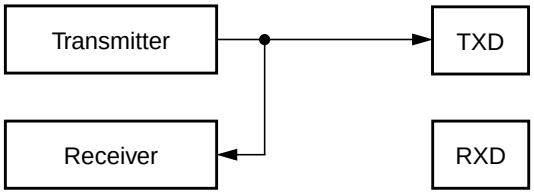

Figure 11-31. Loop Operation (LOOPS = 1, RSRC = 0)

Enable loop operation by setting the LOOPS bit and clearing the RSRC bit in SCI control register 1 (SCICR1). Setting the LOOPS bit disables the path from the RXD pin to the receiver. Clearing the RSRC bit connects the transmitter output to the receiver input. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).

NOTE

In loop operation data from the transmitter is not recognized by the receiver if RXPOL and TXPOL are not the same.

11.5 Initialization/Application Information

11.5.1 Reset Initialization

See Section 11.3.2, “Register Descriptions”.

11.5.2 Modes of Operation

11.5.2.1 Run Mode

Normal mode of operation.

To initialize a SCI transmission, see Section 11.4.5.2, “Character Transmission”.

11.5.2.2 Wait Mode

SCI operation in wait mode depends on the state of the SCISWAI bit in the SCI control register 1 (SCICR1).

- If SCISWAI is clear, the SCI operates normally when the CPU is in wait mode.
- If SCISWAI is set, SCI clock generation ceases and the SCI module enters a power-conservation state when the CPU is in wait mode. Setting SCISWAI does not affect the state of the receiver enable bit, RE, or the transmitter enable bit, TE.

13.3.2 Register Descriptions

The Flash module contains a set of 20 control and status registers located between Flash module base + 0x0000 and 0x0013. A summary of the Flash module registers is given in Figure 13-4 with detailed descriptions in the following subsections.

CAUTION

Writes to any Flash register must be avoided while a Flash command is active (CCIF=0) to prevent corruption of Flash register contents and adversely affect Memory Controller behavior.

Address & Name		7	6	5	4	3	2	1	0
0x0000 FCLKDIV	R	FDIVLD	FDIVLCK	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
	W								
0x0001 FSEC	R	KEYEN1	KEYEN0	RNV5	RNV4	RNV3	RNV2	SEC1	SEC0
	W								
0x0002 FCCOBIX	R	0	0	0	0	0	CCOBIX2	CCOBIX1	CCOBIX0
	W								
0x0003 FRSV0	R	0	0	0	0	0	0	0	0
	W								
0x0004 FCNFG	R	CCIE	0	0	IGNSF	0	0	FDFD	FSFD
	W								
0x0005 FERCNFG	R	0	0	0	0	0	0	DFDIE	SFDIE
	W								
0x0006 FSTAT	R	CCIF	0	ACCERR	FPVIOL	MGBUSY	RSVD	MGSTAT1	MGSTAT0
	W								
0x0007 FERSTAT	R	0	0	0	0	0	0	DFDIF	SFDIF
	W								
0x0008 FPROT	R	FPOPEN	RNV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
	W								
0x0009 DFPROT	R	DPOPEN	0	0	0	DPS3	DPS2	DPS1	DPS0
	W								

Figure 13-4. FTMRC128K1 Register Summary

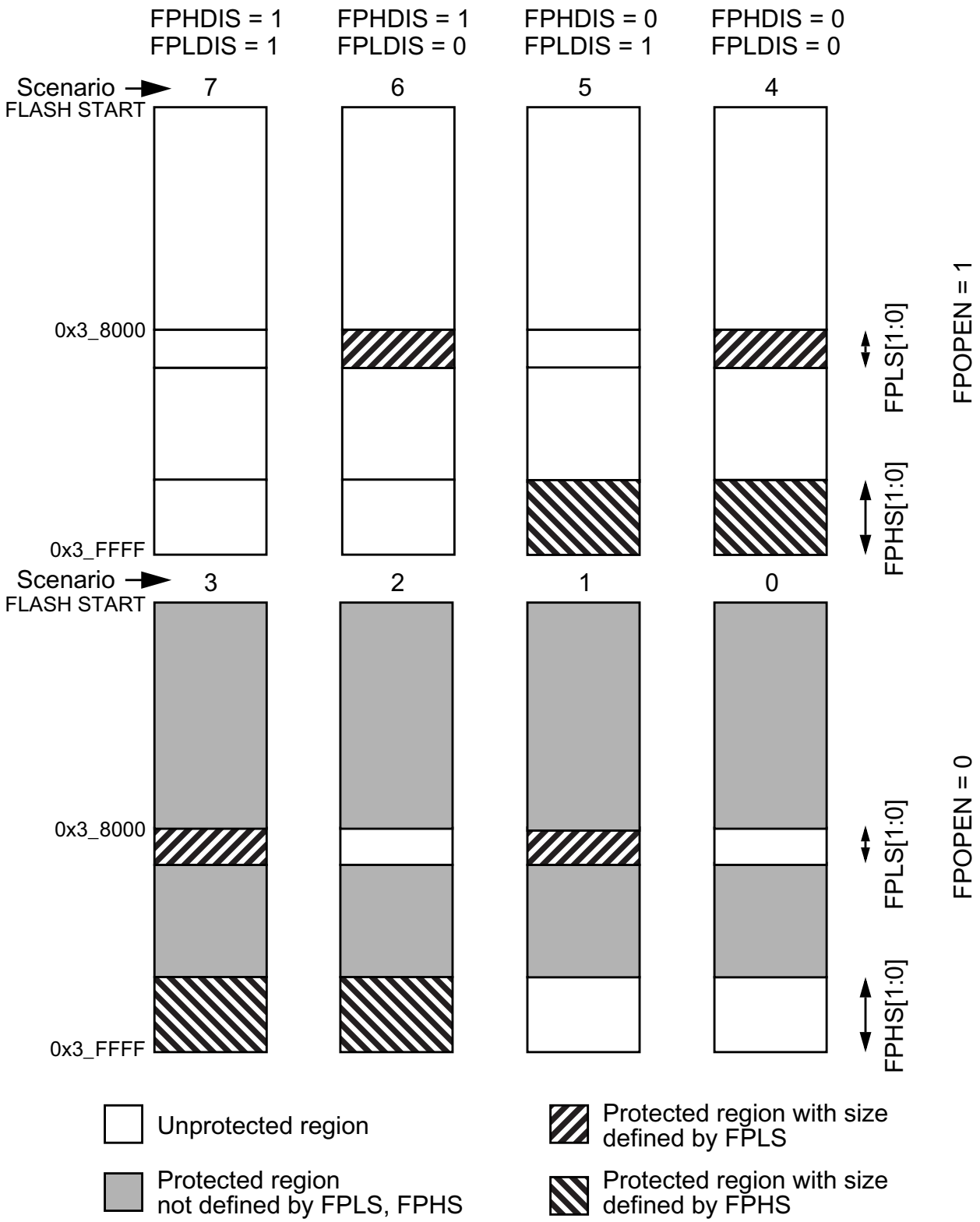

Figure 13-14. P-Flash Protection Scenarios

Table A-1. Absolute Maximum Ratings[1]

Num	Rating	Symbol	Min	Max	Unit
1	I/O, regulator and analog supply voltage	V_{DD35}	–0.3	6.0	V
2	Voltage difference V_{DDX} to V_{DDA}	Δ_{VDDX}	–6.0	0.3	V
3	Voltage difference V_{SSX} to V_{SSA}	Δ_{VSSX}	–0.3	0.3	V
4	Digital I/O input voltage	V_{IN}	–0.3	6.0	V
5	Analog reference	V_{RH}, V_{RL}	–0.3	6.0	V
6	EXTAL, XTAL	V_{ILV}	–0.3	2.16	V
7	Instantaneous maximum current Single pin limit for all digital I/O pins[2]	I_D	–25	+25	mA
8	Instantaneous maximum current Single pin limit for EXTAL, XTAL	I_{DL}	–25	+25	mA
9	Storage temperature range	T_{stg}	–65	155	°C

1. Beyond absolute maximum ratings device might be damaged.
2. All digital I/O pins are internally clamped to V_{SSX} and V_{DDX}, or V_{SSA} and V_{DDA}.

A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 stress test qualification for automotive grade integrated circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.1.10.1 Measurement Conditions

Run current is measured on VDDR pin. It does not include the current to drive external loads. Unless otherwise noted the currents are measured in special single chip mode and the CPU code is executed from RAM. For Run and Wait current measurements PLL is on and the reference clock is the IRC1M trimmed to 1MHz. The bus frequency is 32MHz and the CPU frequency is 64MHz. Table A-8., Table A-9. and Table A-10. show the configuration of the CPMU module and the peripherals for Run, Wait and Stop current measurement.

Table A-8. CPMU Configuration for Pseudo Stop Current Measurement

CPMU REGISTER	Bit settings/Conditions
CPMUCLKS	PLLSEL=0, PSTP=1, PRE=PCE=RTIOSCSEL=COPOSCSEL=1
CPMUOSC	OSCE=1, External Square wave on EXTAL f_{EXTAL}=16MHz, V_{IH}= 1.8V, V_{IL}=0V
CPMURTI	RTDEC=0, RTR[6:4]=111, RTR[3:0]=1111;
CPMUCOP	WCOP=1, CR[2:0]=111

Table A-9. CPUM Configuration for Run/Wait and Full Stop Current Measurement

CPMU REGISTER	Bit settings/Conditions
CPMUSYNR	VCOFRQ[1:0]=01,SYNDIV[5:0] = 32
CPMUPOSTDIV	POSTDIV[4:0]=0,
CPMUCLKS	PLLSEL=1
CPMUOSC	OSCE=0, Reference clock for PLL is f_{ref}=f_{irc1m} trimmed to 1MHz
API settings for STOP current measurement	
CPMUAPICTL	APIEA=0, APIFE=1, APIE=0
CPMUAPITR	trimmed to 10Khz
CPMUAPIRH/RL	set to $FFFF