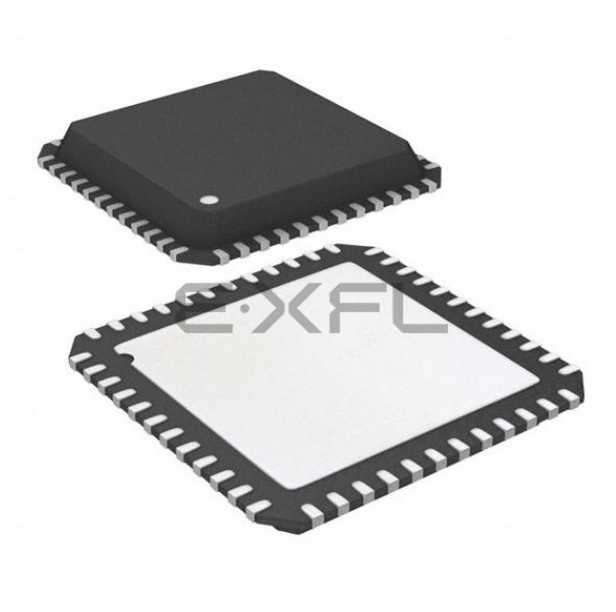

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TFQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
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Chapter 9
Analog-to-Digital Converter (ADC12B10C)

Chapter 10
Pulse-Width Modulator (PWM8B6CV1) Block Description

1.3.3 On-Chip SRAM

- Up to 6 Kbytes of general-purpose RAM

1.3.4 Main External Oscillator (XOSC)

- Loop control Pierce oscillator using a 4 MHz to 16 MHz crystal
  - Current gain control on amplitude output
  - Signal with low harmonic distortion
  - Low power
  - Good noise immunity
  - Eliminates need for external current limiting resistor
  - Transconductance sized for optimum start-up margin for typical crystals

1.3.5 Internal RC Oscillator (IRC)

- Trimmable internal reference clock.
  - Frequency: 1 MHz
  - Trimmed accuracy over –40˚C to +125˚C ambient temperature range: ±1.5%

1.3.6 Internal Phase-Locked Loop (IPLL)

- Phase-locked-loop clock frequency multiplier
  - No external components required
  - Reference divider and multiplier allow large variety of clock rates
  - Automatic bandwidth control mode for low-jitter operation
  - Automatic frequency lock detector
  - Configurable option to spread spectrum for reduced EMC radiation (frequency modulation)
  - Reference clock sources:
    - External 4–16 MHz resonator/crystal (XOSC)
    - Internal 1 MHz RC oscillator (IRC)

1.3.7 System Integrity Support

- Power-on reset (POR)
- System reset generation
- Illegal address detection with reset
- Low-voltage detection with interrupt or reset
- Real time interrupt (RTI)
- Computer operating properly (COP) watchdog
  - Configurable as window COP for enhanced failure detection

1.3.16 Debugger (DBG)

- Trace buffer with depth of 64 entries
- Three comparators (A, B and C)
  - Comparators A compares the full address bus and full 16-bit data bus
  - Exact address or address range comparisons
- Two types of comparator matches
  - Tagged This matches just before a specific instruction begins execution
  - Force This is valid on the first instruction boundary after a match occurs
- Four trace modes
- Four stage state sequencer

Table 1-8. Pin-Out Summary[1]

Package Pin			Function			Power Supply	Internal Pull Resistor		Description
QFP 80	LQFP 64	QFN 48	Pin	2nd Func.	3rd Func.		CTRL	Reset State	
35	29	22	XTAL	—	—	VDDPLL	NA	NA	Oscillator pin
36	30	23	PJ2	KWJ2	—	VDDX	PERJ/PPSJ	Up	Port J I/O, interrupt
37	-	-	PE3	—	—	VDDX	PUCR	Up	Port E I/O
38	-	-	PE2	—	—	VDDX	PUCR	Up	Port E I/O
39	31	24	PE1	$\overline{\text{IRQ}}$	—	VDDX	PUCR	Up	Port E Input, maskable interrupt
40	32	25	PE0	$\overline{\text{XIRQ}}$	—	VDDX	PUCR	Up	Port E Input, non-maskable interrupt
41	33	-	PA0	—	—	VDDX	PUCR	Disabled	Port A I/O
42	34	-	PA1	—	—	VDDX	PUCR	Disabled	Port A I/O
43	35	-	PA2	—	—	VDDX	PUCR	Disabled	Port A I/O
44	36	-	PA3	—	—	VDDX	PUCR	Disabled	Port A I/O
45	-	-	PA4	—	—	VDDX	PUCR	Disabled	Port A I/O
46	-	-	PA5	—	—	VDDX	PUCR	Disabled	Port A I/O
47	-	-	PA6	—	—	VDDX	PUCR	Disabled	Port A I/O
48	-	-	PA7	—	—	VDDX	PUCR	Disabled	Port A I/O
49	37	26	PAD08	AN08	—	VDDA	PER1AD	Disabled	Port AD I/O, analog input of ATD
50	38	27	PAD09	AN09	—	VDDA	PER1AD	Disabled	Port AD I/O, analog input of ATD
51	39	28	PAD00	AN00	—	VDDA	PER1AD	Disabled	Port AD I/O, analog input of ATD
52	40	29	PAD01	AN01	—	VDDA	PER1AD	Disabled	Port AD I/O, analog input of ATD

Address 0x001D Access: User read(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-11. PIM Reserved Register

1. Read: Always reads 0x00
   Write: Unimplemented

2.3.14 IRQ Control Register (IRQCR)

Address 0x001E Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	IRQE	IRQEN	0	0	0	0	0	0
W								
Reset	0	1	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-12. IRQ Control Register (IRQCR)

1. Read: See individual bit descriptions below.
   Write: See individual bit descriptions below.

Table 2-13. IRQCR Register Field Descriptions

Field	Description
7 IRQE	**IRQ select edge sensitive only**— Special mode: Read or write anytime. Normal mode: Read anytime, write once. 1 $\overline{\text{IRQ}}$ pin configured to respond only to falling edges. Falling edges on the $\overline{\text{IRQ}}$ pin will be detected anytime IRQE=1 and will be cleared only upon a reset or the servicing of the $\overline{\text{IRQ}}$ interrupt. 0 $\overline{\text{IRQ}}$ pin configured for low level recognition
6 IRQEN	**IRQ enable**— Read or write anytime. 1 $\overline{\text{IRQ}}$ pin is connected to interrupt logic 0 $\overline{\text{IRQ}}$ pin is disconnected from interrupt logic

2.3.15 PIM Reserved Register

This register is reserved for factory testing of the PIM module and is not available in normal operation. Writing to this register when in special modes can alter the pin functionality.

Table 3-6. DIRECT Field Descriptions

Field	Description
7–0 DP[15:8]	**Direct Page Index Bits 15–8** — These bits are used by the CPU when performing accesses using the direct addressing mode. These register bits form bits [15:8] of the local address (see Figure 3-6).

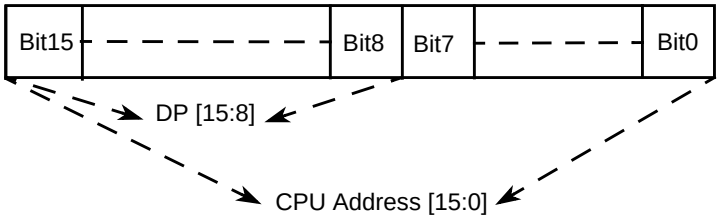


Figure 3-6. DIRECT Address Mapping

Example 3-1. This example demonstrates usage of the Direct Addressing Mode

```
MOVB      #$80,DIRECT       ;Set DIRECT register to 0x80. Write once only.
                            ;Global data accesses to the range 0xXX_80XX can be direct.
                            ;Logical data accesses to the range 0x80XX are direct.

LDY       <$00              ;Load the Y index register from 0x8000 (direct access).
                            ;< operator forces direct access on some assemblers but in
                            ;many cases assemblers are "direct page aware" and can
                            ;automatically select direct mode.
```

3.3.2.3 Program Page Index Register (PPAGE)

Address: 0x0030

	7	6	5	4	3	2	1	0
R	0	0	0	0	PIX3	PIX2	PIX1	PIX0
W								
Reset	0	0	0	0	1	1	1	0

Figure 3-7. Program Page Index Register (PPAGE)

Read: Anytime

Write: Anytime

These four index bits are used to map 16KB blocks into the Flash page window located in the local (CPU or BDM) memory map from address 0x8000 to address 0xBFFF (see Figure 3-8). This supports accessing up to 256 KB of Flash (in the Global map) within the 64KB Local map. The PPAGE index register is effectively used to construct paged Flash addresses in the Local map format. The CPU has special access to read and write this register directly during execution of CALL and RTC instructions.

clock please make sure that the communication rate is adapted accordingly and a communication time-out (BDM soft reset) has occurred.

5.3 Memory Map and Register Definition

5.3.1 Module Memory Map

Table 5-1 shows the BDM memory map when BDM is active.

Table 5-1. BDM Memory Map

Global Address	Module	Size (Bytes)
0x3_FF00–0x3_FF0B	BDM registers	12
0x3_FF0C–0x3_FF0E	BDM firmware ROM	3
0x3_FF0F	Family ID (part of BDM firmware ROM)	1
0x3_FF10–0x3_FFFF	BDM firmware ROM	240

5.3.2 Register Descriptions

A summary of the registers associated with the BDM is shown in Figure 5-2. Registers are accessed by host-driven communications to the BDM hardware using READ_BD and WRITE_BD commands.

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x3_FF00	Reserved	R	X	X	X	X	X	X	0	0
		W								
0x3_FF01	BDMSTS	R	ENBDM	BDMACT	0	SDV	TRACE	0	UNSEC	0
		W								
0x3_FF02	Reserved	R	X	X	X	X	X	X	X	X
		W								
0x3_FF03	Reserved	R	X	X	X	X	X	X	X	X
		W								
0x3_FF04	Reserved	R	X	X	X	X	X	X	X	X
		W								

= Unimplemented, Reserved

= Implemented (do not alter)

X = Indeterminate

0 = Always read zero

Figure 5-2. BDM Register Summary

Table 6-26. DBGXAM Field Descriptions

Field	Description
7–0 Bit[15:8]	**Comparator Address Mid Compare Bits** — The Comparator address mid compare bits control whether the selected comparator compares the address bus bits [15:8] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

6.3.2.8.4 Debug Comparator Address Low Register (DBGXAL)

Address: 0x002B

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 6-18. Debug Comparator Address Low Register (DBGXAL)

Read: Anytime. See Table 6-24 for visible register encoding.

Write: If DBG not armed. See Table 6-24 for visible register encoding.

Table 6-27. DBGXAL Field Descriptions

Field	Description
7–0 Bits[7:0]	**Comparator Address Low Compare Bits** — The Comparator address low compare bits control whether the selected comparator compares the address bus bits [7:0] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

6.3.2.8.5 Debug Comparator Data High Register (DBGADH)

Address: 0x002C

	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 6-19. Debug Comparator Data High Register (DBGADH)

Read: If COMRV[1:0] = 00

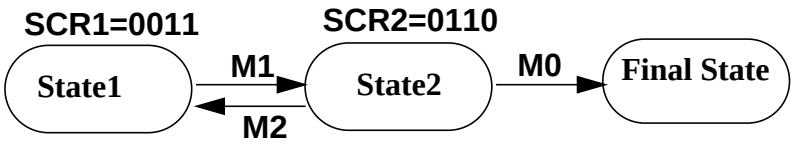
Write: If COMRV[1:0] = 00 and DBG not armed.

This however violates the S12SDBGV1 specification, which states that a match leading to final state always has priority in case of a simultaneous match, whilst priority is also given to the lowest channel number. For S12SDBG the corresponding CPU priority decoder is removed to support this, such that on simultaneous taghits, taghits pointing to final state have highest priority. If no taghit points to final state then the lowest channel number has priority. Thus with the above encoding from State3, the CPU and DBG would break on a simultaneous M0/M2.

6.5.6 Scenario 5

Trigger if following event A, event C precedes event B. i.e. the expected execution flow is A->B->C.

Figure 6-34. Scenario 5

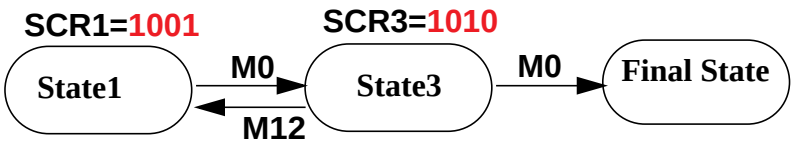


Scenario 5 is possible with the S12SDBGV1 SCR encoding

6.5.7 Scenario 6

Trigger if event A occurs twice in succession before any of 2 other events (BC) occurs. This scenario is not possible using the S12SDBGV1 SCR encoding. S12SDBGV2 includes additions shown in red. The change in SCR1 encoding also has the advantage that a State1->State3 transition using M0 is now possible. This is advantageous because range and data bus comparisons use channel0 only.

Figure 6-35. Scenario 6



6.5.8 Scenario 7

Trigger when a series of 3 events is executed out of order. Specifying the event order as M1,M2,M0 to run in loops (120120120). Any deviation from that order should trigger. This scenario is not possible using the

Figure 8-24. Receive/Transmit Message Buffer — Extended Identifier Mapping (continued)

Register Name		Bit 7	6	5	4	3	2	1	Bit0
0x00X4 DSR0	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X5 DSR1	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X6 DSR2	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X7 DSR3	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X8 DSR4	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X9 DSR5	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XA DSR6	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XB DSR7	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XC DLR	R					DLC3	DLC2	DLC1	DLC0
	W								

= Unused, always read 'x'

Read:

- For transmit buffers, anytime when TXEx flag is set (see Section 8.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 8.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").
- For receive buffers, only when RXF flag is set (see Section 8.3.2.5, "MSCAN Receiver Flag Register (CANRFLG)").

Write:

- Any CAN node is able to send out a stream of scheduled messages without releasing the CAN bus between the two messages. Such nodes arbitrate for the CAN bus immediately after sending the previous message and only release the CAN bus in case of lost arbitration.
- The internal message queue within any CAN node is organized such that the highest priority message is sent out first, if more than one message is ready to be sent.

The behavior described in the bullets above cannot be achieved with a single transmit buffer. That buffer must be reloaded immediately after the previous message is sent. This loading process lasts a finite amount of time and must be completed within the inter-frame sequence (IFS) to be able to send an uninterrupted stream of messages. Even if this is feasible for limited CAN bus speeds, it requires that the CPU reacts with short latencies to the transmit interrupt.

A double buffer scheme de-couples the reloading of the transmit buffer from the actual message sending and, therefore, reduces the reactiveness requirements of the CPU. Problems can arise if the sending of a message is finished while the CPU re-loads the second buffer. No buffer would then be ready for transmission, and the CAN bus would be released.

At least three transmit buffers are required to meet the first of the above requirements under all circumstances. The MSCAN has three transmit buffers.

The second requirement calls for some sort of internal prioritization which the MSCAN implements with the "local priority" concept described in Section 8.4.2.2, "Transmit Structures."

8.4.2.2 Transmit Structures

The MSCAN triple transmit buffer scheme optimizes real-time performance by allowing multiple messages to be set up in advance. The three buffers are arranged as shown in Figure 8-39.

All three buffers have a 13-byte data structure similar to the outline of the receive buffers (see Section 8.3.3, "Programmer's Model of Message Storage"). An additional Transmit Buffer Priority Register (TBPR) contains an 8-bit local priority field (PRIO) (see Section 8.3.3.4, "Transmit Buffer Priority Register (TBPR)"). The remaining two bytes are used for time stamping of a message, if required (see Section 8.3.3.5, "Time Stamp Register (TSRH–TSRL)").

To transmit a message, the CPU must identify an available transmit buffer, which is indicated by a set transmitter buffer empty (TXEx) flag (see Section 8.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)"). If a transmit buffer is available, the CPU must set a pointer to this buffer by writing to the CANTBSEL register (see Section 8.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)"). This makes the respective buffer accessible within the CANTXFG address space (see Section 8.3.3, "Programmer's Model of Message Storage"). The algorithmic feature associated with the CANTBSEL register simplifies the transmit buffer selection. In addition, this scheme makes the handler software simpler because only one address area is applicable for the transmit process, and the required address space is minimized.

The CPU then stores the identifier, the control bits, and the data content into one of the transmit buffers. Finally, the buffer is flagged as ready for transmission by clearing the associated TXE flag.

9.3.2.3 ATD Control Register 2 (ATDCTL2)

Writes to this register will abort current conversion sequence.

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	0	AFFC	ICLKSTP	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ACMPIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-5. ATD Control Register 2 (ATDCTL2)

Read: Anytime

Write: Anytime

Table 9-6. ATDCTL2 Field Descriptions

Field	Description
6 AFFC	**ATD Fast Flag Clear All** 0 ATD flag clearing done by write 1 to respective CCF[*n*] flag. 1 Changes all ATD conversion complete flags to a fast clear sequence. For compare disabled (CMPE[*n*]=0) a read access to the result register will cause the associated CCF[*n*] flag to clear automatically. For compare enabled (CMPE[*n*]=1) a write access to the result register will cause the associated CCF[*n*] flag to clear automatically.
5 ICLKSTP	**Internal Clock in Stop Mode Bit** — This bit enables A/D conversions in stop mode. When going into stop mode and ICLKSTP=1 the ATD conversion clock is automatically switched to the internally generated clock ICLK. Current conversion sequence will seamless continue. Conversion speed will change from prescaled bus frequency to the ICLK frequency (see ATD Electrical Characteristics in device description). The prescaler bits PRS4-0 in ATDCTL4 have no effect on the ICLK frequency. For conversions during stop mode the automatic compare interrupt or the sequence complete interrupt can be used to inform software handler about changing A/D values. External trigger will not work while converting in stop mode. For conversions during transition from Run to Stop Mode or vice versa the result is not written to the results register, no CCF flag is set and no compare is done. When converting in Stop Mode (ICLKSTP=1) an ATD Stop Recovery time $t_{ATDSTPRCV}$ is required to switch back to bus clock based ATDCLK when leaving Stop Mode. Do not access ATD registers during this time. 0 If A/D conversion sequence is ongoing when going into stop mode, the actual conversion sequence will be aborted and automatically restarted when exiting stop mode. 1 A/D continues to convert in stop mode using internally generated clock (ICLK)
4 ETRIGLE	**External Trigger Level/Edge Control** — This bit controls the sensitivity of the external trigger signal. See Table 9-7 for details.
3 ETRIGP	**External Trigger Polarity** — This bit controls the polarity of the external trigger signal. See Table 9-7 for details.
2 ETRIGE	**External Trigger Mode Enable** — This bit enables the external trigger on one of the AD channels or one of the ETRIG3-0 inputs as described in Table 9-5. If external trigger source is one of the AD channels, the digital input buffer of this channel is enabled. The external trigger allows to synchronize the start of conversion with external events. External trigger will not work while converting in stop mode. 0 Disable external trigger 1 Enable external trigger

Table 9-15. Analog Input Channel Select Coding

SC	CD	CC	CB	CA	Analog Input Channel
0	0	0	0	0	AN0
	0	0	0	1	AN1
	0	0	1	0	AN2
	0	0	1	1	AN3
	0	1	0	0	AN4
	0	1	0	1	AN5
	0	1	1	0	AN6
	0	1	1	1	AN7
	1	0	0	0	AN8
	1	0	0	1	AN9
	1	0	1	0	AN9
	1	0	1	1	AN9
	1	1	0	0	AN9
	1	1	0	1	AN9
	1	1	1	0	AN9
	1	1	1	1	AN9
1	0	0	0	0	Reserved
	0	0	0	1	SPECIAL17
	0	0	1	X	Reserved
	0	1	0	0	V_{RH}
	0	1	0	1	V_{RL}
	0	1	1	0	$(V_{RH}+V_{RL}) / 2$
	0	1	1	1	Reserved
	1	X	X	X	Reserved

9.3.2.7 ATD Status Register 0 (ATDSTAT0)

This register contains the Sequence Complete Flag, overrun flags for external trigger and FIFO mode, and the conversion counter.

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-9. ATD Status Register 0 (ATDSTAT0)

Chapter 10
Pulse-Width Modulator (PWM8B6CV1) Block Description

10.1 Introduction

The pulse width modulation (PWM) definition is based on the HC12 PWM definitions. The PWM8B6CV1 module contains the basic features from the HC11 with some of the enhancements incorporated on the HC12, that is center aligned output mode and four available clock sources. The PWM8B6CV1 module has six channels with independent control of left and center aligned outputs on each channel.

Each of the six PWM channels has a programmable period and duty cycle as well as a dedicated counter. A flexible clock select scheme allows a total of four different clock sources to be used with the counters. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%. The PWM outputs can be programmed as left aligned outputs or center aligned outputs

10.1.1 Features

- Six independent PWM channels with programmable period and duty cycle
- Dedicated counter for each PWM channel
- Programmable PWM enable/disable for each channel
- Software selection of PWM duty pulse polarity for each channel
- Period and duty cycle are double buffered. Change takes effect when the end of the effective period is reached (PWM counter reaches 0) or when the channel is disabled.
- Programmable center or left aligned outputs on individual channels
- Six 8-bit channel or three 16-bit channel PWM resolution
- Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies.
- Programmable clock select logic
- Emergency shutdown

10.1.2 Modes of Operation

There is a software programmable option for low power consumption in wait mode that disables the input clock to the prescaler.

In freeze mode there is a software programmable option to disable the input clock to the prescaler. This is useful for emulation.

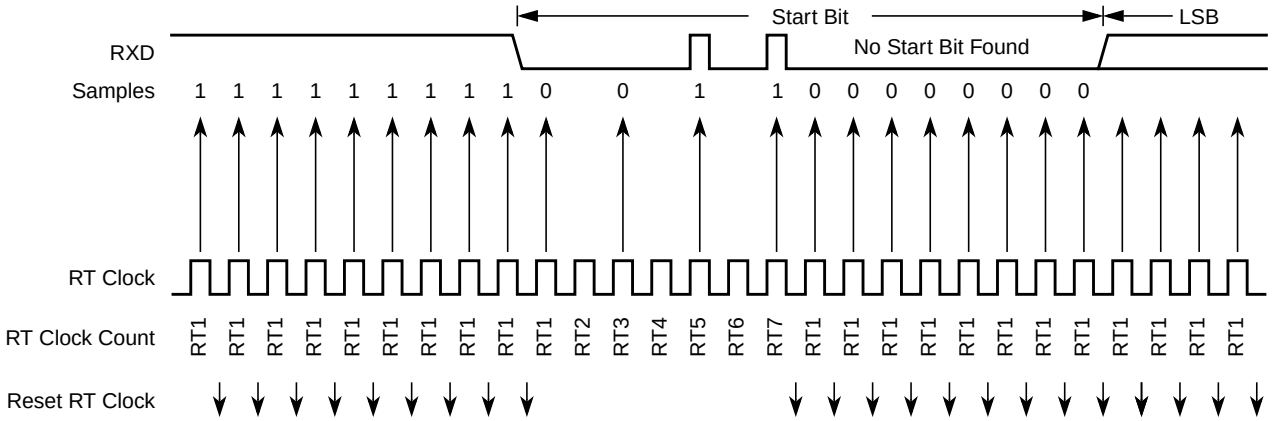


Figure 11-26. Start Bit Search Example 5

In Figure 11-27, a noise burst makes the majority of data samples RT8, RT9, and RT10 high. This sets the noise flag but does not reset the RT clock. In start bits only, the RT8, RT9, and RT10 data samples are ignored.

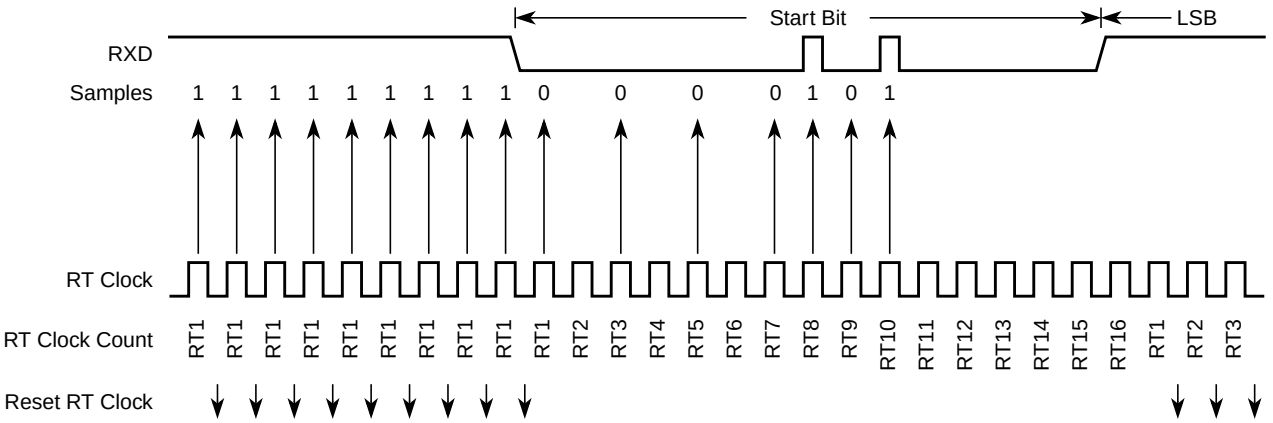


Figure 11-27. Start Bit Search Example 6

11.4.6.4 Framing Errors

If the data recovery logic does not detect a logic 1 where the stop bit should be in an incoming frame, it sets the framing error flag, FE, in SCI status register 1 (SCISR1). A break character also sets the FE flag because a break character has no stop bit. The FE flag is set at the same time that the RDRF flag is set.

11.4.6.5 Baud Rate Tolerance

A transmitting device may be operating at a baud rate below or above the receiver baud rate. Accumulated bit time misalignment can cause one of the three stop bit data samples (RT8, RT9, and RT10) to fall outside the actual stop bit. A noise error will occur if the RT8, RT9, and RT10 samples are not all the same logical values. A framing error will occur if the receiver clock is misaligned in such a way that the majority of the RT8, RT9, and RT10 stop bit samples are a logic zero.

12.3.2.5 SPI Data Register (SPIDR = SPIDRH:SPIDRL)

Module Base +0x0004

	7	6	5	4	3	2	1	0
R	R15	R14	R13	R12	R11	R10	R9	R8
W	T15	T14	T13	T12	T11	T10	T9	T8
Reset	0	0	0	0	0	0	0	0

Figure 12-7. SPI Data Register High (SPIDRH)

Module Base +0x0005

	7	6	5	4	3	2	1	0
R	R7	R6	R5	R4	R3	R2	R1	R0
W	T7	T6	T5	T4	T3	T2	T1	T0
Reset	0	0	0	0	0	0	0	0

Figure 12-8. SPI Data Register Low (SPIDRL)

Read: Anytime; read data only valid when SPIF is set

Write: Anytime

The SPI data register is both the input and output register for SPI data. A write to this register allows data to be queued and transmitted. For an SPI configured as a master, queued data is transmitted immediately after the previous transmission has completed. The SPI transmitter empty flag SPTEF in the SPISR register indicates when the SPI data register is ready to accept new data.

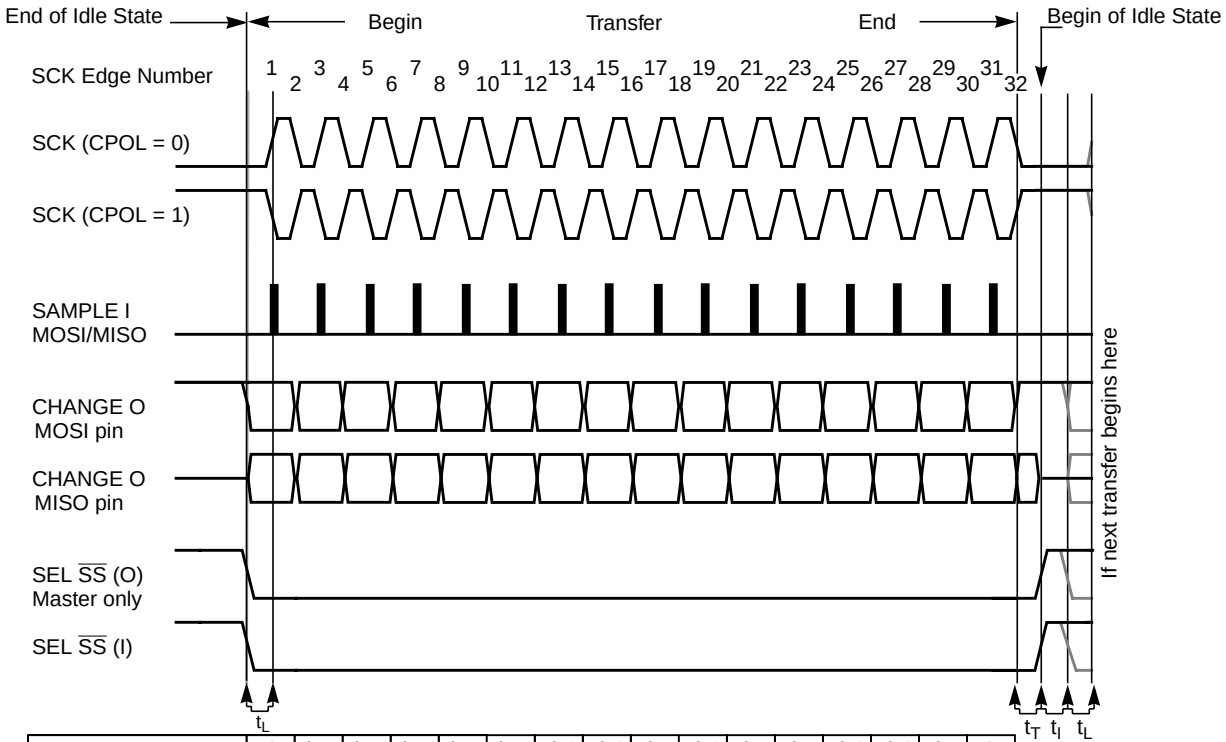
Received data in the SPIDR is valid when SPIF is set.

If SPIF is cleared and data has been received, the received data is transferred from the receive shift register to the SPIDR and SPIF is set.

If SPIF is set and not serviced, and a second data value has been received, the second received data is kept as valid data in the receive shift register until the start of another transmission. The data in the SPIDR does not change.

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced before the start of a third transmission, the data in the receive shift register is transferred into the SPIDR and SPIF remains set (see Figure 12-9).

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced after the start of a third transmission, the data in the receive shift register has become invalid and is not transferred into the SPIDR (see Figure 12-10).



t_L = Minimum leading time before the first SCK edge
t_T = Minimum trailing time after the last SCK edge
t_l = Minimum idling time between transfers (minimum $\overline{SS}$ high time)
t_L, t_T, and t_l are guaranteed for the master mode and required for the slave mode.

Figure 12-13. SPI Clock Format 0 (CPHA = 0), with 16-Bit Transfer Width selected (XFRW = 1)

In slave mode, if the $\overline{SS}$ line is not deasserted between the successive transmissions then the content of the SPI data register is not transmitted; instead the last received data is transmitted. If the $\overline{SS}$ line is deasserted for at least minimum idle time (half SCK cycle) between successive transmissions, then the content of the SPI data register is transmitted.

In master mode, with slave select output enabled the $\overline{SS}$ line is always deasserted and reasserted between successive transfers for at least minimum idle time.

12.4.3.3 CPHA = 1 Transfer Format

Some peripherals require the first SCK edge before the first data bit becomes available at the data out pin, the second edge clocks data into the system. In this format, the first SCK edge is issued by setting the CPHA bit at the beginning of the n[1]-cycle transfer operation.

The first edge of SCK occurs immediately after the half SCK clock cycle synchronization delay. This first edge commands the slave to transfer its first data bit to the serial data input pin of the master.

A half SCK cycle later, the second edge appears on the SCK pin. This is the latching edge for both the master and slave.

1. n depends on the selected transfer width, please refer to Section 12.3.2.2, “SPI Control Register 2 (SPICR2)

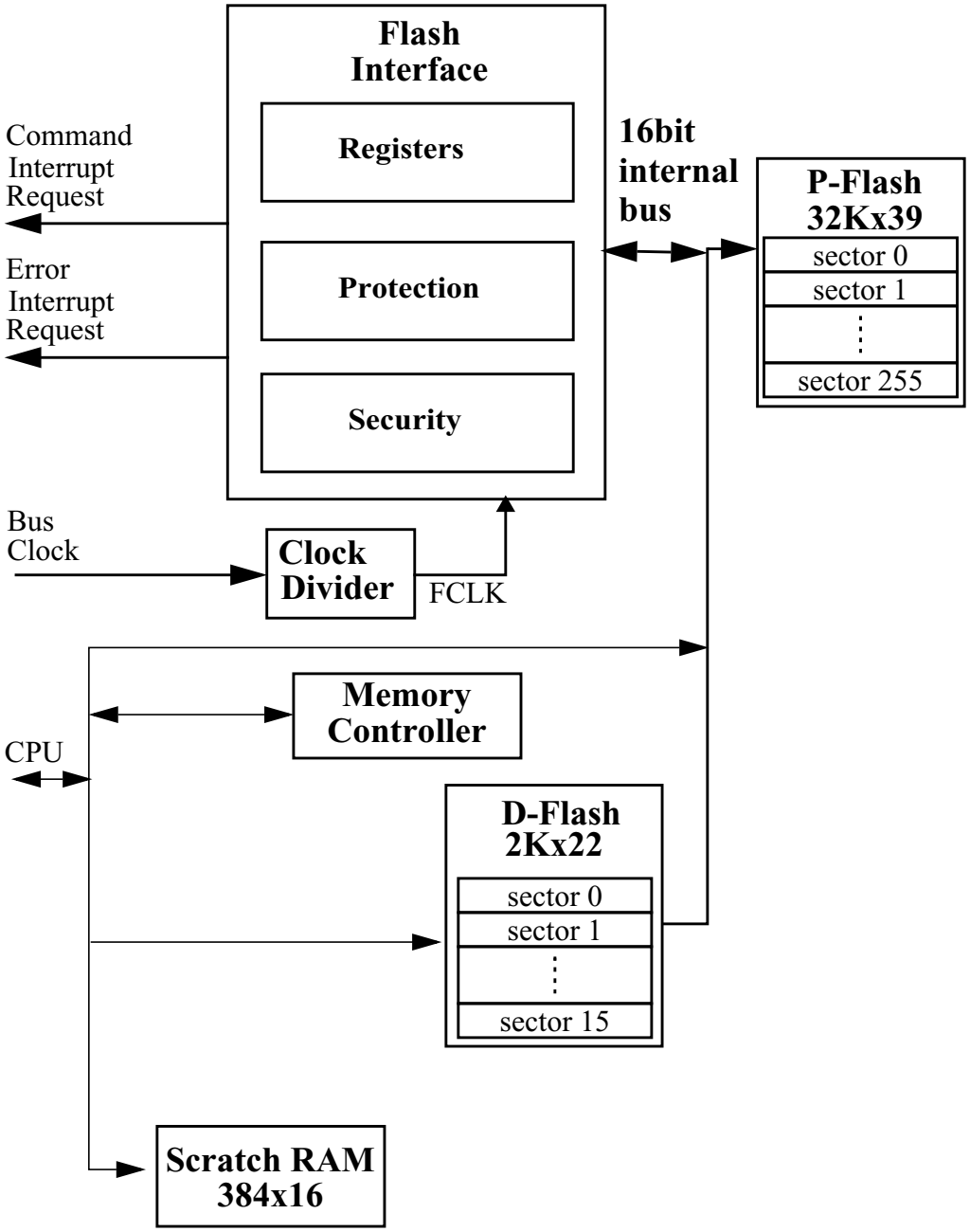


Figure 13-1. FTMRC128K1 Block Diagram

13.2 External Signal Description

The Flash module contains no signals that connect off-chip.

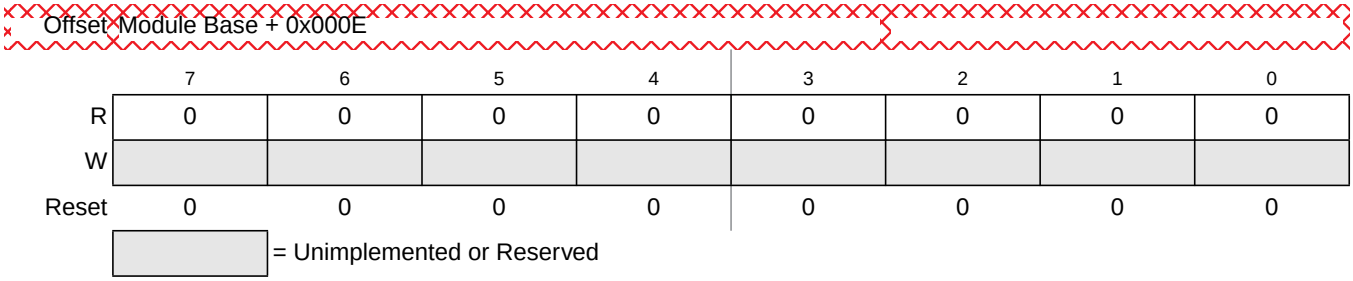


Figure 13-20. Flash Reserved3 Register (FRSV3)

All bits in the FRSV3 register read 0 and are not writable.

13.3.2.15 Flash Reserved4 Register (FRSV4)

This Flash register is reserved for factory testing.

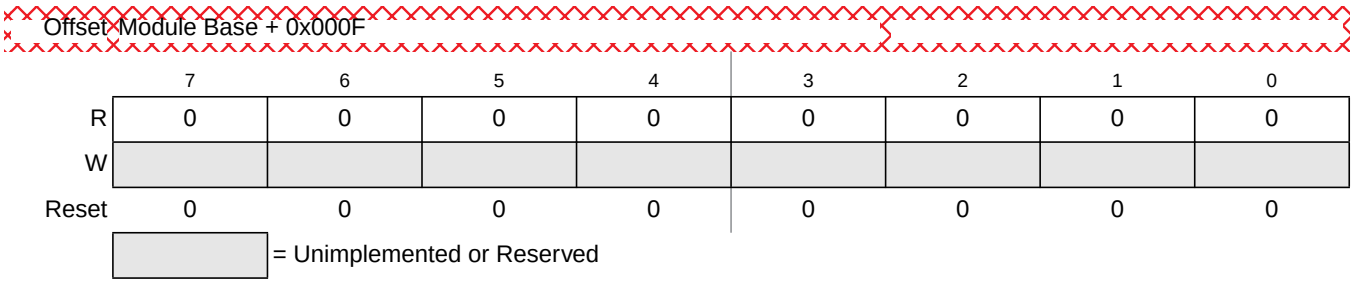


Figure 13-21. Flash Reserved4 Register (FRSV4)

All bits in the FRSV4 register read 0 and are not writable.

13.3.2.16 Flash Option Register (FOPT)

The FOPT register is the Flash option register.

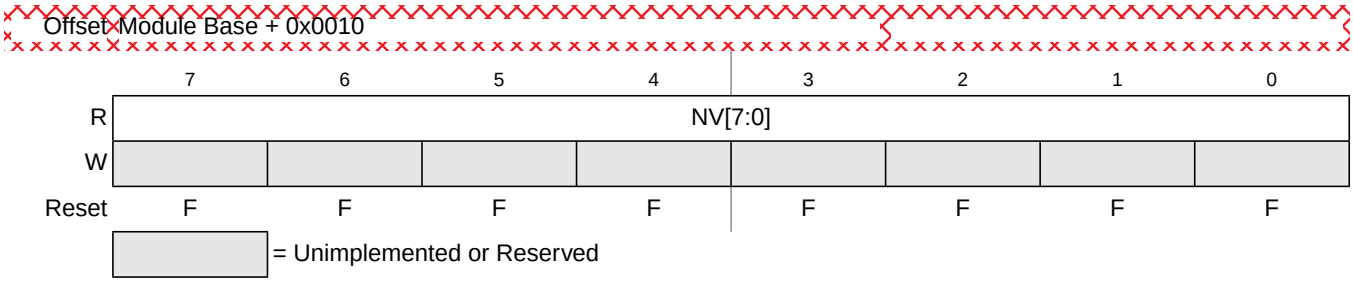


Figure 13-22. Flash Option Register (FOPT)

All bits in the FOPT register are readable but are not writable.

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field at global address 0x3_FF0E located in P-Flash memory (see Table 13-3) as indicated by reset condition F in Figure 13-22. If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

A.1.9 I/O Characteristics

This section describes the characteristics of all I/O pins except EXTAL, XTAL, TEST and supply pins.

Table A-6. 3.3-V I/O Characteristics
ALL 3.3V RANGE I/O PARAMETERS ARE SUBJECT TO CHANGE FOLLOWING CHARACTERIZATION

Conditions are 3.15 V < V_{DD35} < 3.6 V junction temperature from –40°C to +150°C, unless otherwise noted
I/O Characteristics for all I/O pins except EXTAL, XTAL,TEST and supply pins.

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Input high voltage	V_{IH}	0.65*V_{DD35}	—	—	V
	T	Input high voltage	V_{IH}	—	—	V_{DD35} + 0.3	V
2	P	Input low voltage	V_{IL}	—	—	0.35*V_{DD35}	V
	T	Input low voltage	V_{IL}	V_{SS35} – 0.3	—	—	V
3	C	Input hysteresis	V_{HYS}		250		mV
4	 P C C	Input leakage current (pins in high impedance input mode)[1] V_{in} = V_{DD35} or V_{SS35} **M** temperature range –40°C to +150°C **V** temperature range –40°C to +125°C **C** temperature range –40°C to +105°C	I_{in}	 –1.00 -0.75 -0.50	 — — —	 1.00 0.75 0.50	µA
5	C	Output high voltage (pins in output mode) Partial drive I_{OH} = –0.75 mA	V_{OH}	V_{DD35} – 0.4	—	—	V
6	P	Output high voltage (pins in output mode) Full drive I_{OH} = –4 mA	V_{OH}	V_{DD35} – 0.4	—	—	V
7	C	Output low voltage (pins in output mode) Partial Drive I_{OL} = +0.9 mA	V_{OL}	—	—	0.4	V
8	P	Output low voltage (pins in output mode) Full Drive I_{OL} = +4.75 mA	V_{OL}	—	—	0.4	V
9	P	Internal pull up resistance V_{IH} min > input voltage > V_{IL} max	R_{PUL}	25	—	50	KΩ
10	P	Internal pull down resistance V_{IH} min > input voltage > V_{IL} max	R_{PDH}	25	—	50	KΩ
11	D	Input capacitance	C_{in}	—	6	—	pF
12	T	Injection current[2] Single pin limit Total device limit, sum of all injected currents	 I_{ICS} I_{ICP}	 –2.5 –25	—	 2.5 25	mA
13	P	Port J, P interrupt input pulse filtered (STOP)[3]	t_{PULSE}	—	—	3	µs
14	P	Port J, P interrupt input pulse passed (STOP)[3]	t_{PULSE}	10	—	—	µs
15	D	Port J, P interrupt input pulse filtered ($\overline{\text{STOP}}$)	t_{PULSE}	—	—	3	tcyc
16	D	Port J, P interrupt input pulse passed ($\overline{\text{STOP}}$)	t_{PULSE}	4	—	—	tcyc
17	D	$\overline{\text{IRQ}}$ pulse width, edge-sensitive mode ($\overline{\text{STOP}}$)	PW_{IRQ}	1	—	—	tcyc

1. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8°C to 12 C° in the temperature range from 50°C to 125°C.
2. Refer to Section A.1.4, “Current Injection” for more details
3. Parameter only applies in stop or pseudo stop mode.