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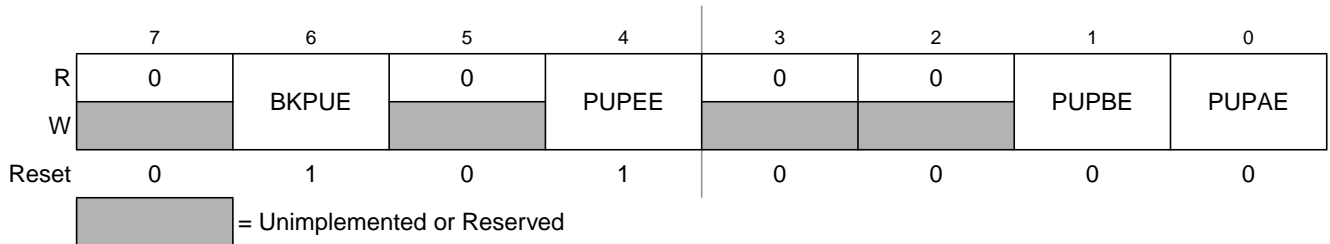
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TFQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12p96mft">https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12p96mft</a>

### 2.3.10 Ports A, B, E, BKGD pin Pull-up Control Register (PUCR)

Address 0x000C

Access: User read/write<sup>(1)</sup>


**Figure 2-8. Ports ABEK, BKGD pin Pull-up Control Register (PUCR)**

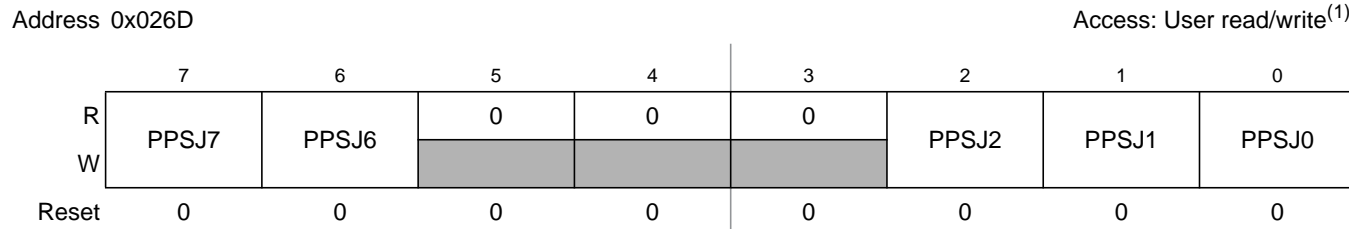
1. Read:Anytime in single-chip modes.

Write:Anytime, except BKPUE which is writable in Special Single-Chip Mode only.

**Table 2-10. PUCR Register Field Descriptions**

Field	Description
6 BKPUE	<b>BKGD pin pull-up Enable</b> —Enable pull-up device on pin This bit configures whether a pull-up device is activated, if the pin is used as input. If a pin is used as output this bit has no effect.  1 Pull-up device enabled 0 Pull-up device disabled
4 PUPEE	<b>Port E Pull-up Enable</b> —Enable pull-up devices on all port input pins except pins 5 and 6 This bit configures whether a pull-up device is activated on all associated port input pins. If a pin is used as output this bit has no effect. Pins 5 and 6 have pull-down devices enabled only during reset. This bit has no effect on these pins.  1 Pull-up device enabled 0 Pull-up device disabled
1 PUPBE	<b>Port B Pull-up Enable</b> —Enable pull-up devices on all port input pins This bit configures whether a pull-up device is activated on all associated port input pins. If a pin is used as output this bit has no effect.  1 Pull-up device enabled 0 Pull-up device disabled
0 PUPAE	<b>Port A Pull-up Enable</b> —Enable pull-up devices on all port input pins This bit configures whether a pull-up device is activated on all associated port input pins. If a pin is used as output this bit has no effect.  1 Pull-up device enabled 0 Pull-up device disabled

### 2.3.54 Port J Polarity Select Register (PPSJ)



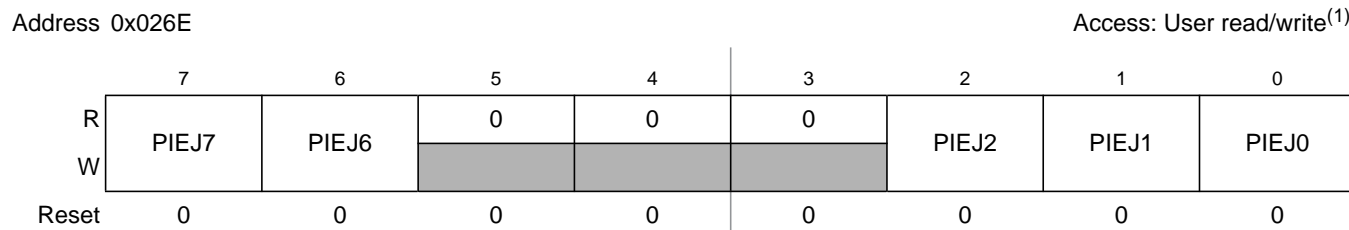
**Figure 2-52. Port J Polarity Select Register (PPSJ)**

1. Read: Anytime  
Write: Anytime

**Table 2-48. PPSJ Register Field Descriptions**

Field	Description
7-6, 2-0 PPSJ	<b>Port J pull device select</b> —Configure pull device and pin interrupt edge polarity on input pin This bit selects a pull-up or a pull-down device if enabled on the associated port input pin. This bit also selects the polarity of the active pin interrupt edge.  1 A pull-down device is selected; rising edge selected 0 A pull-up device is selected; falling edge selected

### 2.3.55 Port J Interrupt Enable Register (PIEJ)



**Figure 2-53. Port J Interrupt Enable Register (PIEJ)**

1. Read: Anytime  
Write: Anytime

**Table 2-49. PIEJ Register Field Descriptions**

Field	Description
7-6, 2-0 PIEJ	<b>Port J interrupt enable</b> — This bit enables or disables on the edge sensitive pin interrupt on the associated pin.  1 Interrupt is enabled 0 Interrupt is disabled (interrupt flag masked)

### 5.3.3 Family ID Assignment

The family ID is an 8-bit value located in the BDM ROM in active BDM (at global address: 0x3\_FF0F). The read-only value is a unique family ID which is 0xC2 for devices with an HCS12S core.

## 5.4 Functional Description

The BDM receives and executes commands from a host via a single wire serial interface. There are two types of BDM commands: hardware and firmware commands.

Hardware commands are used to read and write target system memory locations and to enter active background debug mode, see [Section 5.4.3, “BDM Hardware Commands”](#). Target system memory includes all memory that is accessible by the CPU.

Firmware commands are used to read and write CPU resources and to exit from active background debug mode, see [Section 5.4.4, “Standard BDM Firmware Commands”](#). The CPU resources referred to are the accumulator (D), X index register (X), Y index register (Y), stack pointer (SP), and program counter (PC).

Hardware commands can be executed at any time and in any mode excluding a few exceptions as highlighted (see [Section 5.4.3, “BDM Hardware Commands”](#)) and in secure mode (see [Section 5.4.1, “Security”](#)). BDM firmware commands can only be executed when the system is not secure and is in active background debug mode (BDM).

### 5.4.1 Security

If the user resets into special single chip mode with the system secured, a secured mode BDM firmware lookup table is brought into the map overlapping a portion of the standard BDM firmware lookup table. The secure BDM firmware verifies that the on-chip Flash EEPROM are erased. This being the case, the UNSEC and ENBDM bit will get set. The BDM program jumps to the start of the standard BDM firmware and the secured mode BDM firmware is turned off and all BDM commands are allowed. If the Flash does not verify as erased, the BDM firmware sets the ENBDM bit, without asserting UNSEC, and the firmware enters a loop. This causes the BDM hardware commands to become enabled, but does not enable the firmware commands. This allows the BDM hardware to be used to erase the Flash.

BDM operation is not possible in any other mode than special single chip mode when the device is secured. The device can only be unsecured via BDM serial interface in special single chip mode. For more information regarding security, please see the S12S\_9SEC Block Guide.

### 5.4.2 Enabling and Activating BDM

The system must be in active BDM to execute standard BDM firmware commands. BDM can be activated only after being enabled. BDM is enabled by setting the ENBDM bit in the BDM status (BDMSTS) register. The ENBDM bit is set by writing to the BDM status (BDMSTS) register, via the single-wire interface, using a hardware command such as WRITE\_BD\_BYTE.

After being enabled, BDM is activated by one of the following<sup>1</sup>:

- Hardware BACKGROUND command

1. BDM is enabled and active immediately out of special single-chip reset.

Since the host knows the target serial clock frequency, the SYNC command (used to abort a command) does not need to consider the lower possible target frequency. In this case, the host could issue a SYNC very close to the 128 serial clock cycles length. Providing a small overhead on the pulse length in order to assure the SYNC pulse will not be misinterpreted by the target. See [Section 5.4.9, “SYNC — Request Timed Reference Pulse”](#).

Figure 5-12 shows a SYNC command being issued after a READ\_BYTE, which aborts the READ\_BYTE command. Note that, after the command is aborted a new command could be issued by the host computer.

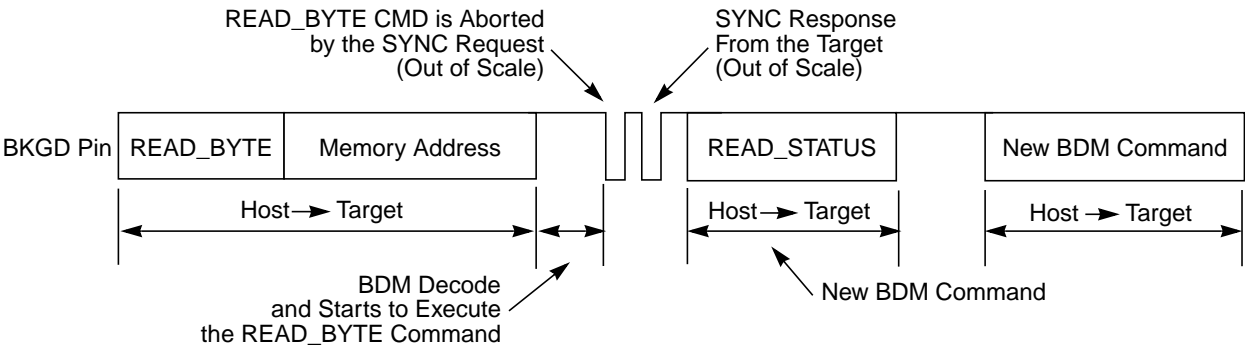


Figure 5-12. ACK Abort Procedure at the Command Level

**NOTE**

Figure 5-12 does not represent the signals in a true timing scale

Figure 5-13 shows a conflict between the ACK pulse and the SYNC request pulse. This conflict could occur if a POD device is connected to the target BKGD pin and the target is already in debug active mode. Consider that the target CPU is executing a pending BDM command at the exact moment the POD is being connected to the BKGD pin. In this case, an ACK pulse is issued along with the SYNC command. In this case, there is an electrical conflict between the ACK speedup pulse and the SYNC pulse. Since this is not a probable situation, the protocol does not prevent this conflict from happening.

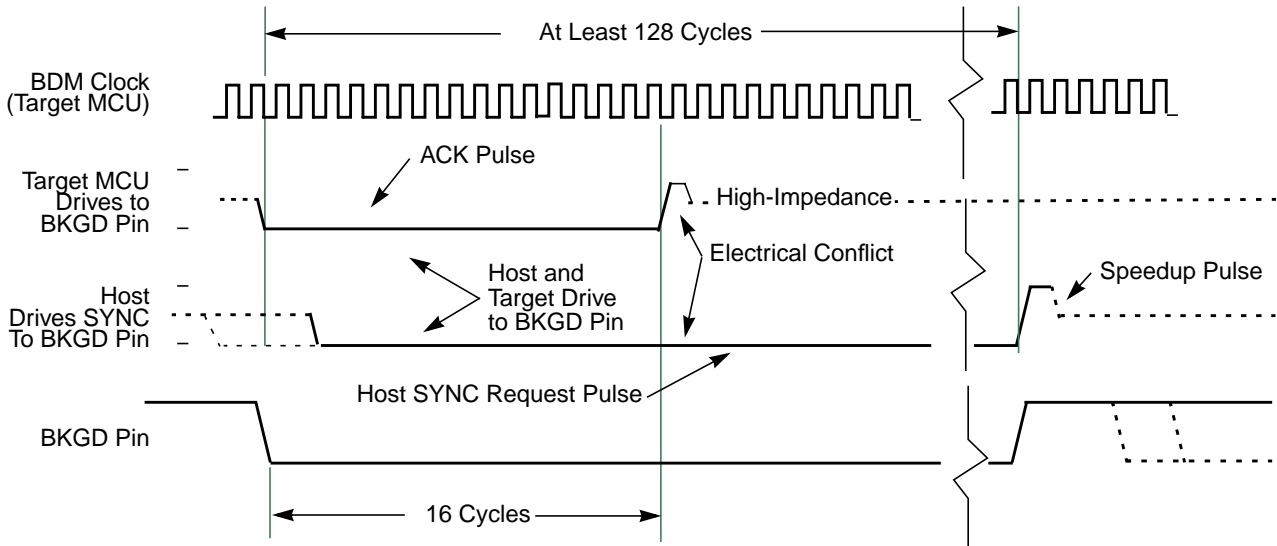
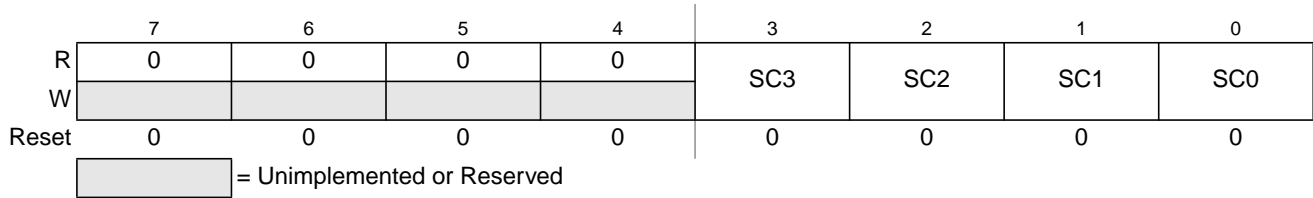


Figure 5-13. ACK Pulse and SYNC Request Conflict

### 6.3.2.7.3 Debug State Control Register 3 (DBGSCR3)

Address: 0x0027



**Figure 6-11. Debug State Control Register 3 (DBGSCR3)**

Read: If COMRV[1:0] = 10

Write: If COMRV[1:0] = 10 and DBG is not armed.

This register is visible at 0x0027 only with COMRV[1:0] = 10. The state control register three selects the targeted next state whilst in State3. The matches refer to the match channels of the comparator match control logic as depicted in [Figure 6-1](#) and described in [6.3.2.8.1](#). Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

**Table 6-19. DBGSCR3 Field Descriptions**

Field	Description
3–0 SC[3:0]	These bits select the targeted next state whilst in State3, based upon the match event.

**Table 6-20. State3 — Sequencer Next State Selection**

SC[3:0]	Description (Unspecified matches have no effect)
0000	Match0 to State1
0001	Match2 to State2..... Match1 to Final State
0010	Match0 to Final State..... Match1 to State1
0011	Match1 to Final State..... Match2 to State1
0100	Match1 to State2
0101	Match1 to Final State
0110	Match2 to State2..... Match0 to Final State
0111	Match0 to Final State
1000	Reserved
1001	Reserved
1010	Either Match1 or Match2 to State1..... Match0 to Final State
1011	Reserved
1100	Reserved
1101	Either Match1 or Match2 to Final State..... Match0 to State1
1110	Match0 to State2..... Match2 to Final State
1111	Reserved

The priorities described in [Table 6-36](#) dictate that in the case of simultaneous matches, a match leading to final state has priority followed by the match on the lower channel number (0,1,2).

Table 6-26. DBGXAM Field Descriptions

Field	Description
7–0 Bit[15:8]	<b>Comparator Address Mid Compare Bits</b> — The Comparator address mid compare bits control whether the selected comparator compares the address bus bits [15:8] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

### 6.3.2.8.4 Debug Comparator Address Low Register (DBGXAL)

Address: 0x002B

	7	6	5	4	3	2	1	0
R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								
Reset	0	0	0	0	0	0	0	0

Figure 6-18. Debug Comparator Address Low Register (DBGXAL)

Read: Anytime. See Table 6-24 for visible register encoding.

Write: If DBG not armed. See Table 6-24 for visible register encoding.

Table 6-27. DBGXAL Field Descriptions

Field	Description
7–0 Bits[7:0]	<b>Comparator Address Low Compare Bits</b> — The Comparator address low compare bits control whether the selected comparator compares the address bus bits [7:0] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

### 6.3.2.8.5 Debug Comparator Data High Register (DBGADH)

Address: 0x002C

	7	6	5	4	3	2	1	0
R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
Reset	0	0	0	0	0	0	0	0

Figure 6-19. Debug Comparator Data High Register (DBGADH)

Read: If COMRV[1:0] = 00

Write: If COMRV[1:0] = 00 and DBG not armed.

## 7.1.2 Modes of Operation

This subsection lists and briefly describes all operating modes supported by the S12CPMU.

### 7.1.2.1 Run Mode

The voltage regulator is in Full Performance Mode (FPM).

The Phase Locked Loop (PLL) is on.

The Internal Reference Clock (IRC1M) is on.

The API is available.

- **PLL Engaged Internal (PEI)**
  - This is the default mode after System Reset and Power-On Reset.
  - The Bus Clock is based on the PLLCLK.
  - After reset the PLL is configured for 64MHz VCOCLK operation  
Post divider is 0x03, so PLLCLK is VCOCLK divided by 4, that is 16MHz and Bus Clock is 8MHz.  
The PLL can be re-configured for other bus frequencies.
  - The reference clock for the PLL (REFCLK) is based on internal reference clock IRC1M
- **PLL Engaged External (PEE)**
  - The Bus Clock is based on the PLLCLK.
  - This mode can be entered from default mode PEI by performing the following steps:
    - Configure the PLL for desired bus frequency.
    - Program the reference divider (REFDIV[3:0] bits) to divide down oscillator frequency if necessary.
    - Enable the external oscillator (OSCE bit)
- **PLL Bypassed External (PBE)**
  - The Bus Clock is based on the Oscillator Clock (OSCCLK).
  - This mode can be entered from default mode PEI by performing the following steps:
    - Enable the external oscillator (OSCE bit)
    - Wait for oscillator to start up (UPOSC=1)
    - Select the Oscillator Clock (OSCCLK) as Bus Clock (PLLSEL=0).
  - The PLLCLK is still on to filter possible spikes of the external oscillator clock.

### 7.1.2.2 Wait Mode

For S12CPMU Wait Mode is the same as Run Mode.



Write: Refer to each bit for individual write conditions

**Table 7-3. CPMUFLG Field Descriptions**

Field	Description
7 RTIF	<b>Real Time Interrupt Flag</b> — RTIF is set to 1 at the end of the RTI period. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (RTIE=1), RTIF causes an interrupt request. 0 RTI time-out has not yet occurred. 1 RTI time-out has occurred.
6 PORF	<b>Power on Reset Flag</b> — PORF is set to 1 when a power on reset occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Power on reset has not occurred. 1 Power on reset has occurred.
5 LVRF	<b>Low Voltage Reset Flag</b> — LVRF is set to 1 when a low voltage reset occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Low voltage reset has not occurred. 1 Low voltage reset has occurred.
4 LOCKIF	<b>PLL Lock Interrupt Flag</b> — LOCKIF is set to 1 when LOCK status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (LOCKIE=1), LOCKIF causes an interrupt request. 0 No change in LOCK bit. 1 LOCK bit has changed.
3 LOCK	<b>Lock Status Bit</b> — LOCK reflects the current state of PLL lock condition. Writes have no effect. While PLL is unlocked (LOCK=0) $f_{PLL}$ is $f_{VCO} / 4$ to protect the system from high core clock frequencies during the PLL stabilization time clock. 0 VCOCLK is not within the desired tolerance of the target frequency. $f_{PLL} = f_{VCO}/4$ . 1 VCOCLK is within the desired tolerance of the target frequency. $f_{PLL} = f_{VCO}/(POSTDIV+1)$ .
2 ILAF	<b>Illegal Address Reset Flag</b> — ILAF is set to 1 when an illegal address reset occurs. Refer to MMC chapter for details. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Illegal address reset has not occurred. 1 Illegal address reset has occurred.
1 OSCIF	<b>Oscillator Interrupt Flag</b> — OSCIF is set to 1 when UPOSC status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (OSCIE=1), OSCIF causes an interrupt request. 0 No change in UPOSC bit. 1 UPOSC bit has changed.
0 UPOSC	<b>Oscillator Status Bit</b> — UPOSC reflects the status of the oscillator. Writes have no effect. While UPOSC=0 the OSCCLK going to the MSCAN module is off. Entering Full Stop Mode UPOSC is cleared. 0 The oscillator is off or oscillation is not qualified by the PLL. 1 The oscillator is qualified by the PLL.

### NOTE

The adaptive spike filter uses the VCO clock as a reference to continuously qualify the external oscillator clock. Because of this, the PLL is always active and a valid PLL configuration is required for the system to work properly. Furthermore, the adaptive spike filter is used to determine the status of the external oscillator (reflected in the UPOSC bit). Since this function also relies on the VCO clock, losing PLL lock status (LOCK=0, except for entering Pseudo Stop Mode) means losing the oscillator status information as well (UPOSC=0).

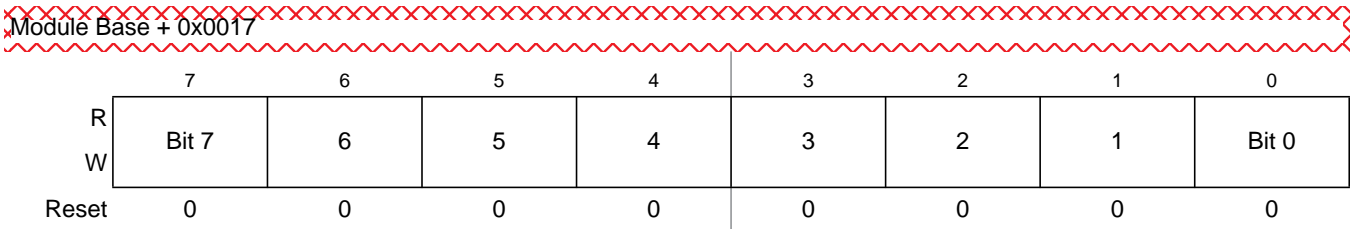


Figure 10-26. PWM Channel Period Registers (PWMPER5)

Read: anytime

Write: anytime

### 10.3.2.14 PWM Channel Duty Registers (PWMDTYx)

There is a dedicated duty register for each channel. The value in this register determines the duty of the associated PWM channel. The duty value is compared to the counter and if it is equal to the counter value a match occurs and the output changes state.

The duty registers for each channel are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to 0x0000)
- The channel is disabled

In this way, the output of the PWM will always be either the old duty waveform or the new duty waveform, not some variation in between. If the channel is not enabled, then writes to the duty register will go directly to the latches as well as the buffer.

#### NOTE

Reads of this register return the most recent value written. Reads do not necessarily return the value of the currently active duty due to the double buffering scheme.

Reference [Section 10.4.2.3, “PWM Period and Duty,”](#) for more information.

#### NOTE

Depending on the polarity bit, the duty registers will contain the count of either the high time or the low time. If the polarity bit is 1, the output starts high and then goes low when the duty count is reached, so the duty registers contain a count of the high time. If the polarity bit is 0, the output starts low and then goes high when the duty count is reached, so the duty registers contain a count of the low time.

To calculate the output duty cycle (high time as a % of period) for a particular channel:

- Polarity = 0 (PPOLx = 0)  
Duty cycle = [(PWMPERx PWMDTYx)/PWMPERx] \* 100%
- Polarity = 1 (PPOLx = 1)  
Duty cycle = [PWMDTYx / PWMPERx] \* 100%

## 12.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

### 12.3.2.1 SPI Control Register 1 (SPICR1)

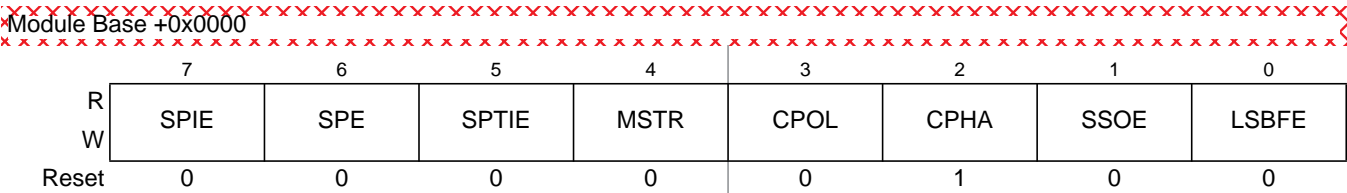


Figure 12-3. SPI Control Register 1 (SPICR1)

Read: Anytime

Write: Anytime

Table 12-2. SPICR1 Field Descriptions

Field	Description
7 SPIE	<b>SPI Interrupt Enable Bit</b> — This bit enables SPI interrupt requests, if SPIF or MODF status flag is set. 0 SPI interrupts disabled. 1 SPI interrupts enabled.
6 SPE	<b>SPI System Enable Bit</b> — This bit enables the SPI system and dedicates the SPI port pins to SPI system functions. If SPE is cleared, SPI is disabled and forced into idle state, status bits in SPISR register are reset. 0 SPI disabled (lower power consumption). 1 SPI enabled, port pins are dedicated to SPI functions.
5 SPTIE	<b>SPI Transmit Interrupt Enable</b> — This bit enables SPI interrupt requests, if SPTEF flag is set. 0 SPTEF interrupt disabled. 1 SPTEF interrupt enabled.
4 MSTR	<b>SPI Master/Slave Mode Select Bit</b> — This bit selects whether the SPI operates in master or slave mode. Switching the SPI from master to slave or vice versa forces the SPI system into idle state. 0 SPI is in slave mode. 1 SPI is in master mode.
3 CPOL	<b>SPI Clock Polarity Bit</b> — This bit selects an inverted or non-inverted SPI clock. To transmit data between SPI modules, the SPI modules must have identical CPOL values. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Active-high clocks selected. In idle state SCK is low. 1 Active-low clocks selected. In idle state SCK is high.
2 CPHA	<b>SPI Clock Phase Bit</b> — This bit is used to select the SPI clock format. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Sampling of data occurs at odd edges (1,3,5,...) of the SCK clock. 1 Sampling of data occurs at even edges (2,4,6,...) of the SCK clock.

The CPOL clock polarity control bit specifies an active high or low clock and has no significant effect on the transmission format.

The CPHA clock phase control bit selects one of two fundamentally different transmission formats.

Clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transmissions to allow a master device to communicate with peripheral slaves having different requirements.

### 12.4.3.2 CPHA = 0 Transfer Format

The first edge on the SCK line is used to clock the first data bit of the slave into the master and the first data bit of the master into the slave. In some peripherals, the first bit of the slave's data is available at the slave's data out pin as soon as the slave is selected. In this format, the first SCK edge is issued a half cycle after  $\overline{SS}$  has become low.

A half SCK cycle later, the second edge appears on the SCK line. When this second edge occurs, the value previously latched from the serial data input pin is shifted into the LSB or MSB of the shift register, depending on LSBFE bit.

After this second edge, the next bit of the SPI master data is transmitted out of the serial data output pin of the master to the serial input pin on the slave. This process continues for a total of 16 edges on the SCK line, with data being latched on odd numbered edges and shifted on even numbered edges.

Data reception is double buffered. Data is shifted serially into the SPI shift register during the transfer and is transferred to the parallel SPI data register after the last bit is shifted in.

After  $2n^1$  (last) SCK edges:

- Data that was previously in the master SPI data register should now be in the slave data register and the data that was in the slave data register should be in the master.
- The SPIF flag in the SPI status register is set, indicating that the transfer is complete.

Figure 12-12 is a timing diagram of an SPI transfer where CPHA = 0. SCK waveforms are shown for CPOL = 0 and CPOL = 1. The diagram may be interpreted as a master or slave timing diagram because the SCK, MISO, and MOSI pins are connected directly between the master and the slave. The MISO signal is the output from the slave and the MOSI signal is the output from the master. The  $\overline{SS}$  pin of the master must be either high or reconfigured as a general-purpose output not affecting the SPI.

1. n depends on the selected transfer width, please refer to [Section 12.3.2.2, "SPI Control Register 2 \(SPICR2\)"](#)

Table 13-7. FDIV values for various BUSCLK Frequencies

BUSCLK Frequency (MHz)		FDIV[5:0]	BUSCLK Frequency (MHz)		FDIV[5:0]
MIN <sup>(1)</sup>	MAX <sup>(2)</sup>		MIN <sup>1</sup>	MAX <sup>2</sup>	
1.0	1.6	0x00	16.6	17.6	0x10
1.6	2.6	0x01	17.6	18.6	0x11
2.6	3.6	0x02	18.6	19.6	0x12
3.6	4.6	0x03	19.6	20.6	0x13
4.6	5.6	0x04	20.6	21.6	0x14
5.6	6.6	0x05	21.6	22.6	0x15
6.6	7.6	0x06	22.6	23.6	0x16
7.6	8.6	0x07	23.6	24.6	0x17
8.6	9.6	0x08	24.6	25.6	0x18
9.6	10.6	0x09	25.6	26.6	0x19
10.6	11.6	0x0A	26.6	27.6	0x1A
11.6	12.6	0x0B	27.6	28.6	0x1B
12.6	13.6	0x0C	28.6	29.6	0x1C
13.6	14.6	0x0D	29.6	30.6	0x1D
14.6	15.6	0x0E	30.6	31.6	0x1E
15.6	16.6	0x0F	31.6	32.6	0x1F

1. BUSCLK is Greater Than this value.

2. BUSCLK is Less Than or Equal to this value.

### 13.3.2.2 Flash Security Register (FSEC)

The FSEC register holds all bits associated with the security of the MCU and Flash module.

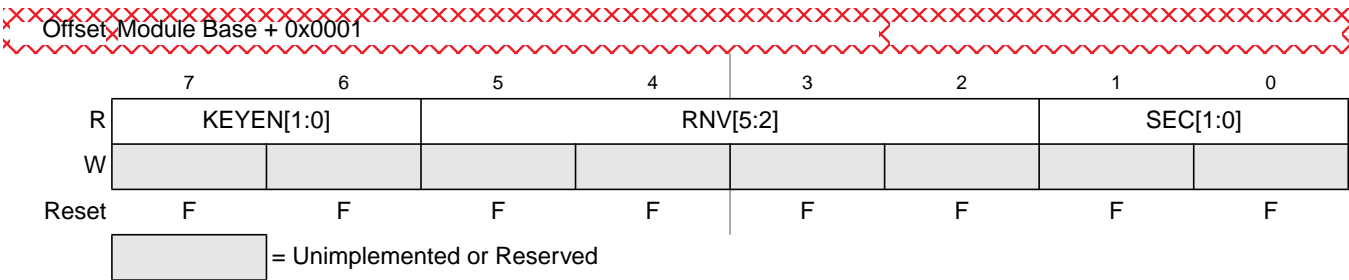


Figure 13-6. Flash Security Register (FSEC)

All bits in the FSEC register are readable but not writable.

During the reset sequence, the FSEC register is loaded with the contents of the Flash security byte in the Flash configuration field at global address 0x3\_FF0F located in P-Flash memory (see Table 13-3) as indicated by reset condition F in Figure 13-6. If a double bit fault is detected while reading the P-Flash

phrase containing the Flash security byte during the reset sequence, all bits in the FSEC register will be set to leave the Flash module in a secured state with backdoor key access disabled.

Table 13-8. FSEC Field Descriptions

Field	Description
7–6 KEYEN[1:0]	<b>Backdoor Key Security Enable Bits</b> — The KEYEN[1:0] bits define the enabling of backdoor key access to the Flash module as shown in Table 13-9.
5–2 RNV[5:2]	<b>Reserved Nonvolatile Bits</b> — The RNV bits should remain in the erased state for future enhancements.
1–0 SEC[1:0]	<b>Flash Security Bits</b> — The SEC[1:0] bits define the security state of the MCU as shown in Table 13-10. If the Flash module is unsecured using backdoor key access, the SEC bits are forced to 10.

Table 13-9. Flash KEYEN States

KEYEN[1:0]	Status of Backdoor Key Access
00	DISABLED
01	DISABLED <sup>(1)</sup>
10	ENABLED
11	DISABLED

1. Preferred KEYEN state to disable backdoor key access.

Table 13-10. Flash Security States

SEC[1:0]	Status of Security
00	SECURED
01	SECURED <sup>(1)</sup>
10	UNSECURED
11	SECURED

1. Preferred SEC state to set MCU to secured state.

The security function in the Flash module is described in Section 13.5.

13.3.2.3 Flash CCOB Index Register (FCCOBIX)

The FCCOBIX register is used to index the FCCOB register for Flash memory operations.

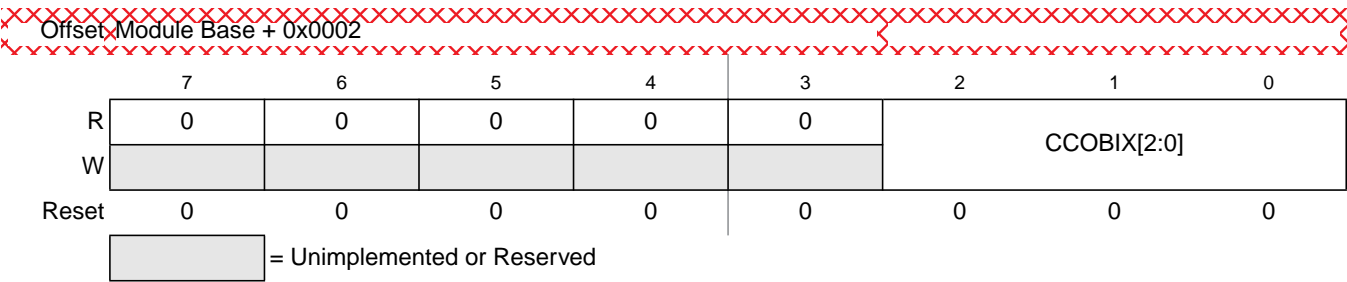


Figure 13-7. FCCOB Index Register (FCCOBIX)

CCOBIX bits are readable and writable while remaining bits read 0 and are not writable.

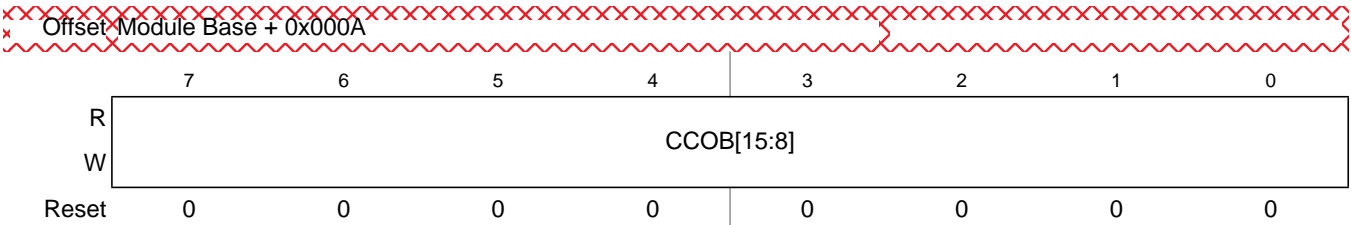


Figure 13-16. Flash Common Command Object High Register (FCCOBHI)

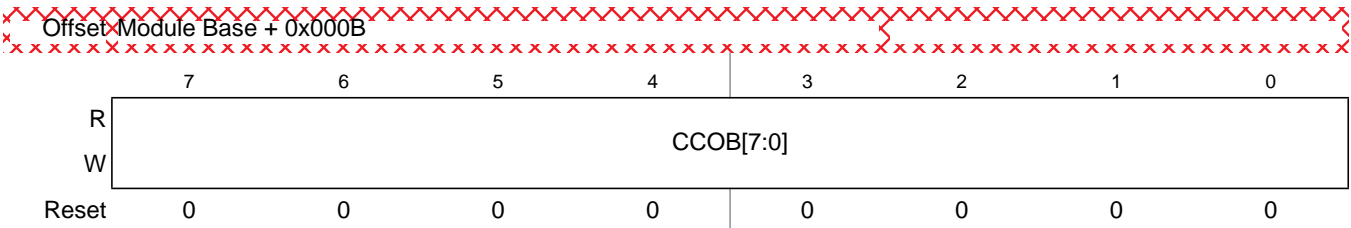


Figure 13-17. Flash Common Command Object Low Register (FCCOBLO)

13.3.2.11.1 FCCOB - NVM Command Mode

NVM command mode uses the indexed FCCOB register to provide a command code and its relevant parameters to the Memory Controller. The user first sets up all required FCCOB fields and then initiates the command’s execution by writing a 1 to the CCIF bit in the FSTAT register (a 1 written by the user clears the CCIF command completion flag to 0). When the user clears the CCIF bit in the FSTAT register all FCCOB parameter fields are locked and cannot be changed by the user until the command completes (as evidenced by the Memory Controller returning CCIF to 1). Some commands return information to the FCCOB register array.

The generic format for the FCCOB parameter fields in NVM command mode is shown in Table 13-23. The return values are available for reading after the CCIF flag in the FSTAT register has been returned to 1 by the Memory Controller. Writes to the unimplemented parameter fields (CCOBIX = 110 and CCOBIX = 111) are ignored with reads from these fields returning 0x0000.

Table 13-23 shows the generic Flash command format. The high byte of the first word in the CCOB array contains the command code, followed by the parameters for this specific Flash command. For details on the FCCOB settings required by each command, see the Flash command descriptions in Section 13.4.5.

Table 13-23. FCCOB - NVM Command Mode (Typical Usage)

CCOBIX[2:0]	Byte	FCCOB Parameter Fields (NVM Command Mode)
000	HI	FCMD[7:0] defining Flash command
	LO	6'h0, Global address [17:16]
001	HI	Global address [15:8]
	LO	Global address [7:0]
010	HI	Data 0 [15:8]
	LO	Data 0 [7:0]

**NOTE**

In the following context  $V_{DD35}$  is used for either VDDA, VDDR, and VDDX;  $V_{SS35}$  is used for either VSSA and VSSX unless otherwise noted.

$I_{DD35}$  denotes the sum of the currents flowing into the VDDA, VDDX and VDDR pins.

**A.1.3 Pins**

There are four groups of functional pins.

**A.1.3.1 I/O Pins**

The I/O pins have a level in the range of 3.15V to 5.5V. This class of pins is comprised of all port I/O pins, the analog inputs, BKGD and the RESET pins. Some functionality may be disabled.

**A.1.3.2 Analog Reference**

This group is made up by the VRH and VRL pins.

**A.1.3.3 Oscillator**

The pins EXTAL, XTAL dedicated to the oscillator have a nominal 1.8V level.

**A.1.3.4 TEST**

This pin is used for production testing only. The TEST pin must be tied to ground in all applications.

**A.1.4 Current Injection**

Power supply must maintain regulation within operating  $V_{DD35}$  or  $V_{DD}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{in} > V_{DD35}$ ) is greater than  $I_{DD35}$ , the injection current may flow out of  $V_{DD35}$  and could result in external power supply going out of regulation. Ensure external  $V_{DD35}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power; e.g., if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

**A.1.5 Absolute Maximum Ratings**

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either  $V_{SS35}$  or  $V_{DD35}$ ).



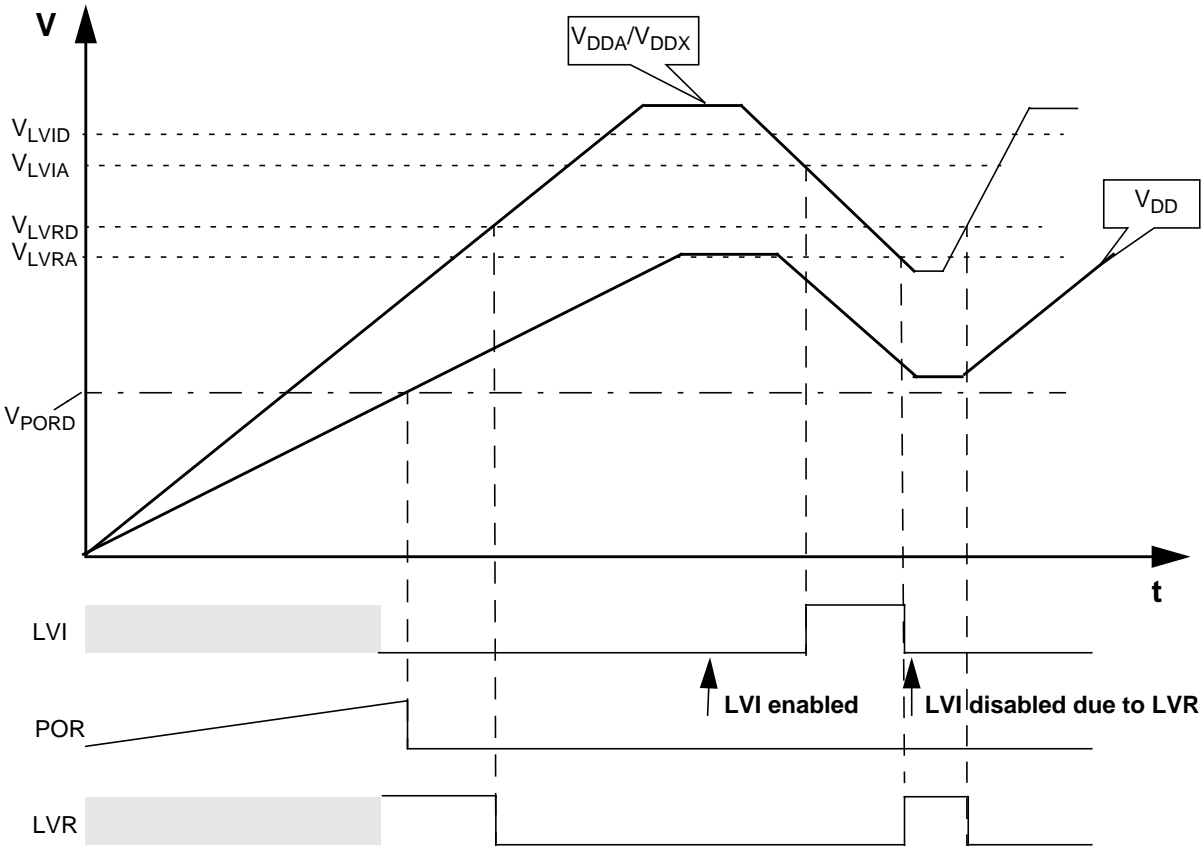
**Table A-15. ATD Electrical Characteristics**

Conditions are shown in <a href="#">Table A-4</a> unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	C	Max input source resistance <sup>(1)</sup>	$R_S$	—	—	1	$k\Omega$
2	D	Total input capacitance Non sampling	$C_{INN}$	—	—	10	$pF$
		Total input capacitance Sampling	$C_{INS}$	—	—	16	
3	D	Input internal Resistance	$R_{INA}$	-	5	15	$k\Omega$
4	C	Disruptive analog input current	$I_{NA}$	-2.5	—	2.5	mA
5	C	Coupling ratio positive current injection	$K_p$	—	—	1E-4	A/A
6	C	Coupling ratio negative current injection	$K_n$	—	—	5E-3	A/A

1. 1 Refer to [A.2.2.2](#) for further information concerning source resistance

### A.2.3 ATD Accuracy

Table A-16. and Table A-17. specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

**Figure A-4. MC9S12P-Family - Chip Power-up and Voltage Drops (not scaled)**

## 0x0040-0x006F Timer Module (TIM) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x004C	TIE	R W	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
0x004D	TSCR2	R W	TOI	0	0	0	TCRE	PR2	PR1	PR0
0x004E	TFLG1	R W	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
0x004F	TFLG2	R W	TOF	0	0	0	0	0	0	0
0x0050	TC0H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x0051	TC0L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0052	TC1H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x0053	TC1L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0054	TC2H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x0055	TC2L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0056	TC3H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x0057	TC3L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0058	TC4H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x0059	TC4L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x005A	TC5H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x005B	TC5L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x005C	TC6H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x005D	TC6L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x005E	TC7H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x005F	TC7L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0060	PACTL	R W	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
0x0061	PAFLG	R W	0	0	0	0	0	0	PAOVF	PAIF
0x0062	PACNTH	R W	PACNT15	PACNT14	PACNT13	PACNT12	PACNT11	PACNT10	PACNT9	PACNT8

## 0x0070-0x009F Analog to Digital Converter 12-Bit 10-Channel (ATD) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x007E	ATDCMPHPTH	R	0	0	0	0	0	0	CMPHT[9:8]		
		W									
0x007F	ATDCMPHTL	R	CMPHT[7:0]								
		W									
0x0080	ATDDR0H	R	Bit15	14	13	12	11	10	9	Bit8	
		W									
0x0081	ATDDR0L	R	Bit7	Bit6	0	0	0	0	0	0	
		W									
0x0082	ATDDR1H	R	Bit15	14	13	12	11	10	9	Bit8	
		W									
0x0083	ATDDR1L	R	Bit7	Bit6	0	0	0	0	0	0	
		W									
0x0084	ATDDR2H	R	Bit15	14	13	12	11	10	9	Bit8	
		W									
0x0085	ATDDR2L	R	Bit7	Bit6	0	0	0	0	0	0	
		W									
0x0086	ATDDR3H	R	Bit15	14	13	12	11	10	9	Bit8	
		W									
0x0087	ATDDR3L	R	Bit7	Bit6	0	0	0	0	0	0	
		W									
0x0088	ATDDR4H	R	Bit15	14	13	12	11	10	9	Bit8	
		W									
0x0089	ATDDR4L	R	Bit7	Bit6	0	0	0	0	0	0	
		W									
0x008A	ATDDR5H	R	Bit15	14	13	12	11	10	9	Bit8	
		W									
0x008B	ATDDR5L	R	Bit7	Bit6	0	0	0	0	0	0	
		W									
0x008C	ATDDR6H	R	Bit15	14	13	12	11	10	9	Bit8	
		W									
0x008D	ATDDR6L	R	Bit7	Bit6	0	0	0	0	0	0	
		W									
0x008E	ATDDR7H	R	Bit15	14	13	12	11	10	9	Bit8	
		W									
0x008F	ATDDR7L	R	Bit7	Bit6	0	0	0	0	0	0	
		W									
0x0090	ATDDR8H	R	Bit15	14	13	12	11	10	9	Bit8	
		W									
0x0091	ATDDR8L	R	Bit7	Bit6	0	0	0	0	0	0	
		W									
0x0092	ATDDR9H	R	Bit15	14	13	12	11	10	9	Bit8	
		W									
0x0093	ATDDR9L	R	Bit7	Bit6	0	0	0	0	0	0	
		W									
0x0094	ATDDR10H	R	Bit15	14	13	12	11	10	9	Bit8	
		W									

## 0x00C8-0x00CF Serial Communication Interface (SCI) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00C8	SCIBDH <sup>(1)</sup>	R W	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
0x00C9	SCIBDL <sup>1</sup>	R W	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
0x00CA	SCICR1 <sup>1</sup>	R W	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
0x00C8	SCIASR1 <sup>(2)</sup>	R W	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
0x00C9	SCIACR1 <sup>2</sup>	R W	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
0x00CA	SCIACR2 <sup>2</sup>	R W	0	0	0	0	0	BERRM1	BERRM0	BKDFE
0x00CB	SCICR2	R W	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
0x00CC	SCISR1	R W	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
0x00CD	SCISR2	R W	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
0x00CE	SCIDRH	R W	R8	T8	0	0	0	0	0	0
0x00CF	SCIDRL	R W	R7	R6	R5	R4	R3	R2	R1	R0
			T7	T6	T5	T4	T3	T2	T1	T0

1. Those registers are accessible if the AMAP bit in the SCI0SR2 register is set to zero

2. Those registers are accessible if the AMAP bit in the SCI0SR2 register is set to one

## 0x00D0-0x00D7 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00D0-0x00D7	Reserved	R W	0	0	0	0	0	0	0	0

## 0x00D8-0x00DF Serial Peripheral Interface (SPI) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00D8	SPICR1	R W	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
0x00D9	SPICR2	R W	0	XFRW	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
0x00DA	SPIBR	R W	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
0x00DB	SPISR	R W	SPIF	0	SPTEF	MODF	0	0	0	0