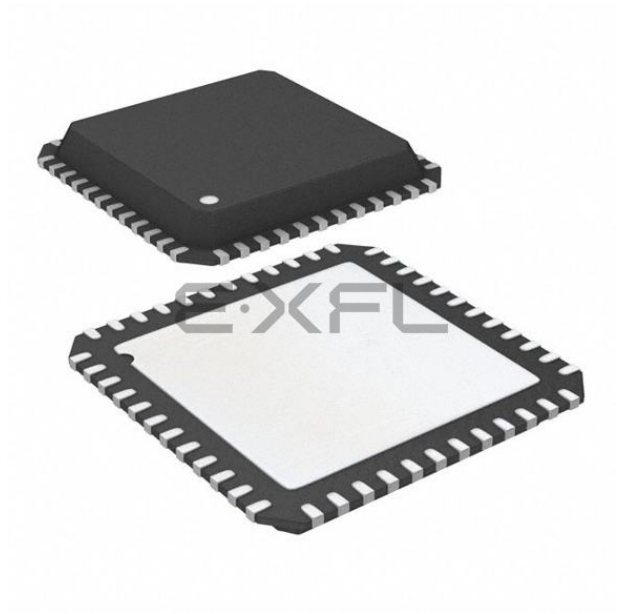

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Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TFQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12p32j0vft

Chapter 3
Memory Map Control (S12PMMCV1)

Chapter 6
S12S Debug Module (S12SDBGV2)

1.2.1 MC9S12P Family Comparison

Table 1 provides a summary of different members of the MC9S12P family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this microcontroller family.

Table 1. MC9S12P Family

Feature	MC9S12P32	MC9S12P64	MC9S12P96	MC9S12P128
CPU	CPU12-V1			
Flash memory (ECC)	32 Kbytes	64 Kbytes	96 Kbytes	128 Kbytes
Data flash (ECC)	4 Kbytes			
RAM	2 Kbytes	4 Kbytes	6 Kbytes	
MSCAN	1			
SCI	1			
SPI	1			
Timer	8 ch x 16-bit			
PWM	6 ch x 8-bit			
ADC	10 ch x 12-bit			
Frequency modulated PLL	Yes			
External oscillator (4 – 16 MHz Pierce with loop control)	Yes			
Internal 1 MHz RC oscillator	Yes			
Supply voltage	3.15 V – 5.5 V			
Execution speed	Static(1) – 32 MHz			
Package	80 QFP, 64 LQFP, 48 QFN			

1. P or D Flash erasing or programming requires a minimum bus frequency of 1MHz

1.2.2 Chip-Level Features

On-chip modules available within the family include the following features:

- S12 CPU core
- Up to 128 Kbyte on-chip flash with ECC
- 4 Kbyte data flash with ECC
- Up to 6 Kbyte on-chip SRAM
- Phase locked loop (IPLL) frequency multiplier with internal filter
- 4–16 MHz amplitude controlled Pierce oscillator
- 1 MHz internal RC oscillator
- Timer module (TIM) supporting input/output channels that provide a range of 16-bit input capture, output compare, counter, and pulse accumulator functions

Table 1-8. Pin-Out Summary[1]

Package Pin			Function			Power Supply	Internal Pull Resistor		Description
QFP 80	LQFP 64	QFN 48	Pin	2nd Func.	3rd Func.		CTRL	Reset State	
1	1	1	PP3	KWP3	PWM3	VDDX	PERP/PPSP	Disabled	Port P I/O, interrupt, PWM channel
2	2	2	PP2	KWP2	PWM2	VDDX	PERP/PPSP	Disabled	Port P I/O, interrupt, PWM channel
3	3	3	PP1	KWP1	PWM1	VDDX	PERP/PPSP	Disabled	Port P I/O, interrupt, PWM channel
4	4	-	PP0	KWP0	PWM0	VDDX	PERP/PPSP	Disabled	Port P I/O, interrupt, PWM/ channel
5	5	4	PT0	IOC0	PWM0	VDDX	PERT/PPST	Disabled	Port T I/O, TIM channel
6	6	5	PT1	IOC1	—	VDDX	PERT/PPST	Disabled	Port T I/O, TIM channel
7	7	6	PT2	IOC2	—	VDDX	PERT/PPST	Disabled	Port T I/O, TIM channel
8	8	7	PT3	IOC3	—	VDDX	PERT/PPST	Disabled	Port T I/O, TIM channel
9	9	-	PJ0	KWJ0	—	VDDX	PERJ/PPSJ	Up	Port J I/O, interrupt
10	10	-	PJ1	KWJ1	—	VDDX	PERJ/PPSJ	Up	Port J I/O, interrupt
11	11	8	PT4	IOC4	PWM4	VDDX	PERT/PPST	Disabled	Port T I/O, PWM/TIM channel
12	12	9	PT5	IOC5	PWM5 or API_EXTCLK	VDDX	PERT/PPST	Disabled	Port T I/O, PWM/TIM channel, API output
13	13	10	PT6	IOC6		VDDX	PERT/PPST	Disabled	Port T I/O, channel of TIM
14	14	11	PT7	IOC7		VDDX	PERT/PPST	Disabled	Port T I/O, channel of TIM
15	15	12	BKGD	MODC	—	VDDX	Always on	Up	Background debug

Table 1-8. Pin-Out Summary[1]

Package Pin			Function			Power Supply	Internal Pull Resistor		Description
QFP 80	LQFP 64	QFN 48	Pin	2nd Func.	3rd Func.		CTRL	Reset State	
53	41	30	PAD02	AN02	—	VDDA	PER1AD	Disabled	Port AD I/O, analog input of ATD
54	42	31	PAD03	AN03	—	VDDA	PER1AD	Disabled	Port AD I/O, analog input of ATD
55	43	32	PAD04	AN04	—	VDDA	PER1AD	Disabled	Port AD I/O, analog input of ATD
56	44	33	PAD05	AN05	—	VDDA	PER1AD	Disabled	Port AD I/O, analog input of ATD
57	45	34	PAD06	AN06	—	VDDA	PER1AD	Disabled	Port AD I/O, analog input of ATD
58	46	35	PAD07	AN07	—	VDDA	PER1AD	Disabled	Port AD I/O, analog input of ATD
59	47	36	VDDA	—	—	—	—	—	—
60	48	36	VRH[2]	—	—	—	—	—	—
61	49	37	VRL[3]	—	—	—	—	—	—
62	49	37	VSSA	—	—	—	—	—	—
63	50	38	PS0	RXD	—	VDDX	PERS/PPSS	Up	Port S I/O, RXD of SCI
64	51	39	PS1	TXD	—	VDDX	PERS/PPSS	Up	Port S I/O, TXD of SCI
65	52	-	PS2		—	VDDX	PERS/PPSS	Up	Port S I/O
66	53	-	PS3		—	VDDX	PERS/PPSS	Up	Port S I/O
67	54	40	TEST	—	—	N.A.	$\overline{\text{RESET}}$ pin	DOWN	Test input
68	-	-	PJ7	KWJ7	—	VDDX	PERJ/PPSJ	Up	Port J I/O, interrupt
69	-	-	PJ6	KWJ6	—	VDDX	PERJ/PPSJ	Up	Port J I/O, interrupt
70	55	41	PM5	SCK	—	VDDX	PERM/PPSM	Disabled	Port M I/O, MISO of SPI

Table 1-12. Interrupt Vector Locations (Sheet 2 of 3)

Vector Address[1]	Interrupt Source	CCR Mask	Local Enable	Wake up from STOP	Wakeup from WAIT
Vector base+ $F0	RTI timeout interrupt	I bit	CPMUINT (RTIE)	7.6 Interrupts	
Vector base+ $EE	TIM timer channel 0	I bit	TIE (C0I)	No	Yes
Vector base + $EC	TIM timer channel 1	I bit	TIE (C1I)	No	Yes
Vector base+ $EA	TIM timer channel 2	I bit	TIE (C2I)	No	Yes
Vector base+ $E8	TIM timer channel 3	I bit	TIE (C3I)	No	Yes
Vector base+ $E6	TIM timer channel 4	I bit	TIE (C4I)	No	Yes
Vector base+ $E4	TIM timer channel 5	I bit	TIE (C5I)	No	Yes
Vector base + $E2	TIM timer channel 6	I bit	TIE (C6I)	No	Yes
Vector base+ $E0	TIM timer channel 7	I bit	TIE (C7I)	No	Yes
Vector base+ $DE	TIM timer overflow	I bit	TSRC2 (TOF)	No	Yes
Vector base+ $DC	TIM Pulse accumulator A overflow	I bit	PACTL (PAOVI)	No	Yes
Vector base + $DA	TIM Pulse accumulator input edge	I bit	PACTL (PAI)	No	Yes
Vector base + $D8	SPI	I bit	SPICR1 (SPIE, SPTIE)	No	Yes
Vector base+ $D6	SCI	I bit	SCICR2 (TIE, TCIE, RIE, ILIE)	Yes	Yes
Vector base + $D4	Reserved				
Vector base + $D2	ATD	I bit	ATDCTL2 (ASCIE)	Yes	Yes
Vector base + $D0	Reserved				
Vector base + $CE	Port J	I bit	PIEJ (PIEJ7-PIEJ6, PIEJ2-PIEJ0)	Yes	Yes
Vector base + $CC to Vector base + $CA	Reserved				
Vector base + $C8	Oscillator status interrupt	I bit	CPMUINT (OSCIE)	No	No
Vector base + $C6	PLL lock interrupt	I bit	CPMUINT (LOCKIE)	No	No
Vector base + $C4 to Vector base + $BC	Reserved				
Vector base + $BA	FLASH error	I bit	FERCNFG (SFDIE, DFDIE)	No	No
Vector base + $B8	FLASH command	I bit	FCNFG (CCIE)	No	Yes
Vector base + $B6	CAN wake-up	I bit	CANRIER (WUPIE)	8.4.7 Interrupts	
Vector base + $B4	CAN errors	I bit	CANRIER (CSCIE, OVRIE)		
Vector base + $B2	CAN receive	I bit	CANRIER (RXFIE)		
Vector base + $B0	CAN transmit	I bit	CANTIER (TXEIE[2:0])		

1.12 COP Configuration

The COP time-out rate bits CR[2:0] and the WCOP bit in the CPMUCOP register at address 0x003C are loaded from the Flash register FOPT. See Table 1-13 and Table 1-14 for coding. The FOPT register is loaded from the Flash configuration field byte at global address 0x3_FF0E during the reset sequence.

Table 1-13. Initial COP Rate Configuration

NV[2:0] in FOPT Register	CR[2:0] in COPCTL Register
000	111
001	110
010	101
011	100
100	011
101	010
110	001
111	000

Table 1-14. Initial WCOP Configuration

NV[3] in FOPT Register	WCOP in COPCTL Register
1	0
0	1

1.13 ATD External Trigger Input Connection

The ATD module includes external trigger inputs ETRIG0 and ETRIG1. The external trigger allows the user to synchronize ATD conversion to external trigger events. Table 1-15 shows the connection of the external trigger inputs.

Table 1-15. ATD External Trigger Sources

External Trigger Input	Connectivity
ETRIG0	PWM channel 1
ETRIG1	PWM channel 3

Consult the ATD section for information about the analog-to-digital converter module. References to freeze mode are equivalent to active BDM mode.

2.3.48 PIM Reserved Registers

Address 0x0260-0x267 Access: User read(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved u = Unaffected by reset

Figure 2-46. PIM Reserved Registers

1. Read: Always reads 0x00
   Write: Unimplemented

2.3.49 Port J Data Register (PTJ)

Address 0x0268 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	PTJ7	PTJ6	0	0	0	PTJ2	PTJ1	PTJ0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-47. Port J Data Register (PTJ)

1. Read: Anytime. The data source is depending on the data direction value.
   Write: Anytime

Table 2-43. PTJ Register Field Descriptions

Field	Description
7-6, 2-0 PTJ	**Port J general purpose input/output data**—Data Register, pin interrupt input/output The associated pin can be used as general purpose I/O. In general purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the buffered pin input state is read. • Pin interrupts can be generated if enabled in input or output mode.

each trace buffer entry. In Detail mode CINF comprises of R/W and size access information (CRW and CSZ respectively).

Single byte data accesses in Detail Mode are always stored to the low byte of the trace buffer (DATAL) and the high byte is cleared. When tracing word accesses, the byte at the lower address is always stored to trace buffer byte1 and the byte at the higher address is stored to byte0.

Table 6-37. Trace Buffer Organization (Normal,Loop1,Detail modes)

Mode	Entry Number	4-bits	8-bits	8-bits
		Field 2	Field 1	Field 0
Detail Mode	Entry 1	CINF1,ADRH1	ADRM1	ADRL1
		0	DATAH1	DATAL1
	Entry 2	CINF2,ADRH2	ADRM2	ADRL2
		0	DATAH2	DATAL2
Normal/Loop1 Modes	Entry 1	PCH1	PCM1	PCL1
	Entry 2	PCH2	PCM2	PCL2

6.4.5.3.1 Information Bit Organization

The format of the bits is dependent upon the active trace mode as described below.

Field2 Bits in Detail Mode

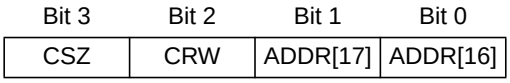

Figure 6-25. Field2 Bits in Detail Mode

In Detail Mode the CSZ and CRW bits indicate the type of access being made by the CPU.

Table 6-38. Field Descriptions

Bit	Description
3 CSZ	**Access Type Indicator**— This bit indicates if the access was a byte or word size when tracing in Detail Mode 0 Word Access 1 Byte Access
2 CRW	**Read Write Indicator** — This bit indicates if the corresponding stored address corresponds to a read or write access when tracing in Detail Mode. 0 Write Access 1 Read Access
1 ADDR[17]	**Address Bus bit 17**— Corresponds to system address bus bit 17.
0 ADDR[16]	**Address Bus bit 16**— Corresponds to system address bus bit 16.

7.3.2.5 S12CPMU Interrupt Enable Register (CPMUINT)

This register enables S12CPMU interrupt requests.

0x0038

	7	6	5	4	3	2	1	0
R	RTIE	0	0	LOCKIE	0	0	OSCIE	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 7-8. S12CPMU Interrupt Enable Register (CPMUINT)

Read: Anytime

Write: Anytime

Table 7-4. CRGINT Field Descriptions

Field	Description
7 RTIE	**Real Time Interrupt Enable Bit** 0 Interrupt requests from RTI are disabled. 1 Interrupt will be requested whenever RTIF is set.
4 LOCKIE	**PLL Lock Interrupt Enable Bit** 0 PLL LOCK interrupt requests are disabled. 1 Interrupt will be requested whenever LOCKIF is set.
1 OSCIE	**Oscillator Corrupt Interrupt Enable Bit** 0 Oscillator Corrupt interrupt requests are disabled. 1 Interrupt will be requested whenever OSCIF is set.

Table 7-19. Selectable Autonomous Periodical Interrupt Periods

APICLK	APIR[15:0]	Selected Period
0	0000	0.2 ms[1]
0	0001	0.4 ms[1]
0	0002	0.6 ms[1]
0	0003	0.8 ms[1]
0	0004	1.0 ms[1]
0	0005	1.2 ms[1]
0	.....	.....
0	FFFD	13106.8 ms[1]
0	FFFE	13107.0 ms[1]
0	FFFF	13107.2 ms[1]
1	0000	2 * Bus Clock period
1	0001	4 * Bus Clock period
1	0002	6 * Bus Clock period
1	0003	8 * Bus Clock period
1	0004	10 * Bus Clock period
1	0005	12 * Bus Clock period
1	.....	.....
1	FFFD	131068 * Bus Clock period
1	FFFE	131070 * Bus Clock period
1	FFFF	131072 * Bus Clock period

1 When f_{ACLK} is trimmed to 10KHz.

Table 9-6. ATDCTL2 Field Descriptions (continued)

Field	Description
1 ASCIE	**ATD Sequence Complete Interrupt Enable** 0 ATD Sequence Complete interrupt requests are disabled. 1 ATD Sequence Complete interrupt will be requested whenever SCF=1 is set.
0 ACMPIE	**ATD Compare Interrupt Enable** — If automatic compare is enabled for conversion *n* (CMPE[*n*]=1 in ATDCMPE register) this bit enables the compare interrupt. If the CCF[*n*] flag is set (showing a successful compare for conversion *n*), the compare interrupt is triggered. 0 ATD Compare interrupt requests are disabled. 1 For the conversions in a sequence for which automatic compare is enabled (CMPE[*n*]=1), ATD Compare Interrupt will be requested whenever any of the respective CCF flags is set.

Table 9-7. External Trigger Configurations

ETRIGLE	ETRIGP	External Trigger Sensitivity
0	0	Falling edge
0	1	Rising edge
1	0	Low level
1	1	High level

9.3.2.4 ATD Control Register 3 (ATDCTL3)

Writes to this register will abort current conversion sequence.

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R W	DJM	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
Reset	0	0	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-6. ATD Control Register 3 (ATDCTL3)

Read: Anytime

Write: Anytime

Read: anytime

Write: anytime (causes the scale counter to load the PWMSCLA value)

10.3.2.10 PWM Scale B Register (PWMSCLB)

PWMSCLB is the programmable scale value used in scaling clock B to generate clock SB. Clock SB is generated by taking clock B, dividing it by the value in the PWMSCLB register and dividing that by two.

Clock SB = Clock B / (2 * PWMSCLB)

NOTE

When PWMSCLB = 0x0000, PWMSCLB value is considered a full scale value of 256. Clock B is thus divided by 512.

Any value written to this register will cause the scale counter to load the new scale value (PWMSCLB).

Module Base + 0x0009

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 10-12. PWM Scale B Register (PWMSCLB)

Read: anytime

Write: anytime (causes the scale counter to load the PWMSCLB value).

10.3.2.11 Reserved Registers (PWMSCNTx)

The registers PWMSCNTA and PWMSCNTB are reserved for factory testing of the PWM module and are not available in normal modes.

Module Base + 0x000A

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-13. Reserved Register (PWMSCNTA)

11.4.5.5 LIN Transmit Collision Detection

This module allows to check for collisions on the LIN bus.

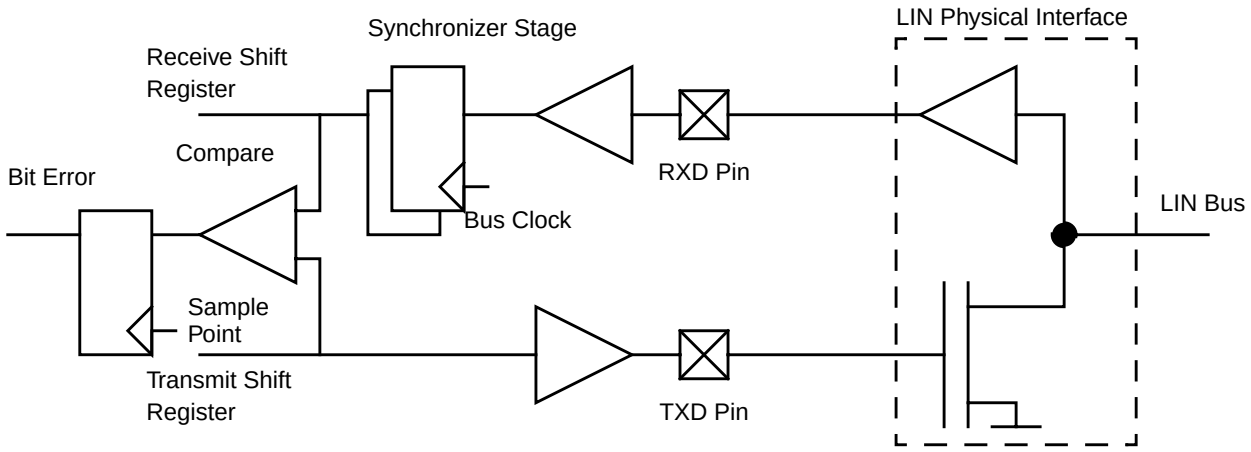

Figure 11-18. Collision Detect Principle

If the bit error circuit is enabled (BERRM[1:0] = 0:1 or = 1:0]), the error detect circuit will compare the transmitted and the received data stream at a point in time and flag any mismatch. The timing checks run when transmitter is active (not idle). As soon as a mismatch between the transmitted data and the received data is detected the following happens:

- The next bit transmitted will have a high level (TXPOL = 0) or low level (TXPOL = 1)
- The transmission is aborted and the byte in transmit buffer is discarded.
- the transmit data register empty and the transmission complete flag will be set
- The bit error interrupt flag, BERRIF, will be set.
- No further transmissions will take place until the BERRIF is cleared.

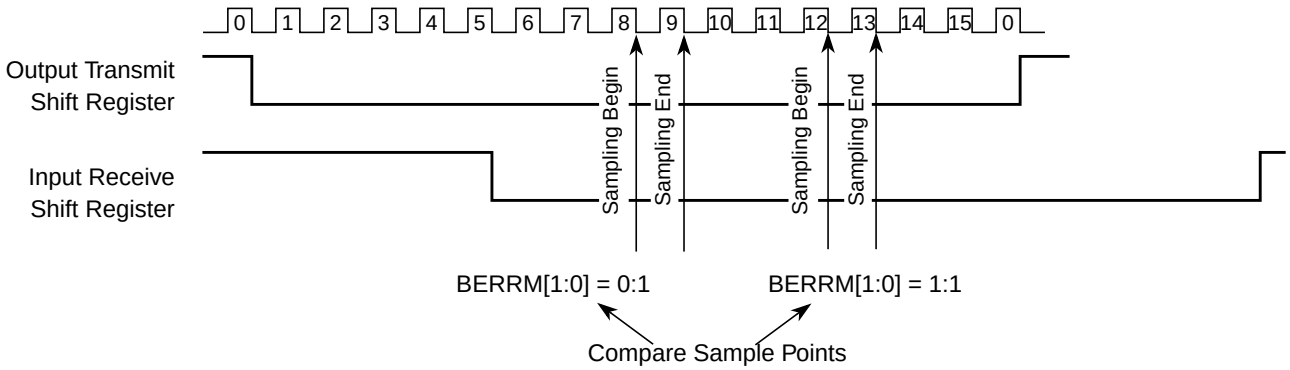

Figure 11-19. Timing Diagram Bit Error Detection

If the bit error detect feature is disabled, the bit error interrupt flag is cleared.

NOTE

The RXPOL and TXPOL bit should be set the same when transmission collision detect feature is enabled, otherwise the bit error interrupt flag may be set incorrectly.

Table 14-20. PAFLG Field Descriptions

Field	Description
1 PAOVF	**Pulse Accumulator Overflow Flag** — Set when the 16-bit pulse accumulator overflows from 0xFFFF to 0x0000. Clearing this bit requires writing a one to this bit in the PAFLG register while TEN bit of TSCR1 or PAEN bit of PACTL register is set to one.
0 PAIF	**Pulse Accumulator Input edge Flag** — Set when the selected edge is detected at the IOC7 input pin.In event mode the event edge triggers PAIF and in gated time accumulation mode the trailing edge of the gate signal at the IOC7 input pin triggers PAIF. Clearing this bit requires writing a one to this bit in the PAFLG register while TEN bit of TSCR1 or PAEN bit of PACTL register is set to one. Any access to the PACNT register will clear all the flags in this register when TFFCA bit in register TSCR(0x0006) is set.

14.3.2.17 Pulse Accumulators Count Registers (PACNT)

Module Base + 0x0022

	15	14	13	12	11	10	9	0
R W	PACNT15	PACNT14	PACNT13	PACNT12	PACNT11	PACNT10	PACNT9	PACNT8
Reset	0	0	0	0	0	0	0	0

Figure 14-26. Pulse Accumulator Count Register High (PACNTH)

Module Base + 0x0023

	7	6	5	4	3	2	1	0
R W	PACNT7	PACNT6	PACNT5	PACNT4	PACNT3	PACNT2	PACNT1	PACNT0
Reset	0	0	0	0	0	0	0	0

Figure 14-27. Pulse Accumulator Count Register Low (PACNTL)

Read: Anytime

Write: Anytime

These registers contain the number of active input edges on its input pin since the last reset.

When PACNT overflows from 0xFFFF to 0x0000, the Interrupt flag PAOVF in PAFLG (0x0021) is set.

Full count register access should take place in one clock cycle. A separate read/write for high byte and low byte will give a different result than accessing them as a word.

NOTE

Reading the pulse accumulator counter registers immediately after an active edge on the pulse accumulator input pin may miss the last count because the input has to be synchronized with the bus clock first.

4. Junction to case thermal resistance was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the “case” temperature. This basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.
5. Thermal characterization parameter Ψ_{JT} is the “resistance” from junction to reference point thermocouple on top center of the case as defined in JESD51-2. Ψ_{JT} is a useful value to use to estimate junction temperature in a steady state customer enviroment.
6. Junction to case thermal resistance was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the “case” temperature. This basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.
7. Thermal characterization parameter Ψ_{JT} is the “resistance” from junction to reference point thermocouple on top center of the case as defined in JESD51-2. Ψ_{JT} is a useful value to use to estimate junction temperature in a steady state customer enviroment.

Table A-13. Pseudo Stop Current Characteristics

Conditions are: VDDR=5.5V, RTI and COP and API enabled, see Table A-8.							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	C	150°C	I_{DDPS}		450		µA
2	C	-40°C	I_{DDPS}		175		µA
3	C	25°C	I_{DDPS}		200		µA

A.2 ATD Characteristics

This section describes the characteristics of the analog-to-digital converter.

A.2.1 ATD Operating Characteristics

The Table A-14 and Table A-15 show conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:

$$V_{SSA} \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DDA}.$$

This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-14. ATD Operating Characteristics

Conditions are shown in Table A-4 unless otherwise noted, supply voltage 3.13 V < V_{DDA} < 5.5 V							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA}/2$	 — —	 $V_{DDA}/2$ V_{DDA}	 V V
2	D	Voltage difference V_{DDX} to V_{DDA}	Δ_{VDDX}	–2.35	0	0.1	V
3	D	Voltage difference V_{SSX} to V_{SSA}	Δ_{VSSX}	–0.1	0	0.1	V
4	C	Differential reference voltage[1]	V_{RH}-V_{RL}	3.13	5.0	5.5	V
5	C	ATD Clock Frequency (derived from bus clock via the prescaler bus)	f_{ATDCLk}	0.25		8.0	MHz
6	P	ATD Clock Frequency in Stop mode (internal generated temperature and voltage dependent clock, ICLK)		0.6	1	1.7	MHz
7	D	ADC conversion in stop, recovery time[2]	$t_{ATDSTPRCV}$	—	—	1.5	us
8	D	ATD Conversion Period[3] 12 bit resolution: 10 bit resolution: 8 bit resolution:	 N_{CONV12} N_{CONV10} N_{CONV8}	 20 19 17		 42 41 39	 ATD clock Cycles

1. Full accuracy is not guaranteed when differential voltage is less than 4.50 V
2. When converting in Stop Mode (ICLKSTP=1) an ATD Stop Recovery time tATDSTPRCV is required to switch back to bus clock based ATDCLK when leaving Stop Mode. Do not access ATD registers during this time.
3. The minimum time assumes a sample time of 4 ATD clock cycles. The maximum time assumes a sample time of 24 ATD clock cycles and the discharge feature (SMP_DIS) enabled, which adds 2 ATD clock cycles.

The D-Flash sector erase time is ~5ms on a new device and can extend to ~20ms as the flash is cycled.

Table A-18. NVM Timing Characteristics (FTMRC)

Num	C	Rating	Symbol	Min	Typ(1)	Max(2)	Unit(3)
1		Bus frequency	f_{NVMBUS}	1	—	32	MHz
2		Operating frequency	f_{NVMOP}	0.8	1.0	1.05	MHz
3	D	Erase all blocks (mass erase) time	t_{mass}	—	100	130	ms
4	D	Erase verify all blocks (blank check) time	t_{check}	—	—	35500	t_{cyc}
5	D	Unsecure Flash time	t_{uns}	—	100	130	ms
6	D	P-Flash block erase time	t_{pmass}	—	100	130	ms
7	D	P-Flash erase verify (blank check) time	t_{pcheck}	—	—	33500	t_{cyc}
8	D	P-Flash sector erase time	t_{pera}	—	20	26	ms
9	D	P-Flash phrase programming time	t_{ppgm}	—	226	285	µs
10	D	D-Flash sector erase time	t_{dera}	—	5(4)	26	ms
11	D	D-Flash erase verify (blank check) time	t_{dcheck}	—	—	2800	t_{cyc}
12a	D	D-Flash one word programming time	t_{dpgm1}	—	100	107	µs
12b	D	D-Flash two word programming time	t_{dpgm2}	—	170	185	µs
12c	D	D-Flash three word programming time	t_{dpgm3}	—	241	262	µs
12d	D	D-Flash four word programming time	t_{dpgm4}	—	311	339	µs
12e	D	D-Flash four word programming time crossing row boundary	t_{dpgm4c}	—	328	357	µs

1. Typical program and erase times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
2. Maximum program and erase times are based on minimum f_{NVMOP} and maximum f_{NVMBUS}
3. $t_{cyc} = 1 / f_{NVMBUS}$
4. Typical value for a new device

A.3.2 NVM Reliability Parameters

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

The data retention and program/erase cycling failure rates are specified at the operating conditions noted. The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xXX1E	CANxTTSRH	R	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		W								
0xXX1F	CANxTTSRL	R	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		W								

0x0180-023F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0180-0x023F	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0240 -0x027F Port Integration Module (PIM) Map 4 of 4

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0240	PTT	R	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
		W								
0x0241	PTIT	R	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
		W								
0x0242	DDRT	R	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
		W								
0x0243	RDRT	R	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
		W								
0x0244	PERT	R	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
		W								
0x0245	PPST	R	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
		W								
0x0246	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0247	PTTRR	R	PTTRR7	PTTRR6	PTTRR5	PTTRR4	0	PTTRR2	PTTRR1	PTTRR0
		W								