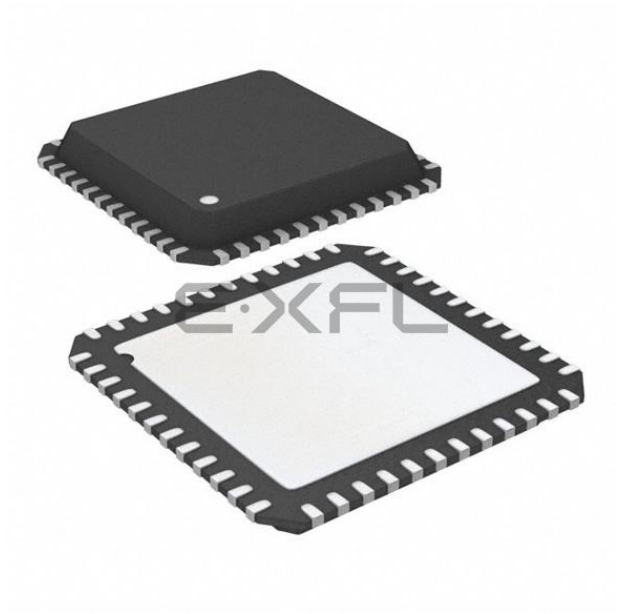

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Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
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Chapter 4
Interrupt Module (S12SINTV1)

Chapter 5
Background Debug Module (S12SBDMV1)

1.7.3.20 PM1 / TXCAN — Port M I/O Pin 1

PM1 is a general-purpose input or output pin. It can be configured as the transmit pin TXCAN of the scalable controller area network controller (CAN).

1.7.3.21 PM0 / RXCAN — Port M I/O Pin 0

PM0 is a general-purpose input or output pin. It can be configured as the receive pin RXCAN of the scalable controller area network controller (CAN).

1.7.3.22 PP[5:0] / KWP[5:0] / PWM[5:0] — Port P I/O Pins 5-0

PP[5:0] are a general-purpose input or output pins. They can be configured as keypad wakeup inputs. They can be configured as pulse width modulator (PWM) channel 5-0 output

1.7.3.23 PP7 / KWP7 — Port P I/O Pin 7

PP7 is a general-purpose input or output pin. It can be configured as a keypad wakeup input.

1.7.3.24 PS3 — Port S I/O Pin 3

PS3 is a general-purpose input or output pin.

1.7.3.25 PS2 — Port S I/O Pin 2

PS2 is a general-purpose input or output pin.

1.7.3.26 PS1 / TXD — Port S I/O Pin 1

PS1 is a general-purpose input or output pin. It can be configured as the transmit pin TXD of serial communication interface (SCI).

1.7.3.27 PS0 / RXD — Port S I/O Pin 0

PS0 is a general-purpose input or output pin. It can be configured as the receive pin RXD of serial communication interface (SCI).

1.7.3.28 PT[7:6] / IOC[7:6] — Port T I/O Pins 7-6

PT[7:6] are general-purpose input or output pins. They can be configured as timer (TIM) channel 7-6.

1.7.3.29 PT5 / IOC5 / PWM5 / API_EXTCLK — Port T I/O Pin 5

PT5 is a general-purpose input or output pin. It can be configured as timer (TIM) channel 5, pulse width modulator (PWM) output 5 or as the output of the API_EXTCLK.

Table 2-2. Block Memory Map (continued)

Port	Offset or Address	Register	Access	Reset Value	Section/Page
S	0x0248	PTS—Port S Data Register	R/W	0x00	2.3.24/2-77
	0x0249	PTIS—Port S Input Register	R	[4]	2.3.25/2-77
	0x024A	DDRS—Port S Data Direction Register	R/W	0x00	2.3.26/2-78
	0x024B	RDRS—Port S Reduced Drive Register	R/W	0x00	2.3.27/2-79
	0x024C	PERS—Port S Pull Device Enable Register	R/W	0xFF	2.3.28/2-79
	0x024D	PTPS—Port S Polarity Select Register	R/W	0x00	2.3.29/2-80
	0x024E	WOMS—Port S Wired-Or Mode Register	R/W	0x00	2.3.30/2-80
	0x024F	PIM Reserved	R	0x00	2.3.39/2-86
M	0x0250	PTM—Port M Data Register	R/W	0x00	2.3.32/2-81
	0x0251	PTIM—Port M Input Register	R	[4]	2.3.33/2-82
	0x0252	DDRM—Port M Data Direction Register	R/W	0x00	2.3.34/2-83
	0x0253	RDRM—Port M Reduced Drive Register	R/W	0x00	2.3.35/2-84
	0x0254	PERM—Port M Pull Device Enable Register	R/W	0x00	2.3.36/2-85
	0x0255	PPSM—Port M Polarity Select Register	R/W	0x00	2.3.37/2-85
	0x0256	WOMM—Port M Wired-Or Mode Register	R/W	0x00	2.3.38/2-86
	0x0257	PIM Reserved	R	0x00	2.3.39/2-86
P	0x0258	PTP—Port P Data Register	R/W	0x00	2.3.40/2-87
	0x0259	PTIP—Port P Input Register	R	[4]	2.3.41/2-88
	0x025A	DDRP—Port P Data Direction Register	R/W	0x00	2.3.42/2-88
	0x025B	RDRP—Port P Reduced Drive Register	R/W	0x00	2.3.43/2-89
	0x025C	PERP—Port P Pull Device Enable Register	R/W	0x00	2.3.44/2-90
	0x025D	PTPP—Port P Polarity Select Register	R/W	0x00	2.3.45/2-90
	0x025E	PIEP—Port P Interrupt Enable Register	R/W	0x00	2.3.46/2-91
	0x025F	PIFP—Port P Interrupt Flag Register	R/W	0x00	2.3.47/2-91
	0x0260 : 0x0267	PIM Reserved	R	0x00	2.3.48/2-92

2.3.12 ECLK Control Register (ECLKCTL)

Address 0x001C Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	NECLK	NCLKX2	DIV16	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
Reset:	Mode Depen-dent	1	0	0	0	0	0	0
Special single-chip	0	1	0	0	0	0	0	0
Normal single-chip	1	1	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-10. ECLK Control Register (ECLKCTL)

1. Read: Anytime
   Write: Anytime

Table 2-12. ECLKCTL Register Field Descriptions

Field	Description
7 NECLK	**No ECLK**—Disable ECLK output This bit controls the availability of a free-running clock on the ECLK pin. This clock has a fixed rate of equivalent to the internal bus clock. 1 ECLK disabled 0 ECLK enabled
6 NCLKX2	**No ECLKX2**—Disable ECLKX2 output This bit controls the availability of a free-running clock on the ECLKX2 pin. This clock has a fixed rate of twice the internal bus clock. 1 ECLKX2 disabled 0 ECLKX2 enabled
5 DIV16	**Free-running ECLK pre-divider**—Divide by 16 This bit enables a divide-by-16 stage on the selected EDIV rate. 1 Divider enabled: ECLK rate = EDIV rate divided by 16 0 Divider disabled: ECLK rate = EDIV rate
4-0 EDIV	**Free-running ECLK Divider**—Configure ECLK rate These bits determine the rate of the free-running clock on the ECLK pin. 00000 ECLK rate = bus clock rate 00001 ECLK rate = bus clock rate divided by 2 00010 ECLK rate = bus clock rate divided by 3,... 11111 ECLK rate = bus clock rate divided by 32

2.3.13 PIM Reserved Register

Table 2-29. PTIM Register Field Descriptions

Field	Description
5-0 PTIM	**Port M input data**— A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.3.34 Port M Data Direction Register (DDRM)

Address 0x0252 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-32. Port M Data Direction Register (DDRM)

1. Read: Anytime
   Write: Anytime

Table 2-30. DDRM Register Field Descriptions

Field	Description
5 DDRM	**Port M data direction**— This bit determines whether the associated pin is an input or output. Depending on the configuration of the enabled SPI the I/O state will be forced to be input or output. In this case the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input
4 DDRM	**Port M data direction**— This bit determines whether the associated pin is an input or output. Depending on the configuration of the enabled SPI the I/O state will be forced to be input or output. In this case the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input
3 DDRM	**Port M data direction**— This bit determines whether the associated pin is an input or output. Depending on the configuration of the enabled SPI the I/O state will be forced to be input or output. In this case the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input

2.3.40 Port P Data Register (PTP)

Address 0x0258 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	PTP7	0	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
W								
Altern. Function	—	—	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Reset	0	0	0	0	0	0	0	0

Figure 2-38. Port P Data Register (PTP)

1. Read: Anytime. The data source is depending on the data direction value.
   Write: Anytime

Table 2-35. PTP Register Field Descriptions

Field	Description
7 PTP	**Port P general purpose input/output data**—Data Register, pin interrupt input/output The associated pin can be used as general purpose I/O. In general purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the buffered pin input state is read. • Pin interrupts can be generated if enabled in input or output mode.
5 PTP	**Port P general purpose input/output data**—Data Register, PWM input/output, pin interrupt input/output When not used with the alternative function, the associated pin can be used as general purpose I/O. In general purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the buffered pin input state is read. • The PWM function takes precedence over the general purpose I/O function if the related channel or the emergency shut-down feature is enabled. • Pin interrupts can be generated if enabled in input or output mode.
4-0 PTP	**Port P general purpose input/output data**—Data Register, PWM output, pin interrupt input/output When not used with the alternative function, the associated pin can be used as general purpose I/O. In general purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the buffered pin input state is read. • The PWM function takes precedence over the general purpose I/O function if the related channel is enabled. • Pin interrupts can be generated if enabled in input or output mode.

2.3.62 Port AD Reduced Drive Register (RDR1AD)

Address 0x0275 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	RDR1AD7	RDR1AD6	RDR1AD5	RDR1AD4	RDR1AD3	RDR1AD2	RDR1AD1	RDR1AD0
Reset	0	0	0	0	0	0	0	0

Figure 2-60. Port AD Reduced Drive Register (RDR1AD)

1. Read: Anytime
   Write: Anytime

Table 2-56. RDR1AD Register Field Descriptions

Field	Description
7-0 RDR1AD	**Port AD reduced drive**—Select reduced drive for output pin This bit configures the drive strength of the associated output pin as either full or reduced. If a pin is used as input this bit has no effect. The reduced drive function is independent of which function is being used on a particular pin. 1 Reduced drive selected (approx. 1/5 of the full drive strength) 0 Full drive strength enabled

2.3.63 Port AD Pull Up Enable Register (PER0AD)

Address 0x0276 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PER0AD1	PER0AD0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-61. Port AD Pull Up Enable Register (PER0AD)

1. Read: Anytime
   Write: Anytime

Table 2-57. PER0AD Register Field Descriptions

Field	Description
1-0 PER0AD	**Port AD pull-up enable**—Enable pull-up device on input pin This bit controls whether a pull device on the associated port input pin is active. If a pin is used as output this bit has no effect. 1 Pull device enabled 0 Pull device disabled

Table 3-6. DIRECT Field Descriptions

Field	Description
7–0 DP[15:8]	**Direct Page Index Bits 15–8** — These bits are used by the CPU when performing accesses using the direct addressing mode. These register bits form bits [15:8] of the local address (see Figure 3-6).

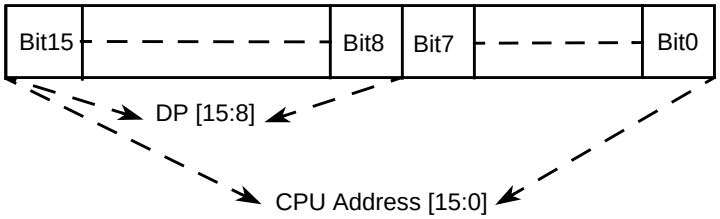

Figure 3-6. DIRECT Address Mapping

Example 3-1. This example demonstrates usage of the Direct Addressing Mode

```
MOVB      #$80,DIRECT       ;Set DIRECT register to 0x80. Write once only.
                            ;Global data accesses to the range 0xXX_80XX can be direct.
                            ;Logical data accesses to the range 0x80XX are direct.

LDY       <$00              ;Load the Y index register from 0x8000 (direct access).
                            ;< operator forces direct access on some assemblers but in
                            ;many cases assemblers are "direct page aware" and can
                            ;automatically select direct mode.
```

3.3.2.3 Program Page Index Register (PPAGE)

Address: 0x0030

	7	6	5	4	3	2	1	0
R	0	0	0	0	PIX3	PIX2	PIX1	PIX0
W								
Reset	0	0	0	0	1	1	1	0

Figure 3-7. Program Page Index Register (PPAGE)

Read: Anytime

Write: Anytime

These four index bits are used to map 16KB blocks into the Flash page window located in the local (CPU or BDM) memory map from address 0x8000 to address 0xBFFF (see Figure 3-8). This supports accessing up to 256 KB of Flash (in the Global map) within the 64KB Local map. The PPAGE index register is effectively used to construct paged Flash addresses in the Local map format. The CPU has special access to read and write this register directly during execution of CALL and RTC instructions.

If an interrupt is pending when a TRACE1 command is issued, the interrupt stacking operation occurs but no user instruction is executed. Once back in standard BDM firmware execution, the program counter points to the first instruction in the interrupt service routine.

Be aware when tracing through the user code that the execution of the user code is done step by step but all peripherals are free running. Hence possible timing relations between CPU code execution and occurrence of events of other peripherals no longer exist.

Do not trace the CPU instruction BGND used for soft breakpoints. Tracing over the BGND instruction will result in a return address pointing to BDM firmware address space.

When tracing through user code which contains stop or wait instructions the following will happen when the stop or wait instruction is traced:

The CPU enters stop or wait mode and the TRACE1 command can not be finished before leaving the low power mode. This is the case because BDM active mode can not be entered after CPU executed the stop instruction. However all BDM hardware commands except the BACKGROUND command are operational after tracing a stop or wait instruction and still being in stop or wait mode. If system stop mode is entered (all bus masters are in stop mode) no BDM command is operational.

As soon as stop or wait mode is exited the CPU enters BDM active mode and the saved PC value points to the entry of the corresponding interrupt service routine.

In case the handshake feature is enabled the corresponding ACK pulse of the TRACE1 command will be discarded when tracing a stop or wait instruction. Hence there is no ACK pulse when BDM active mode is entered as part of the TRACE1 command after CPU exited from stop or wait mode. All valid commands sent during CPU being in stop or wait mode or after CPU exited from stop or wait mode will have an ACK pulse. The handshake feature becomes disabled only when system stop mode has been reached. Hence after a system stop mode the handshake feature must be enabled again by sending the ACK_ENABLE command.

5.4.11 Serial Communication Time Out

The host initiates a host-to-target serial transmission by generating a falling edge on the BKGD pin. If BKGD is kept low for more than 128 target clock cycles, the target understands that a SYNC command was issued. In this case, the target will keep waiting for a rising edge on BKGD in order to answer the SYNC request pulse. If the rising edge is not detected, the target will keep waiting forever without any time-out limit.

Consider now the case where the host returns BKGD to logic one before 128 cycles. This is interpreted as a valid bit transmission, and not as a SYNC request. The target will keep waiting for another falling edge marking the start of a new bit. If, however, a new falling edge is not detected by the target within 512 clock cycles since the last falling edge, a time-out occurs and the current command is discarded without affecting memory or the operating mode of the MCU. This is referred to as a soft-reset.

If a read command is issued but the data is not retrieved within 512 serial clock cycles, a soft-reset will occur causing the command to be disregarded. The data is not available for retrieval after the time-out has occurred. This is the expected behavior if the handshake protocol is not enabled. In order to allow the data to be retrieved even with a large clock frequency mismatch (between BDM and CPU) when the hardware

Table 6-3. DBGC1 Field Descriptions

Field	Description
7 ARM	**Arm Bit** — The ARM bit controls whether the DBG module is armed. This bit can be set and cleared by user software and is automatically cleared on completion of a debug session, or if a breakpoint is generated with tracing not enabled. On setting this bit the state sequencer enters State1. 0 Debugger disarmed 1 Debugger armed
6 TRIG	**Immediate Trigger Request Bit** — This bit when written to 1 requests an immediate trigger independent of state sequencer status. When tracing is complete a forced breakpoint may be generated depending upon DBGBRK and BDM bit settings. This bit always reads back a 0. Writing a 0 to this bit has no effect. If the DBGTCR_TSOURCE bit is clear no tracing is carried out. If tracing has already commenced using BEGIN trigger alignment, it continues until the end of the tracing session as defined by the TALIGN bit, thus TRIG has no affect. In secure mode tracing is disabled and writing to this bit cannot initiate a tracing session. The session is ended by setting TRIG and ARM simultaneously. 0 Do not trigger until the state sequencer enters the Final State. 1 Trigger immediately
4 BDM	**Background Debug Mode Enable** — This bit determines if a breakpoint causes the system to enter Background Debug Mode (BDM) or initiate a Software Interrupt (SWI). If this bit is set but the BDM is not enabled by the ENBDM bit in the BDM module, then breakpoints default to SWI. 0 Breakpoint to Software Interrupt if BDM inactive. Otherwise no breakpoint. 1 Breakpoint to BDM, if BDM enabled. Otherwise breakpoint to SWI
3 DBGBRK	**S12SDBG Breakpoint Enable Bit** — The DBGBRK bit controls whether the debugger will request a breakpoint on reaching the state sequencer Final State. If tracing is enabled, the breakpoint is generated on completion of the tracing session. If tracing is not enabled, the breakpoint is generated immediately. 0 No Breakpoint generated 1 Breakpoint generated
1–0 COMRV	**Comparator Register Visibility Bits** — These bits determine which bank of comparator register is visible in the 8-byte window of the S12SDBG module address map, located between 0x0028 to 0x002F. Furthermore these bits determine which register is visible at the address 0x0027. See Table 6-4.

Table 6-4. COMRV Encoding

COMRV	Visible Comparator	Visible Register at 0x0027
00	Comparator A	DBGSCR1
01	Comparator B	DBGSCR2
10	Comparator C	DBGSCR3
11	None	DBGMFR

6.3.2.2 Debug Status Register (DBGSR)

Address: 0x0021

	7	6	5	4	3	2	1	0
R	TBF	0	0	0	0	SSF2	SSF1	SSF0
W								
Reset	—	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-4. Debug Status Register (DBGSR)

each trace buffer entry. In Detail mode CINF comprises of R/W and size access information (CRW and CSZ respectively).

Single byte data accesses in Detail Mode are always stored to the low byte of the trace buffer (DATAL) and the high byte is cleared. When tracing word accesses, the byte at the lower address is always stored to trace buffer byte1 and the byte at the higher address is stored to byte0.

Table 6-37. Trace Buffer Organization (Normal,Loop1,Detail modes)

Mode	Entry Number	4-bits	8-bits	8-bits
		Field 2	Field 1	Field 0
Detail Mode	Entry 1	CINF1,ADRH1	ADRM1	ADRL1
		0	DATAH1	DATAL1
	Entry 2	CINF2,ADRH2	ADRM2	ADRL2
		0	DATAH2	DATAL2
Normal/Loop1 Modes	Entry 1	PCH1	PCM1	PCL1
	Entry 2	PCH2	PCM2	PCL2

6.4.5.3.1 Information Bit Organization

The format of the bits is dependent upon the active trace mode as described below.

Field2 Bits in Detail Mode

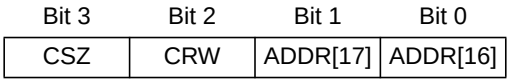

Figure 6-25. Field2 Bits in Detail Mode

In Detail Mode the CSZ and CRW bits indicate the type of access being made by the CPU.

Table 6-38. Field Descriptions

Bit	Description
3 CSZ	**Access Type Indicator**— This bit indicates if the access was a byte or word size when tracing in Detail Mode 0 Word Access 1 Byte Access
2 CRW	**Read Write Indicator** — This bit indicates if the corresponding stored address corresponds to a read or write access when tracing in Detail Mode. 0 Write Access 1 Read Access
1 ADDR[17]	**Address Bus bit 17**— Corresponds to system address bus bit 17.
0 ADDR[16]	**Address Bus bit 16**— Corresponds to system address bus bit 16.

7.6.1.4 Low-Voltage Interrupt (LVI)

In FPM the input voltage V_{DDA} is monitored. Whenever V_{DDA} drops below level $V_{LVIA,}$ the status bit LVDS is set to 1. On the other hand, LVDS is reset to 0 when V_{DDA} rises above level V_{LVID}. An interrupt, indicated by flag LVIF = 1, is triggered by any change of the status bit LVDS if interrupt enable bit LVIE = 1.

7.6.1.5 HTI - High Temperature Interrupt

In FPM the junction temperature T_J is monitored. Whenever T_J exceeds level T_{HTIA} the status bit HTDS is set to 1. Vice versa, HTDS is reset to 0 when T_J get below level T_{HTID}. An interrupt, indicated by flag HTIF = 1, is triggered by any change of the status bit HTDS, if interrupt enable bit HTIE = 1.

7.6.1.6 Autonomous Periodical Interrupt (API)

The API sub-block can generate periodical interrupts independent of the clock source of the MCU. To enable the timer, the bit APIFE needs to be set.

The API timer is either clocked by a trimmable internal RC oscillator (ACLK) or the Bus Clock. Timer operation will freeze when MCU clock source is selected and Bus Clock is turned off. The clock source can be selected with bit APICLK. APICLK can only be written when APIFE is not set.

The APIR[15:0] bits determine the interrupt period. APIR[15:0] can only be written when APIFE is cleared. As soon as APIFE is set, the timer starts running for the period selected by APIR[15:0] bits. When the configured time has elapsed, the flag APIF is set. An interrupt, indicated by flag APIF = 1, is triggered if interrupt enable bit APIE = 1. The timer is re-started automatically again after it has set APIF.

The procedure to change APICLK or APIR[15:0] is first to clear APIFE, then write to APICLK or APIR[15:0], and afterwards set APIFE.

The API Trimming bits APITR[5:0] must be set so the minimum period equals 0.2 ms if stable frequency is desired.

See Table 7-17 for the trimming effect of APITR.

NOTE

The first period after enabling the counter by APIFE might be reduced by API start up delay t_{sdel}.

It is possible to generate with the API a waveform at the external pin API_EXTCLK by setting APIFE and enabling the external access with setting APIEA.

7.7 Initialization/Application Information

8.1.3 Features

The basic features of the MSCAN are as follows:

- Implementation of the CAN protocol — Version 2.0A/B
  - — Standard and extended data frames
  - — Zero to eight bytes data length
  - — Programmable bit rate up to 1 Mbps[1]
  - — Support for remote frames
- Five receive buffers with FIFO storage scheme
- Three transmit buffers with internal prioritization using a "local priority" concept
- Flexible maskable identifier filter supports two full-size (32-bit) extended identifier filters, or four 16-bit filters, or eight 8-bit filters
- Programmable wakeup functionality with integrated low-pass filter
- Programmable loopback mode supports self-test operation
- Programmable listen-only mode for monitoring of CAN bus
- Programmable bus-off recovery functionality
- Separate signalling and interrupt capabilities for all CAN receiver and transmitter error states (warning, error passive, bus-off)
- Programmable MSCAN clock source either bus clock or oscillator clock
- Internal timer for time-stamping of received and transmitted messages
- Three low-power modes: sleep, power down, and MSCAN enable
- Global initialization of configuration registers

8.1.4 Modes of Operation

For a description of the specific MSCAN modes and the module operation related to the system operating modes refer to Section 8.4.4, "Modes of Operation".

8.2 External Signal Description

The MSCAN uses two external pins.

NOTE

On MCUs with an integrated CAN physical interface (transceiver) the MSCAN interface is connected internally to the transceiver interface. In these cases the external availability of signals TXCAN and RXCAN is optional.

8.2.1 RXCAN — CAN Receiver Input Pin

RXCAN is the MSCAN receiver input pin.

1. Depending on the actual bit timing and the clock jitter of the PLL.

Table 8-26. Message Buffer Organization

Offset Address	Register	Access
0x00X0	Identifier Register 0	R/W
0x00X1	Identifier Register 1	R/W
0x00X2	Identifier Register 2	R/W
0x00X3	Identifier Register 3	R/W
0x00X4	Data Segment Register 0	R/W
0x00X5	Data Segment Register 1	R/W
0x00X6	Data Segment Register 2	R/W
0x00X7	Data Segment Register 3	R/W
0x00X8	Data Segment Register 4	R/W
0x00X9	Data Segment Register 5	R/W
0x00XA	Data Segment Register 6	R/W
0x00XB	Data Segment Register 7	R/W
0x00XC	Data Length Register	R/W
0x00XD	Transmit Buffer Priority Register(1)	R/W
0x00XE	Time Stamp Register (High Byte)	R
0x00XF	Time Stamp Register (Low Byte)	R

1. Not applicable for receive buffers

Figure 8-24 shows the common 13-byte data structure of receive and transmit buffers for extended identifiers. The mapping of standard identifiers into the IDR registers is shown in Figure 8-25.

All bits of the receive and transmit buffers are 'x' out of reset because of RAM-based implementation[1]. All reserved or unused bits of the receive and transmit buffers always read 'x'.

Figure 8-24. Receive/Transmit Message Buffer — Extended Identifier Mapping

Register Name		Bit 7	6	5	4	3	2	1	Bit0
0x00X0 IDR0	R	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
	W								
0x00X1 IDR1	R	ID20	ID19	ID18	SRR (=1)	IDE (=1)	ID17	ID16	ID15
	W								
0x00X2 IDR2	R	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
	W								
0x00X3 IDR3	R	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
	W								

1. Exception: The transmit buffer priority registers are 0 out of reset.

Figure 8-24. Receive/Transmit Message Buffer — Extended Identifier Mapping (continued)

Register Name		Bit 7	6	5	4	3	2	1	Bit0
0x00X4 DSR0	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X5 DSR1	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X6 DSR2	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X7 DSR3	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X8 DSR4	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X9 DSR5	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XA DSR6	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XB DSR7	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XC DLR	R					DLC3	DLC2	DLC1	DLC0
	W								

= Unused, always read 'x'

Read:

- For transmit buffers, anytime when TXEx flag is set (see Section 8.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 8.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").
- For receive buffers, only when RXF flag is set (see Section 8.3.2.5, "MSCAN Receiver Flag Register (CANRFLG)").

Write:

Table 9-8. ATDCTL3 Field Descriptions

Field	Description
7 DJM	**Result Register Data Justification** — Result data format is always unsigned. This bit controls justification of conversion data in the result registers. 0 Left justified data in the result registers. 1 Right justified data in the result registers. Table 9-9 gives examples ATD results for an input signal range between 0 and 5.12 Volts.
6–3 S8C, S4C, S2C, S1C	**Conversion Sequence Length** — These bits control the number of conversions per sequence. Table 9-10 shows all combinations. At reset, S4C is set to 1 (sequence length is 4). This is to maintain software continuity to HC12 family.
2 FIFO	**Result Register FIFO Mode** — If this bit is zero (non-FIFO mode), the A/D conversion results map into the result registers based on the conversion sequence; the result of the first conversion appears in the first result register (ATDDR0), the second result in the second result register (ATDDR1), and so on. If this bit is one (FIFO mode) the conversion counter is not reset at the beginning or ending of a conversion sequence; sequential conversion results are placed in consecutive result registers. In a continuously scanning conversion sequence, the result register counter will wrap around when it reaches the end of the result register file. The conversion counter value (CC3-0 in ATDSTAT0) can be used to determine where in the result register file, the current conversion result will be placed. Aborting a conversion or starting a new conversion clears the conversion counter even if FIFO=1. So the first result of a new conversion sequence, started by writing to ATDCTL5, will always be place in the first result register (ATDDDR0). Intended usage of FIFO mode is continuos conversion (SCAN=1) or triggered conversion (ETRIG=1). Which result registers hold valid data can be tracked using the conversion complete flags. Fast flag clear mode may or may not be useful in a particular application to track valid data. If this bit is one, automatic compare of result registers is always disabled, that is ADC12B10C will behave as if ACMPIE and all CPME[*n*] were zero. 0 Conversion results are placed in the corresponding result register up to the selected sequence length. 1 Conversion results are placed in consecutive result registers (wrap around at end).
1–0 FRZ[1:0]	**Background Debug Freeze Enable** — When debugging an application, it is useful in many cases to have the ATD pause when a breakpoint (Freeze Mode) is encountered. These 2 bits determine how the ATD will respond to a breakpoint as shown in Table 9-11. Leakage onto the storage node and comparator reference capacitors may compromise the accuracy of an immediately frozen conversion depending on the length of the freeze period.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0010 PWMCNT4	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0011 PWMCNT5	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0012 PWMPER0	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0013 PWMPER1	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0014 PWMPER2	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0015 PWMPER3	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0016 PWMPER4	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0017 PWMPER5	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0018 PWMDTY0	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0019 PWMPER1	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x001A PWMPER2	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x001B PWMPER3	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x001C PWMPER4	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x001D PWMPER5	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x001E PWMSDB	R	PWMIF	PWMIE	0	PWMLVL	0	PWM5IN	PWM5INL	PWM5ENA
	W			PWMRSTRT					

= Unimplemented or Reserved

Figure 10-2. PWM Register Summary (continued)

11.1.4 Block Diagram

Figure 11-1 is a high level block diagram of the SCI module, showing the interaction of various function blocks.

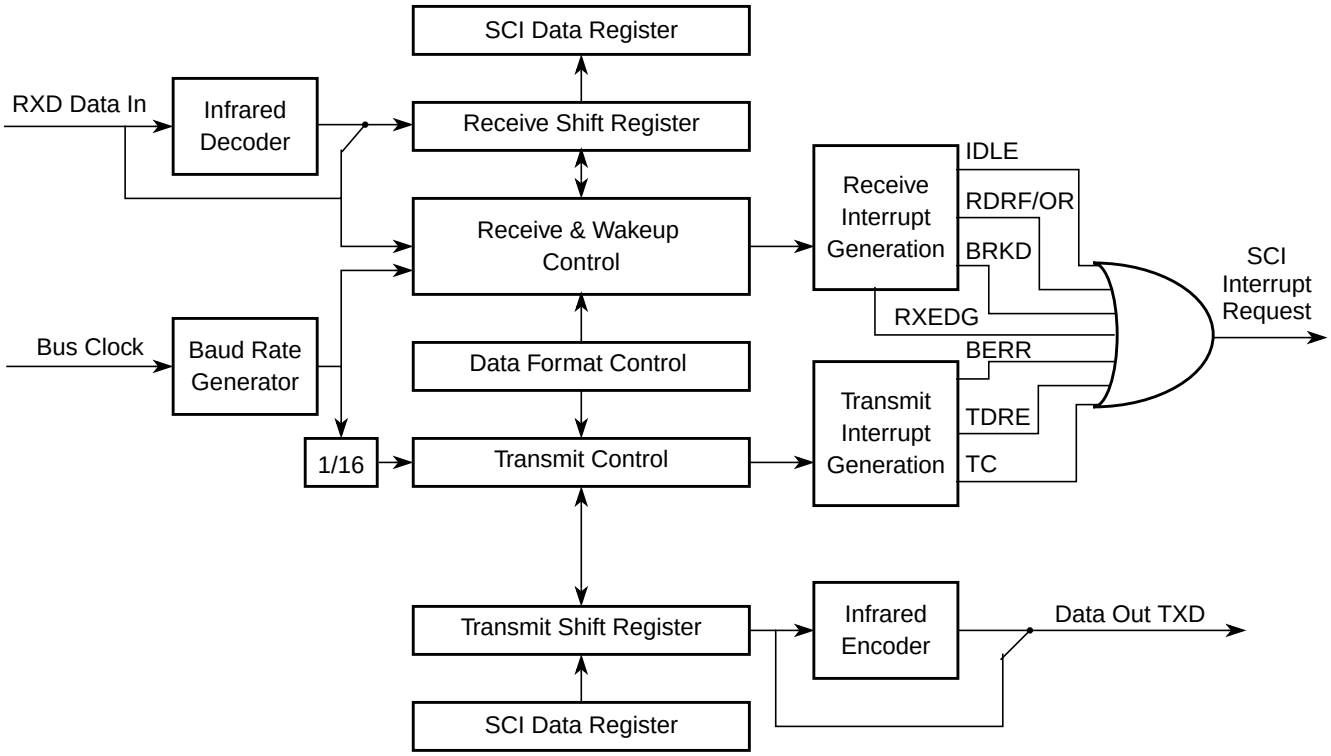

Figure 11-1. SCI Block Diagram

11.2 External Signal Description

The SCI module has a total of two external pins.

11.2.1 TXD — Transmit Pin

The TXD pin transmits SCI (standard or infrared) data. It will idle high in either mode and is high impedance anytime the transmitter is disabled.

11.2.2 RXD — Receive Pin

The RXD pin receives SCI (standard or infrared) data. An idle line is detected as a line high. This input is ignored when the receiver is disabled and should be terminated to a known voltage.

11.3 Memory Map and Register Definition

This section provides a detailed description of all the SCI registers.

To determine the value of a data bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 11-18 summarizes the results of the data bit samples.

Table 11-18. Data Bit Recovery

RT8, RT9, and RT10 Samples	Data Bit Determination	Noise Flag
000	0	0
001	0	1
010	0	1
011	1	1
100	0	1
101	1	1
110	1	1
111	1	0

NOTE

The RT8, RT9, and RT10 samples do not affect start bit verification. If any or all of the RT8, RT9, and RT10 start bit samples are logic 1s following a successful start bit verification, the noise flag (NF) is set and the receiver assumes that the bit is a start bit (logic 0).

To verify a stop bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 11-19 summarizes the results of the stop bit samples.

Table 11-19. Stop Bit Recovery

RT8, RT9, and RT10 Samples	Framing Error Flag	Noise Flag
000	1	0
001	1	1
010	1	1
011	0	1
100	1	1
101	0	1
110	0	1
111	0	0

In Figure 11-22 the verification samples RT3 and RT5 determine that the first low detected was noise and not the beginning of a start bit. The RT clock is reset and the start bit search begins again. The noise flag is not set because the noise occurred before the start bit was found.

P_{IO} is the sum of all output currents on I/O ports associated with V_{DDX}, whereby

$$R_{DSON} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

$$R_{DSON} = \frac{V_{DD35} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

Table A-5. Thermal Package Characteristics(1)

Num	C	Rating	Symbol	Min	Typ	Max	Unit
QFN 48							
1	D	Thermal resistance QFN 48, single sided PCB(2)	θ_{JA}	—	—	82	°C/W
2	D	Thermal resistance QFN 48, double sided PCB with 2 internal planes(3)	θ_{JA}	—	—	28	°C/W
3	D	Junction to Board QFN 48	θ_{JB}	—	—	11	°C/W
4	D	Junction to Case QFN 48[4]	θ_{JC}	—	—	1.4	°C/W
5	D	Junction to Case (Bottom) QFN 48[5]	Ψ_{JT}	—	—	4	°C/W
QFP 80							
6	D	Thermal resistance QFP 80, single sided PCB[2]	θ_{JA}	—	—	56	°C/W
7	D	Thermal resistance QFP 80, double sided PCB with 2 internal planes[3]	θ_{JA}	—	—	43	°C/W
8	D	Junction to Board QFP 80	θ_{JB}	—	—	28	°C/W
9	D	Junction to Case QFP 80(4)	θ_{JC}	—	—	19	°C/W
10	D	Junction to Package Top QFP 80(5)	Ψ_{JT}	—	—	5	°C/W
LQFP 64							
11	D	Thermal resistance LQFP 64, single sided PCB[2]	θ_{JA}	—	—	70	°C/W
12	D	Thermal resistance LQFP 64, double sided PCB with 2 internal planes[3]	θ_{JA}	—	—	52	°C/W
13	D	Junction to Board LQFP 64	θ_{JB}	—	—	35	°C/W
14	D	Junction to Case LQFP 64(6)	θ_{JC}	—	—	17	°C/W
15	D	Junction to Package Top LQFP 64(7)	Ψ_{JT}	—	—	3	°C/W

1. The values for thermal resistance are achieved by package simulations
2. Junction to ambient thermal resistance, θ_{JA} was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection.
3. Junction to ambient thermal resistance, θ_{JA} was simulated to be equivalent to the JEDEC specification JESD51-7 in a horizontal configuration in natural convection.