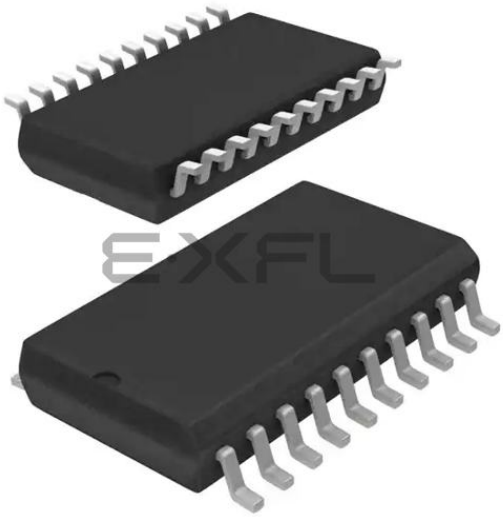

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST6
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI
Peripherals	LED, LVD, POR, WDT
Number of I/O	13
Program Memory Size	3.8KB (3.8K x 8)
Program Memory Type	OTP
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6V
Data Converters	A/D 7x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st62t60cm6

1.2 PIN DESCRIPTIONS

V_{DD} and V_{SS}. Power is supplied to the MCU via these two pins. V_{DD} is the power connection and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected to the on-chip oscillator circuit. A quartz crystal, a ceramic resonator or an external clock signal can be connected between these two pins. The OSCin pin is the input pin, the OSCout pin is the output pin.

$\overline{\text{RESET}}$. The active-low $\overline{\text{RESET}}$ pin is used to restart the microcontroller.

TEST/V_{PP}. The TEST must be held at V_{SS} for normal operation. If TEST pin is connected to a +12.5V level during the reset phase, the EPROM/ OTP programming Mode is entered.

NMI. The NMI pin provides the capability for asynchronous interruption, by applying an external non maskable interrupt to the MCU. It is provided with an on-chip pullup resistor (if option has been enabled), and Schmitt trigger characteristics.

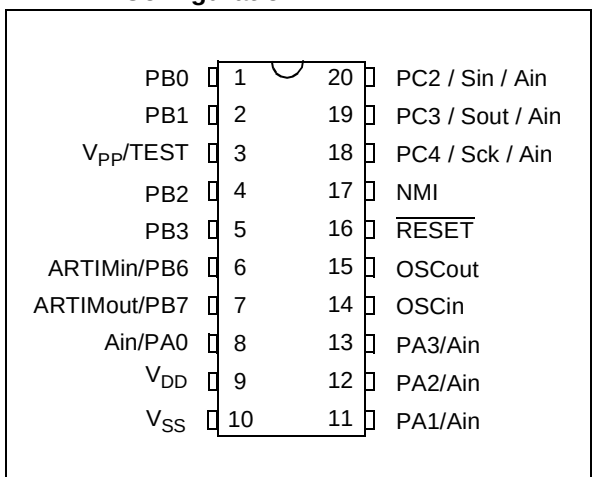
PA0-PA3. These 4 lines are organized as one I/O port (A). Each line may be configured under software control as inputs with or without internal pullup resistors, interrupt generating inputs with pullup resistors, open-drain or push-pull outputs, analog inputs for the A/D converter.

PB0-PB3. These 4 lines are organized as one I/O port (B). Each line may be configured under software control as inputs with or without internal pullup resistors, interrupt generating inputs with pullup resistors, open-drain or push-pull outputs.
PB0-PB3 can also sink 30mA for direct LED driving.

PB6/ARTIMin, PB7/ARTIMout. These pins are either Port B I/O bits or the Input and Output pins of the AR TIMER. To be used as timer input function PB6 has to be programmed as input with or without pull-up. A dedicated bit in the AR TIMER Mode Control Register sets PB7 as timer output function. PB6-PB7 can also sink 30mA for direct LED driving.

PC2-PC4. These 3 lines are organized as one I/O port (C). Each line may be configured under software control as input with or without internal pullup resistor, interrupt generating input with pull-up resistor, analog input for the A/D converter, open-drain or push-pull output.
PC2-PC4 can also be used as respectively Data in, Data out and Clock I/O pins for the on-chip SPI to carry the synchronous serial I/O signals.

Figure 2ST62T53C/T60C/T63C/E60C Pin Configuration



MEMORY MAP (Cont'd)

1.3.6 Data RAM/EEPROM Bank Register (DRBR)

Address: E8h — Write only

7							0
-	-	-	DRBR 4	-	-	DRBR 1	DRBR 0

Bit 7-5 = These bits are not used

Bit 4 - **DRBR4**. This bit, when set, selects RAM Page 2.

Bit 3-2 - Reserved. These bits are not used.

Bit 1 - **DRBR1**. This bit, when set, selects EEPROM Page 1, when available.

Bit 0 - **DRBR0**. This bit, when set, selects EEPROM Page 0, when available.

The selection of the bank is made by programming the Data RAM Bank Switch register (DRBR register) located at address E8h of the Data Space according to Table 1. No more than one bank should be set at a time.

The DRBR register can be addressed like a RAM Data Space at the address E8h; nevertheless it is a write only register that cannot be accessed with single-bit operations. This register is used to select the desired 64-byte RAM/EEPROM bank of the Data Space. The bank number has to be loaded in the DRBR register and the instruction has to point to the selected location as if it was in bank 0 (from 00h address to 3Fh address).

This register is not cleared during the MCU initialization, therefore it must be written before the first access to the Data Space bank region. Refer to the Data Space description for additional information. The DRBR register is not modified when an interrupt or a subroutine occurs.

Notes :

Care is required when handling the DRBR register as it is write only. For this reason, it is not allowed to change the DRBR contents while executing interrupt service routine, as the service routine cannot save and then restore its previous content. If it is impossible to avoid the writing of this register in interrupt service routine, an image of this register must be saved in a RAM location, and each time the program writes to DRBR it must write also to the image register. The image register must be written first, so if an interrupt occurs between the two instructions the DRBR is not affected.

In DRBR Register, only 1 bit must be set. Otherwise two or more pages are enabled in parallel, producing errors.

Care must also be taken not to change the E²PROM page (when available) when the parallel writing mode is set for the E²PROM, as defined in EECTL register.

Table 3Data RAM Bank Register Set-up

DRBR	ST62T53C	ST62T60C/E60C	ST62T63C
00	None	None	None
01	Not Available	EEPROM Page 0	EEPROM Page 0
02	Not Available	EEPROM Page 1	Not Available
08	Not Available	Not Available	Not Available
10h	RAM Page 2	RAM Page 2	RAM Page 2
other	Reserved	Reserved	Reserved

1.4 PROGRAMMING MODES

1.4.1 Option Bytes

The two Option Bytes allow configuration capability to the MCUs. Option byte's content is automatically read, and the selected options enabled, when the chip reset is activated.

It can only be accessed during the programming mode. This access is made either automatically (copy from a master device) or by selecting the OPTION BYTE PROGRAMMING mode of the programmer.

The option bytes are located in a non-user map. No address has to be specified.

EPROM Code Option Byte (LSB)

7							0
PRO-TECT	EXTC-NTL	PB2-3 PULL	PB0-1 PULL	WDACT	DE-LAY	OSCIL	OSGEN

EPROM Code Option Byte (MSB)

15							8
-	-	-	ADC SYNCHRO	-	-	NMI PULL	LVD

D15-D13. Reserved. Must be cleared.

ADC SYNCHRO. When set, an A/D conversion is started upon WAIT instruction execution, in order to reduce supply noise. When this bit is low, an A/D conversion is started as soon as the STA bit of the A/D Converter Control Register is set.

D11. Reserved, must be set to one.

D10. Reserved, must be cleared.

NMI PULL. *NMI Pull-Up*. This bit must be set high to configure the NMI pin with a pull-up resistor. When it is low, no pull-up is provided.

LVD. *LVD RESET enable.*When this bit is set, safe RESET is performed by MCU when the supply voltage is too low. When this bit is cleared, only power-on reset or external RESET are active.

PROTECT. *Readout Protection.* This bit allows the protection of the software contents against piracy. When the bit PROTECT is set high, readout of the OTP contents is prevented by hardware.. When this bit is low, the user program can be read.

EXTCNTL. *External STOP MODE control.*. When EXTCNTL is high, STOP mode is available with watchdog active by setting NMI pin to one. When EXTCNTL is low, STOP mode is not available with the watchdog active.

PB2-3 PULL. When set this bit removes pull-up at reset on PB2-PB3 pins. When cleared PB2-PB3 pins have an internal pull-up resistor at reset.

PB0-1 PULL. When set this bit removes pull-up at reset on PB0-PB1 pins. When cleared PB0-PB1 pins have an internal pull-up resistor at reset.

WDACT. This bit controls the watchdog activation. When it is high, hardware activation is selected. The software activation is selected when WDACT is low.

DELAY. This bit enables the selection of the delay internally generated after the internal reset (external pin, LVD, or watchdog activated) is released. When DELAY is low, the delay is 2048 cycles of the oscillator, it is of 32768 cycles when DELAY is high.

OSCIL. *Oscillator selection*. When this bit is low, the oscillator must be controlled by a quartz crystal, a ceramic resonator or an external frequency. When it is high, the oscillator must be controlled by an RC network, with only the resistor having to be externally provided.

OSGEN. *Oscillator Safe Guard*. This bit must be set high to enable the Oscillator Safe Guard. When this bit is low, the OSG is disabled.

The Option byte is written during programming either by using the PC menu (PC driven Mode) or automatically (stand-alone mode).

PROGRAMMING MODES (Cont'd)

1.4.2 EPROM Erasing

The EPROM of the windowed package of the MCUs may be erased by exposure to Ultra Violet light. The erasure characteristic of the MCUs is such that erasure begins when the memory is exposed to light with a wave lengths shorter than approximately 4000Å. It should be noted that sunlights and some types of fluorescent lamps have wavelengths in the range 3000-4000Å.

It is thus recommended that the window of the MCUs packages be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.

The recommended erasure procedure of the MCUs EPROM is the exposure to short wave ultraviolet light which have a wave-length 2537A. The integrated dose (i.e. U.V. intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm^2 power rating. The ST62E60C should be placed within 2.5cm (1Inch) of the lamp tubes during erasure.

2 CENTRAL PROCESSING UNIT

2.1 INTRODUCTION

The CPU Core of ST6 devices is independent of the I/O or Memory configuration. As such, it may be thought of as an independent central processor communicating with on-chip I/O, Memory and Peripherals via internal address, data, and control buses. In-core communication is arranged as shown in Figure 7; the controller being externally linked to both the Reset and Oscillator circuits, while the core is linked to the dedicated on-chip peripherals via the serial data bus and indirectly, for interrupt purposes, through the control registers.

2.2 CPU REGISTERS

The ST6 Family CPU core features six registers and three pairs of flags available to the programmer. These are described in the following paragraphs.

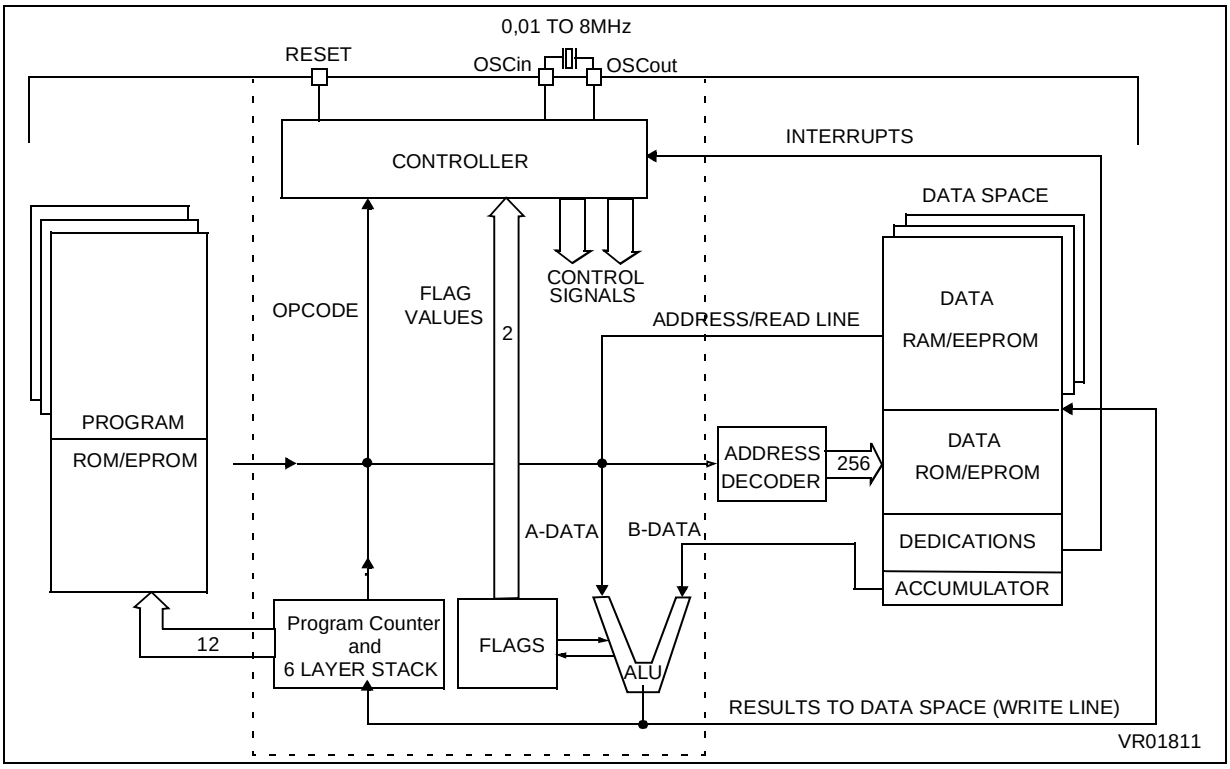
Accumulator (A). The accumulator is an 8-bit general purpose register used in all arithmetic calculations, logical operations, and data manipulations. The accumulator can be addressed in Data space as a RAM location at address FFh. Thus the ST6 can manipulate the accumulator just like any other register in Data space.

Indirect Registers (X, Y). These two indirect registers are used as pointers to memory locations in Data space. They are used in the register-indirect addressing mode. These registers can be addressed in the data space as RAM locations at addresses 80h (X) and 81h (Y). They can also be accessed with the direct, short direct, or bit direct addressing modes. Accordingly, the ST6 instruction set can use the indirect registers as any other register of the data space.

Short Direct Registers (V, W). These two registers are used to save a byte in short direct addressing mode. They can be addressed in Data space as RAM locations at addresses 82h (V) and 83h (W). They can also be accessed using the direct and bit direct addressing modes. Thus, the ST6 instruction set can use the short direct registers as any other register of the data space.

Program Counter (PC). The program counter is a 12-bit register which contains the address of the next ROM location to be processed by the core. This ROM location may be an opcode, an operand, or the address of an operand. The 12-bit length allows the direct addressing of 4096 bytes in Program space.

Figure 7. ST6 Core Block Diagram



CLOCK SYSTEM (Cont'd)

Figure 10. OSG Filtering Principle

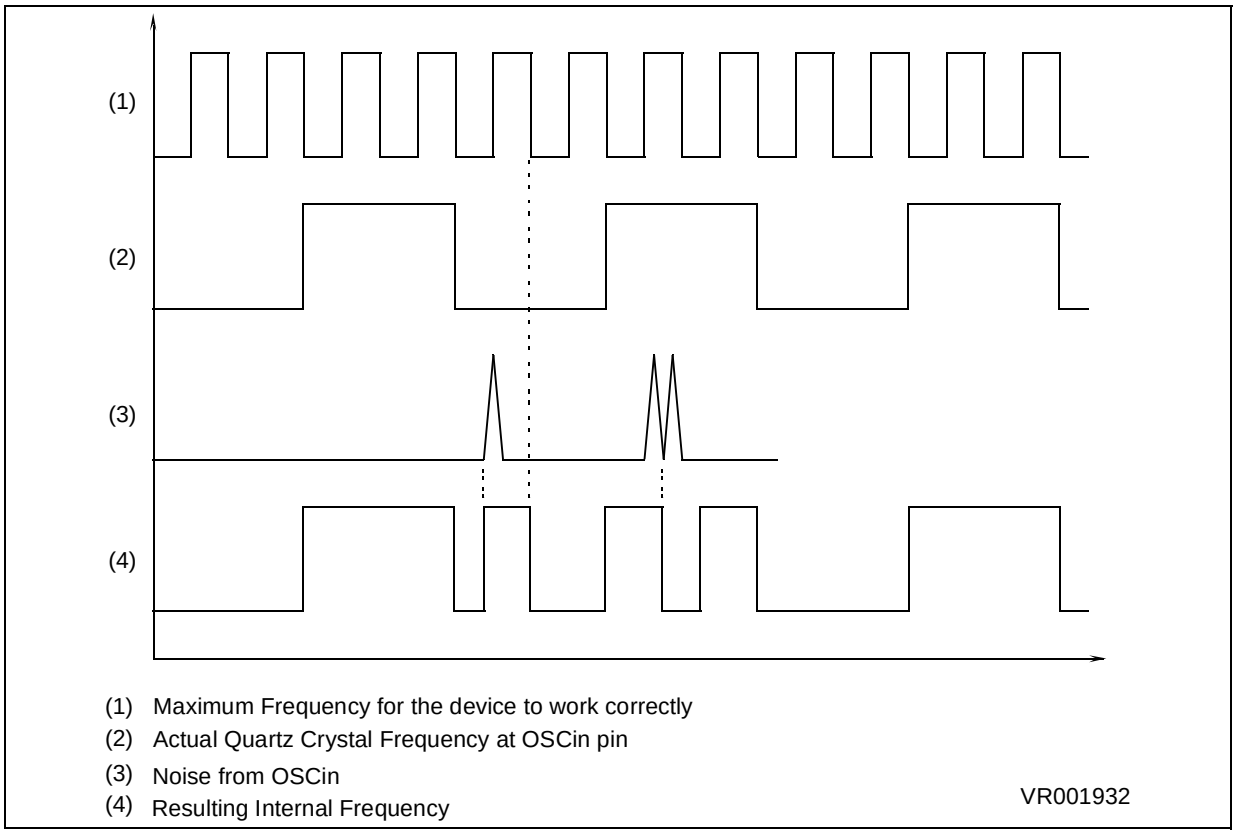
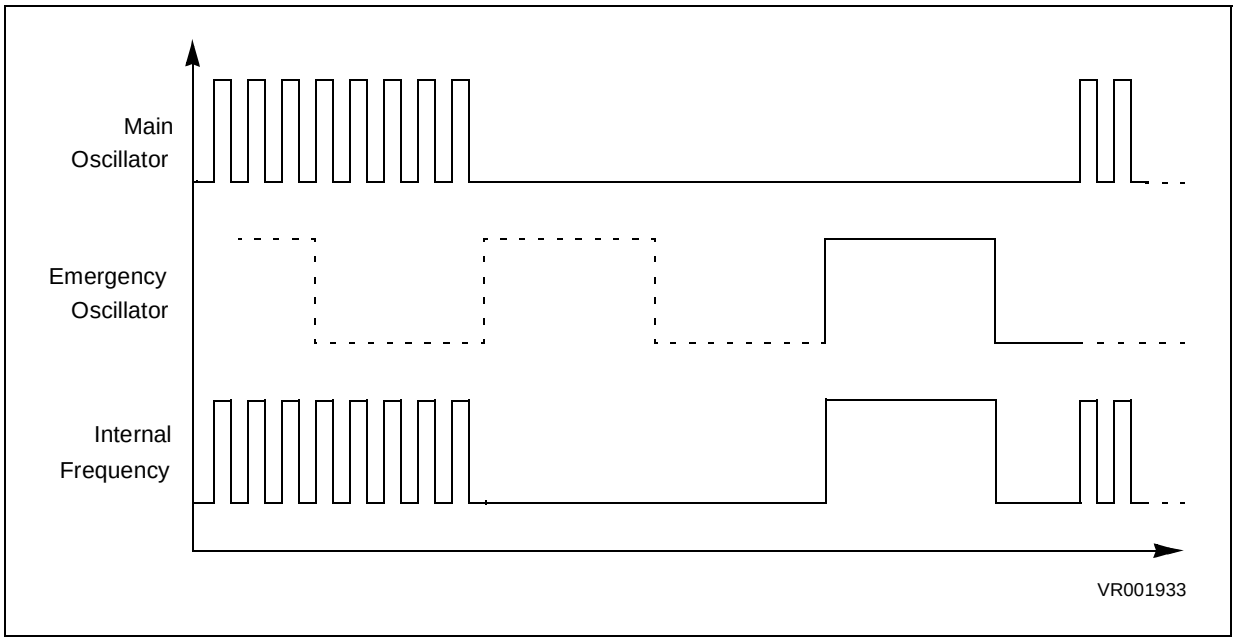


Figure 11. OSG Emergency Oscillator Principle



3.3 DIGITAL WATCHDOG

The digital Watchdog consists of a reloadable downcounter timer which can be used to provide controlled recovery from software upsets.

The Watchdog circuit generates a Reset when the downcounter reaches zero. User software can prevent this reset by reloading the counter, and should therefore be written so that the counter is regularly reloaded while the user program runs correctly. In the event of a software mishap (usually caused by externally generated interference), the user program will no longer behave in its usual fashion and the timer register will thus not be reloaded periodically. Consequently the timer will decrement down to 00h and reset the MCU. In order to maximise the effectiveness of the Watchdog function, user software must be written with this concept in mind.

Watchdog behaviour is governed by two options, known as “WATCHDOG ACTIVATION” (i.e. HARDWARE or SOFTWARE) and “EXTERNAL STOP MODE CONTROL” (see Table 6).

In the SOFTWARE option, the Watchdog is disabled until bit C of the DWDR register has been set. When the Watchdog is disabled, low power Stop mode is available. Once activated, the Watchdog cannot be disabled, except by resetting the MCU.

In the HARDWARE option, the Watchdog is permanently enabled. Since the oscillator will run continuously, low power mode is not available. The STOP instruction is interpreted as a WAIT instruction, and the Watchdog continues to countdown.

However, when the EXTERNAL STOP MODE CONTROL option has been selected low power consumption may be achieved in Stop Mode.

Execution of the STOP instruction is then governed by a secondary function associated with the NMI pin. If a STOP instruction is encountered when the NMI pin is low, it is interpreted as WAIT, as described above. If, however, the STOP instruction is encountered when the NMI pin is high, the Watchdog counter is frozen and the CPU enters STOP mode.

When the MCU exits STOP mode (i.e. when an interrupt is generated), the Watchdog resumes its activity.

Table 6. Recommended Option Choices

Functions Required	Recommended Options
Stop Mode & Watchdog	“EXTERNAL STOP MODE” & “HARDWARE WATCHDOG”
Stop Mode	“SOFTWARE WATCHDOG”
Watchdog	“HARDWARE WATCHDOG”

I/O PORTS (Cont'd)

4.1.1 Operating Modes

Each pin may be individually programmed as input or output with various configurations.

This is achieved by writing the relevant bit in the Data (DR), Data Direction (DDR) and Option registers (OR). Table 10 illustrates the various port configurations which can be selected by user software.

4.1.1.1 Input Options

Pull-up, High Impedance Option. All input lines can be individually programmed with or without an internal pull-up by programming the OR and DR registers accordingly. If the pull-up option is not selected, the input pin will be in the high-impedance state.

4.1.1.2 Interrupt Options

All input lines can be individually connected by software to the interrupt system by programming the OR and DR registers accordingly. The interrupt trigger modes (falling edge, rising edge and low level) can be configured by software as described in the Interrupt Chapter for each port.

4.1.1.3 Analog Input Options

Some pins can be configured as analog inputs by programming the OR and DR registers accordingly. These analog inputs are connected to the on-chip 8-bit Analog to Digital Converter. *ONLY ONE* pin should be programmed as an analog input at any time, since by selecting more than one input simultaneously their pins will be effectively shorted.

Table 10. I/O Port Option Selection

DDR	OR	DR	Mode	Option
0	0	0	Input	With pull-up, no interrupt
0	0	1	Input	No pull-up, no interrupt
0	1	0	Input	With pull-up and with interrupt
0	1	1	Input	Analog input (when available)
1	0	X	Output	Open-drain output (20mA sink when available)
1	1	X	Output	Push-pull output (20mA sink when available)

Note: X = Don't care

I/O PORTS (Cont'd)

4.1.3 AR Timer Alternate function Option

When bit PWMOE of register ARMC is low, pin ARTIMout/PB7 is configured as any standard pin of port B through the port registers. When PWMOE is high, ARTIMout/PB7 is the PWM output, independently of the port registers configuration.

ARTIMin/PB6 is connected to the AR Timer input. It is configured through the port registers as any standard pin of port B. To use ARTIMin/PB6 as AR Timer input, it must be configured as input through DDRB.

4.1.4 SPI Alternate function Option

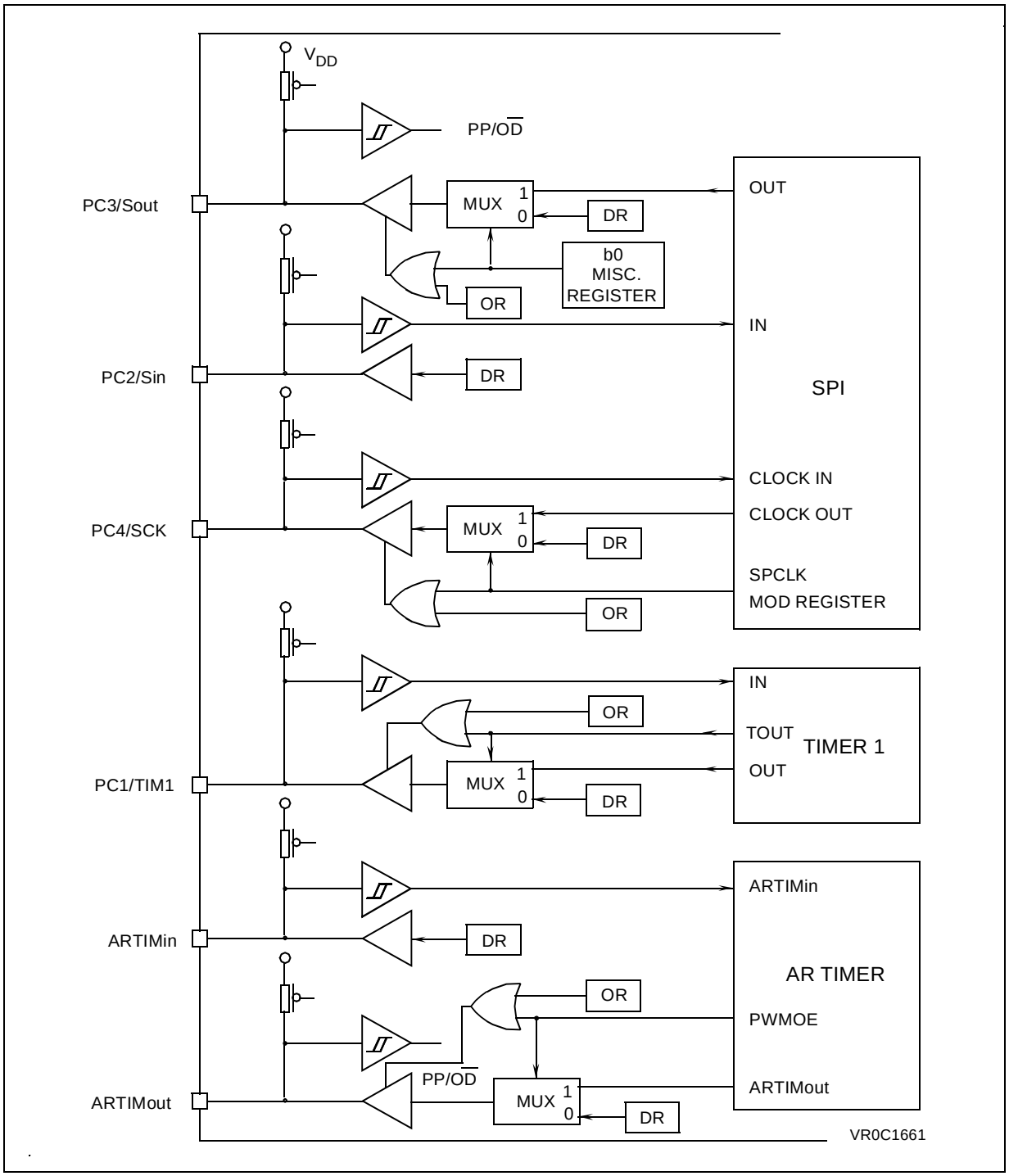
PC2/PC4 are used as standard I/O as long as bit SPCLK of the SPI Mode Register is kept low. When PC2/Sin is configured as input, it is automatically connected to the SPI shift register input, independent of the state at SPCLK.

PC3/SOUT is configured as SPI push-pull output by setting bit 0 of the Miscellaneous register (address DDh), regardless of the state of Port C registers. PC4/SCK is configured as push-pull output clock (master mode) by programming it as push-pull output through DDRC register and by setting bit SPCLK of the SPI Mode Register.

PC4/SCK is configured as input clock (slave mode) by programming it as input through DDRC register and by clearing bit SPCLK of the SPI Mode Register. With this configuration, PC4 can simultaneously be used as an input.

I/O PORTS (Cont'd)

Figure 25Peripheral Interface Configuration of SPI, Timer 1 and AR Timer



4.2 TIMER

The MCU features an on-chip Timer peripheral, consisting of an 8-bit counter with a 7-bit programmable prescaler, giving a maximum count of 2^{15}.

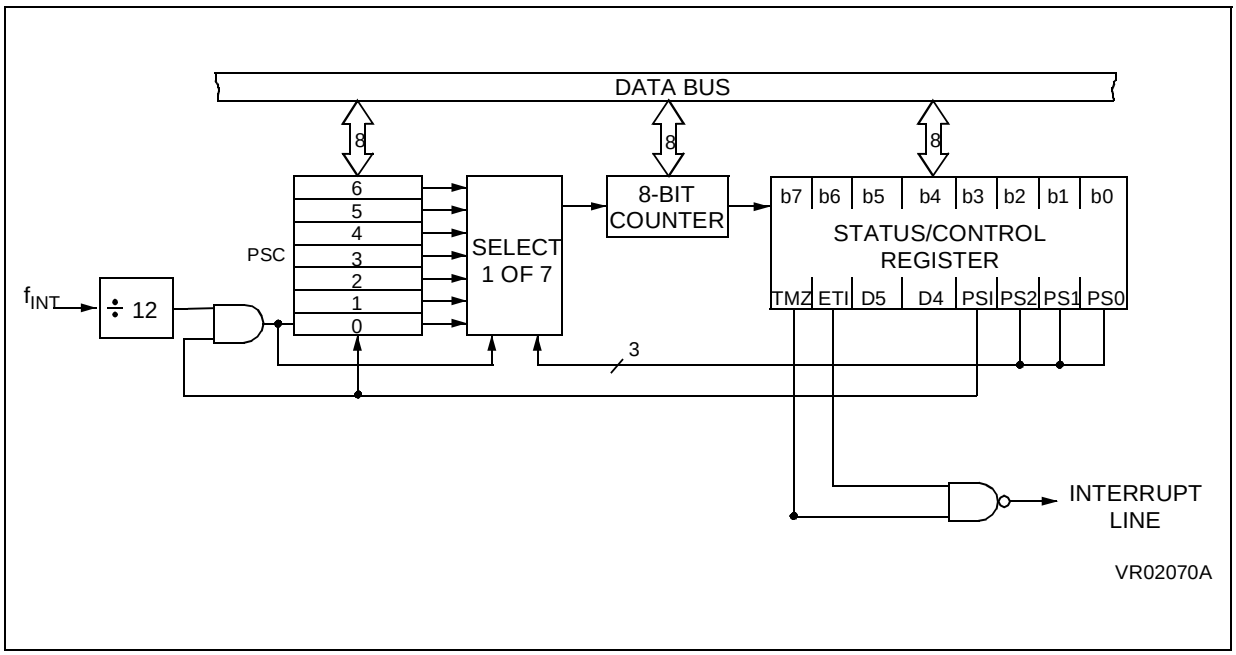
Figure 26 shows the Timer Block Diagram. The content of the 8-bit counter can be read/written in the Timer/Counter register, TCR, which can be addressed in Data space as a RAM location at address 0D3h. The state of the 7-bit prescaler can be read in the PSC register at address 0D2h. The control logic device is managed in the TSCR register as described in the following paragraphs.

The 8-bit counter is decrement by the output (rising edge) coming from the 7-bit prescaler and can be loaded and read under program control. When it decrements to zero then the TMZ (Timer Zero)bit in the TSCR is set. If the ETI (Enable Timer Interrupt) bit in the TSCR is also set, an interrupt request is generated. The Timer interrupt can be used to exit the MCU from WAIT mode.

The prescaler input is the internal frequency (f_{INT}) divided by 12. The prescaler decrements on the rising edge. Depending on the division factor programmed by PS2, PS1 and PS0 bits in the TSCR (see Figure 12), the clock input of the timer/counter register is multiplexed to different sources. For division factor 1, the clock input of the prescaler is also that of timer/counter; for factor 2, bit 0 of the prescaler register is connected to the clock input of TCR. This bit changes its state at half the frequency of the prescaler input clock. For factor 4, bit 1 of the PSC is connected to the clock input of TCR, and so forth. The prescaler initialize bit, PSI, in the TSCR register must be set to allow the prescaler (and hence the counter) to start. If it is cleared, all the prescaler bits are set and the counter is inhibited from counting. The prescaler can be loaded with any value between 0 and 7Fh, if bit PSI is set. The prescaler tap is selected by means of the PS2/PS1/PS0 bits in the control register.

Figure 27 illustrates the Timer's working principle.

Figure 26. Timer Block Diagram



TIMER (Cont'd)

A write to the TCR register will predominate over the 8-bit counter decrement to 00h function, i.e. if a write and a TCR register decrement to 00h occur simultaneously, the write will take precedence, and the TMZ bit is not set until the 8-bit counter reaches 00h again. The values of the TCR and the PSC registers can be read accurately at any time.

4.2.4 Timer Registers

Timer Status Control Register (TSCR)

Address: 0D4h — Read/Write

7							0
TMZ	ETI	D5	D4	PSI	PS2	PS1	PS0

Bit 7 = **TMZ**: *Timer Zero bit*

A low-to-high transition indicates that the timer count register has decrement to zero. This bit must be cleared by user software before starting a new count.

Bit 6 = **ETI**: *Enable Timer Interrup*

When set, enables the timer interrupt request (vector #4). If ETI=0 the timer interrupt is disabled. If ETI=1 and TMZ=1 an interrupt request is generated.

Bit 5 = **D5**: *Reserved*

Must be set to "1".

Bit 4 = **D4**

Do not care.

Bit 3 = **PSI**: *Prescaler Initialize Bit*

Used to initialize the prescaler and inhibit its counting. When PSI="0" the prescaler is set to 7Fh and the counter is inhibited. When PSI="1" the prescaler is enabled to count downwards. As long as PSI="0" both counter and prescaler are not running.

Bit 2, 1, 0 = **PS2, PS1, PS0**: *Prescaler Mux. Select*. These bits select the division ratio of the prescaler register.

Table 12. Prescaler Division Factors

PS2	PS1	PS0	Divided by
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Timer Counter Register (TCR)

Address: 0D3h — Read/Write

7							0
D7	D6	D5	D4	D3	D2	D1	D0

Bit 7-0 = **D7-D0**: *Counter Bits.*

Prescaler Register PSC

Address: 0D2h — Read/Write

7							0
D7	D6	D5	D4	D3	D2	D1	D0

Bit 7 = **D7**: Always read as "0".

Bit 6-0 = **D6-D0**: Prescaler Bits.

A/D CONVERTER (Cont'd)

Since the ADC is on the same chip as the microprocessor, the user should not switch heavily loaded output signals during conversion, if high precision is required. Such switching will affect the supply voltages used as analog references.

The accuracy of the conversion depends on the quality of the power supplies (V_{DD} and V_{SS}). The user must take special care to ensure a well regulated reference voltage is present on the V_{DD} and V_{SS} pins (power supply voltage variations must be less than 5V/ms). This implies, in particular, that a suitable decoupling capacitor is used at the V_{DD} pin.

The converter resolution is given by::

$$\frac{V_{DD} - V_{SS}}{256}$$

The Input voltage (Ain) which is to be converted must be constant for 1µs before conversion and remain constant during conversion.

Conversion resolution can be improved if the power supply voltage (V_{DD}) to the microcontroller is lowered.

In order to optimise conversion resolution, the user can configure the microcontroller in WAIT mode, because this mode minimises noise disturbances and power supply variations due to output switching. Nevertheless, the WAIT instruction should be executed as soon as possible after the beginning of the conversion, because execution of the WAIT instruction may cause a small variation of the V_{DD} voltage. The negative effect of this variation is minimized at the beginning of the conversion when the converter is less sensitive, rather than at the end of conversion, when the less significant bits are determined.

The best configuration, from an accuracy standpoint, is WAIT mode with the Timer stopped. Indeed, only the ADC peripheral and the oscillator are then still working. The MCU must be woken up from WAIT mode by the ADC interrupt at the end of the conversion. It should be noted that waking up the microcontroller could also be done using the Timer interrupt, but in this case the Timer will be working and the resulting noise could affect conversion accuracy.

One extra feature is available in the ADC to get a better accuracy. In fact, each ADC conversion has to be followed by a WAIT instruction to minimize the noise during the conversion. But the first conversion step is performed before the execution of the WAIT when most of clocks signals are still enabled . The key is to synchronize the ADC start with the effective execution of the WAIT. This is achieved by setting ADC SYNC option. This way, ADC conversion starts in effective WAIT for maximum accuracy.

Note: With this extra option, it is mandatory to execute WAIT instruction just after ADC start instruction. Insertion of any extra instruction may cause spurious interrupt request at ADC interrupt vector.

A/D Converter Control Register (ADCR)

Address: 0D1h — Read/Write

7							0
EAI	EOC	STA	PDS	D3	D2	D1	D0

Bit 7 = **EAI**: *Enable A/D Interrupt.* If this bit is set to "1" the A/D interrupt is enabled, when EAI=0 the interrupt is disabled.

Bit 6 = **EOC**: *End of conversion. Read Only*. This read only bit indicates when a conversion has been completed. This bit is automatically reset to "0" when the STA bit is written. If the user is using the interrupt option then this bit can be used as an interrupt pending bit. Data in the data conversion register are valid only when this bit is set to "1".

Bit 5 = **STA***: Start of Conversion. Write Only*. Writing a "1" to this bit will start a conversion on the selected channel and automatically reset to "0" the EOC bit. If the bit is set again when a conversion is in progress, the present conversion is stopped and a new one will take place. This bit is write only, any attempt to read it will show a logical zero.

Bit 4 = **PDS***: Power Down Selection.* This bit activates the A/D converter if set to "1". Writing a "0" to this bit will put the ADC in power down mode (idle mode).

Bit 3-0 = **D3-D0.** Not used

A/D Converter Data Register (ADR)

Address: 0D0h — Read only

7							0
D7	D6	D5	D4	D3	D2	D1	D0

Bit 7-0 = **D7-D0***: 8 Bit A/D Conversion Result.*

SERIAL PERIPHERAL INTERFACE SPI (Cont'd)

SPI DIV Register (DIV)

Address: E1h — Read/Write

Reset status: 00h

7							0
SPINT	DOV6	DIV5	DIV4	DIV3	CD2	CD1	CD0

The SPIDIV register defines the transmission rate and frame format and contains the interrupt flag.

Bits CD0-CD2, DIV3-DIV6 are read/write while SPINT can be read and cleared only. Write access is not allowed if SPRUN in the MOD register is set.

Bit 7 = **SPINT**: *Interrupt Flag.* If SPIE bit=1, SPINT is automatically set to one by the SPI at the end of a transmission or reception and an interrupt request can be generated depending on the state of the interrupt mask bit in the MOD control register. This bit is write and read and must be cleared by user software at the end of the interrupt service routine.

Bit 6-3 = **DIV6-DIV3**: *Burst Mode Bit Clock Period Selection.* Define the number of shift register bits that are transmitted or received in a frame. The available selections are listed in Table 16. The normal maximum setting is 8 bits, since the shift register is 8 bits wide. Note that by setting a greater number of bits, in conjunction with the SPIN bit in the MOD register, unwanted data bits may be filtered from the data stream.

Bit 2-0 = **CD2-CD0**: *Base/Bit Clock Rate Selection*. Define the division ratio between the core clock (f_{INT} divided by 13) and the clock supplied to the Shift Register in Master mode.

Table 15. Base/Bit Clock Ratio Selection

CD2-CD0			Divide Ratio (decimal)
0	0	0	Divide by 1
0	0	1	Divide by 2
0	1	0	Divide by 4
0	1	1	Divide by 8
1	0	0	Divide by 16
1	0	1	Divide by 32
1	1	0	Divide by 64
1	1	1	Divide by 256

Note: For example, when an 8MHz CPU clock is used, asynchronous operation at 9600 Baud is possible (8MHz/13/64). Other Baud rates are available by proportionally selecting division factors depending on CPU clock frequency.

Data setup time on Sin is typically 250ns min, while data hold time is typically 50ns min.

DIV6-DIV3				Number of bits sent	
0	0	0	0	Reserved (not to be used)	
0	0	0	1	1	
0	0	1	0	2	
0	0	1	1	3	
0	1	0	0	4	
0	1	0	1	5	
0	1	1	0	6	
0	1	1	1	7	
1	0	0	0	8	
1	0	0	1	9	)
1	0	1	0	10	|
1	0	1	1	11	| Refer to the
1	1	0	0	12	| description of the
1	1	0	1	13	| DIV6-DIV3 bits in
1	1	1	0	14	| the DIV Register
1	1	1	1	15	)

SPI Data/Shift Register (SPIDSR)

Address: E0h — Read/Write

Reset status: XXh

7							0
D7	D6	D5	D4	D3	D2	D1	D0

SPIDSR is read/write, however write access is not allowed if the SPRUN bit of Mode Control register is set to one.

Data is sampled into SPDSR on the SCK edge determined by the CPOL and CPHA bits. The affect of these setting is shown in the following diagrams.

The Shift Register transmits and receives the Most Significant Bit first.

Bit 7-0 = **DSR7-DSR0**: *Data Bits.* These are the SPI shift register data bits.

Miscellaneous Register (MISCR)

Address: DDh — Write only

Reset status: xxxxxxxb

7							0
-	-	-	-	-	-	-	D0

Bit 7-1 = **D7-D1**: *Reserved.*

Bit 0 = **D0**: *Bit 0.* This bit, when set, selects the Sout pin as the SPI output line. When this bit is cleared, Sout acts as a standard I/O line.

5 SOFTWARE

5.1 ST6 ARCHITECTURE

The ST6 software has been designed to fully use the hardware in the most efficient way possible while keeping byte usage to a minimum; in short, to provide byte efficient programming capability. The ST6 core has the ability to set or clear any register or RAM location bit of the Data space with a single instruction. Furthermore, the program may branch to a selected address depending on the status of any bit of the Data space. The carry bit is stored with the value of the bit when the SET or RES instruction is processed.

5.2 ADDRESSING MODES

The ST6 core offers nine addressing modes, which are described in the following paragraphs. Three different address spaces are available: Program space, Data space, and Stack space. Program space contains the instructions which are to be executed, plus the data for immediate mode instructions. Data space contains the Accumulator, the X,Y,V and W registers, peripheral and Input/ Output registers, the RAM locations and Data ROM locations (for storage of tables and constants). Stack space contains six 12-bit RAM cells used to stack the return addresses for subroutines and interrupts.

Immediate. In the immediate addressing mode, the operand of the instruction follows the opcode location. As the operand is a ROM byte, the immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

Direct. In the direct addressing mode, the address of the byte which is processed by the instruction is stored in the location which follows the opcode. Direct addressing allows the user to directly address the 256 bytes in Data Space memory with a single two-byte instruction.

Short Direct. The core can address the four RAM registers X,Y,V,W (locations 80h, 81h, 82h, 83h) in the short-direct addressing mode. In this case, the instruction is only one byte and the selection of the location to be processed is contained in the opcode. Short direct addressing is a subset of the direct addressing mode. (Note that 80h and 81h are also indirect registers).

Extended. In the extended addressing mode, the 12-bit address needed to define the instruction is obtained by concatenating the four less significant bits of the opcode with the byte following the opcode. The instructions (JP, CALL) which use the extended addressing mode are able to branch to any address of the 4K bytes Program space.

An extended addressing mode instruction is two-byte long.

Program Counter Relative. The relative addressing mode is only used in conditional branch instructions. The instruction is used to perform a test and, if the condition is true, a branch with a span of -15 to +16 locations around the address of the relative instruction. If the condition is not true, the instruction which follows the relative instruction is executed. The relative addressing mode instruction is one-byte long. The opcode is obtained in adding the three most significant bits which characterize the kind of the test, one bit which determines whether the branch is a forward (when it is 0) or backward (when it is 1) branch and the four less significant bits which give the span of the branch (0h to Fh) which must be added or subtracted to the address of the relative instruction to obtain the address of the branch.

Bit Direct. In the bit direct addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode points to the address of the byte in which the specified bit must be set or cleared. Thus, any bit in the 256 locations of Data space memory can be set or cleared.

Bit Test & Branch. The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit test and branch instruction is three-byte long. The bit identification and the tested condition are included in the opcode byte. The address of the byte to be tested follows immediately the opcode in the Program space. The third byte is the jump displacement, which is in the range of -127 to +128. This displacement can be determined using a label, which is converted by the assembler.

Indirect. In the indirect addressing mode, the byte processed by the register-indirect instruction is at the address pointed by the content of one of the indirect registers, X or Y (80h,81h). The indirect register is selected by the bit 4 of the opcode. A register indirect instruction is one byte long.

Inherent. In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. These instructions are one byte long.

Opcode Map Summary. The following table contains an opcode map for the instructions used by the ST6

LOW / HI	**0** **0000**	**1** **0001**	**2** **0010**	**3** **0011**	**4** **0100**	**5** **0101**	**6** **0110**	**7** **0111**	LOW / HI
0 **0000**	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b0,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 LD a,(x) 1 ind	**0** **0000**
1 **0001**	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b0,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC x 1 sd	2 JRC e 1 prc	4 LDI a,nn 2 imm	**1** **0001**
2 **0010**	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b4,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 CP a,(x) 1 ind	**2** **0010**
3 **0011**	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b4,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,x 1 sd	2 JRC e 1 prc	4 CPI a,nn 2 imm	**3** **0011**
4 **0100**	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b2,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 ADD a,(x) 1 ind	**4** **0100**
5 **0101**	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b2,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC y 1 sd	2 JRC e 1 prc	4 ADDI a,nn 2 imm	**5** **0101**
6 **0110**	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b6,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 INC (x) 1 ind	**6** **0110**
7 **0111**	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b6,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,y 1 sd	2 JRC e 1 prc	#	**7** **0111**
8 **1000**	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b1,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 LD (x),a 1 ind	**8** **1000**
9 **1001**	2 RNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b1,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC v 1 sd	2 JRC e 1 prc	#	**9** **1001**
A **1010**	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b5,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 AND a,(x) 1 ind	**A** **1010**
B **1011**	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b5,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,v 1 sd	2 JRC e 1 prc	4 ANDI a,nn 2 imm	**B** **1011**
C **1100**	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b3,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 SUB a,(x) 1 ind	**C** **1100**
D **1101**	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b3,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC w 1 sd	2 JRC e 1 prc	4 SUBI a,nn 2 imm	**D** **1101**
E **1110**	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b7,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 DEC (x) 1 ind	**E** **1110**
F **1111**	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b7,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,w 1 sd	2 JRC e 1 prc	#	**F** **1111**

Abbreviations for Addressing Modes:

dir	Direct
sd	Short Direct
imm	Immediate
inh	Inherent
ext	Extended
b.d	Bit Direct
bt	Bit Test
pcr	Program Counter Relative
ind	Indirect

Legend:

#	Indicates Illegal Instructions
e	5 Bit Displacement
b	3 Bit Address
rr	1byte dataspace address
nn	1 byte immediate data
abc	12 bit address
ee	8 bit Displacement

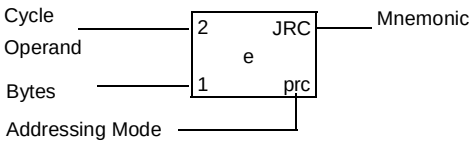
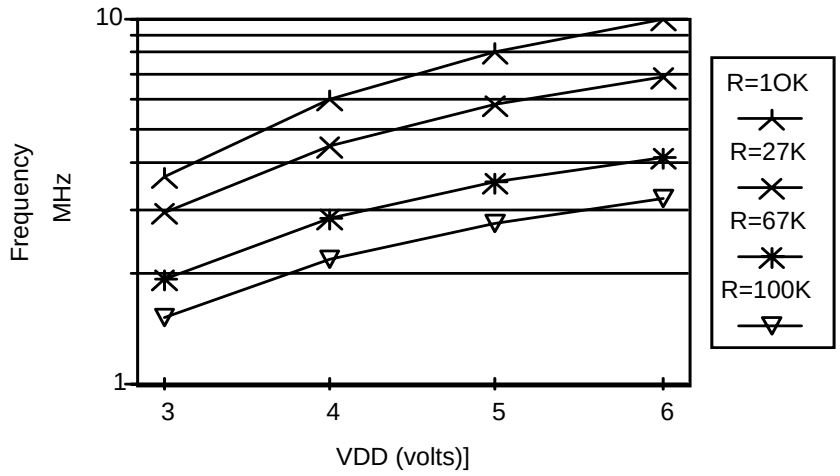
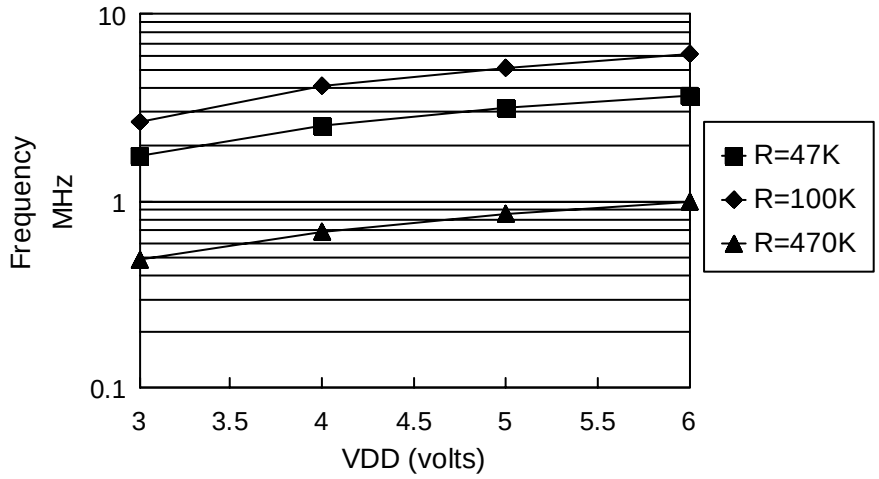


Figure 49. RC frequency versus V_{DD} for ROM ST626xB only



This curves represents typical variations and is given for guidance only

Figure 50. RC frequency versus V_{DD} (Except for ST626xB ROM devices)

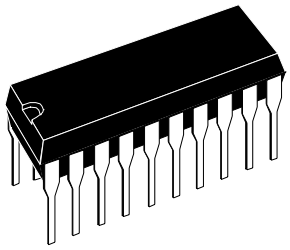


This curves represents typical variations and is given for guidance only

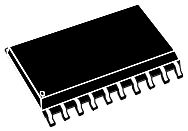
ST6253C/60B/63B

8-BIT ROM MCUs WITH A/D CONVERTER, SAFE RESET, AUTO-RELOAD TIMER, EEPROM AND SPI

- 3.0 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -40 to +125°C Operating Temperature Range
- Run, Wait and Stop Modes
- 5 Interrupt Vectors
- Look-up Table capability in Program Memory
- Data Storage in Program Memory: User selectable size
- Data RAM: 128 bytes
- Data EEPROM: 64/128 bytes (none on ST6253C)
- User Programmable Options
- 13 I/O pins, fully programmable as:
  - Input with pull-up resistor
  - Input without pull-up resistor
  - Input with interrupt generation
  - Open-drain or push-pull output
  - Analog Input
- 6 I/O lines can sink up to 30mA to drive LEDs or TRIACs directly
- 8-bit Timer/Counter with 7-bit programmable prescaler
- 8-bit Auto-reload Timer with 7-bit programmable prescaler (AR Timer)
- Digital Watchdog
- 8-bit A/D Converter with 7 analog inputs
- 8-bit Synchronous Peripheral Interface (SPI)
- On-chip Clock oscillator can be driven by Quartz Crystal Ceramic resonator or RC network
- User configurable Power-on Reset
- One external Non-Maskable Interrupt
- ST626x-EMU2 Emulation and Development System (connects to an MS-DOS PC via a parallel port).



PDIP20



PSO20

(See end of Datasheet for Ordering Information)

DEVICE SUMMARY

DEVICE	ROM (Bytes)	EEPROM	LVD & OSG
ST6253C	1836	-	Yes
ST6260B	3884	128	No
ST6263B	1836	64	No

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1.3 ORDERING INFORMATION

The following section deals with the procedure for transfer of customer codes to STMicroelectronics.

1.3.1 Transfer of Customer Code

Customer code is made up of the ROM contents and the list of the selected mask options. The ROM contents are to be sent on diskette, or by electronic means, with the hexadecimal file generated by the development tool. All unused bytes must be set to FFh.

The selected mask options are communicated to STMicroelectronics using the correctly filled OPTION LIST appended. See page 82.

1.3.2 Listing Generation and Verification

When STMicroelectronics receives the user's ROM contents, a computer listing is generated from it. This listing refers exactly to the mask which will be used to produce the specified MCU. The listing is then returned to the customer who must thoroughly check, complete, sign and return it to STMicroelectronics. The signed listing forms a part of the contractual agreement for the creation of the specific customer mask.

The STMicroelectronics Sales Organization will be pleased to provide detailed information on contractual points.

Table 27. ROM Memory Map for ST6260B

Device Address	Description
0000h-007Fh	Reserved
0080h-0F9Fh	User ROM
0FA0h-0FEFh	Reserved
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved
0FFCh-0FFDh	NMI Interrupt Vector
0FFEh-0FFFh	Reset Vector

Table 28. ROM Memory Map for ST6253C/63B

Device Address	Description
0000h-087Fh	Reserved
0880h-0F9Fh	User ROM
0FA0h-0FEFh	Reserved
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved
0FFCh-0FFDh	NMI Interrupt Vector
0FFEh-0FFFh	Reset Vector

Table 1. ROM Version Ordering Information

Sales Type	ROM (Bytes)	EEPROM (Bytes)	Temperature Range	Package
ST6253CB1/XXX ST6253CB6/XXX ST6253CB3/XXX	1836	-	0 to + 70°C -40 to + 85°C -40 to + 125°C	PDIP20
ST6253CM1/XXX ST6253CM6/XXX ST6253CM3/XXX			0 to + 70°C -40 to + 85°C -40 to + 125°C	PSO20
ST6260BB1/XXX ST6260BB6/XXX ST6260BB3/XXX	3884	128	0 to + 70°C -40 to + 85°C -40 to + 125°C	PDIP20
ST6260BM1/XXX ST6260BM6/XXX ST6260BM3/XXX			0 to + 70°C -40 to + 85°C -40 to + 125°C	PSO20
ST6263BB1/XXX ST6263BB6/XXX ST6263BB3/XXX	1836	64	0 to + 70°C -40 to + 85°C -40 to + 125°C	PDIP20
ST6263BM1/XXX ST6263BM6/XXX ST6263BM3/XXX			0 to + 70°C -40 to + 85°C -40 to + 125°C	PSO20

ST6253C/60B/63B/P53C/P60C/P63C MICROCONTROLLER OPTION LIST

Customer: . . . . . .
Address: . . . . . .
. . . . . .
Contact: . . . . . .
Phone: . . . . . .
Reference: . . . . . .

STMicroelectronics references:

Device: [ ] ST6253C (2 KB) [ ] ST6260B (4 KB) [ ] ST6263B (2 KB)
[ ] ST62P53C (2 KB) [ ] ST62P60C (4 KB) [ ] ST62P63C (2 KB)

Package: [ ] Dual in Line Plastic
[ ] Small Outline Plastic with conditioning

Conditioning option: [ ] Standard (Tube) [ ] Tape & Reel

Temperature Range: [ ] 0°C to + 70°C [ ] - 40°C to + 85°C
[ ] - 40°C to + 125°C

Marking: [ ] Standard marking
[ ] Special marking (ROM only)
PDIP28 (10 char. max): _ _ _ _ _ _ _ _ _ _
PSO28 (8 char. max): _ _ _ _ _ _ _ _
SSOP28 (11 char. max): _ _ _ _ _ _ _ _ _ _ _
Authorized characters are letters, digits, '.', '-', '/' and spaces only.

Oscillator Safeguard*: [ ] Enabled [ ] Disabled

Oscillator Selection: [ ] Quartz crystal / Ceramic resonator
[ ] RC network

Reset Delay: [ ] 32768 cycle delay [ ] 2048 cycle delay

Watchdog Selection: [ ] Software Activation [ ] Hardware Activation

PB1:PB0 Pull-Up at RESET*: [ ] Enabled [ ] Disabled

PB3:PB2 Pull-Up at RESET*: [ ] Enabled [ ] Disabled

External STOP Mode Control: [ ] Enabled [ ] Disabled

Readout Protection: FASTROM:
[ ] Enabled [ ] Disabled
ROM:
[ ] Enabled:
[ ] Fuse is blown by STMicroelectronics
[ ] Fuse can be blown by the customer
[ ] Disabled

Low Voltage Detector*: [ ] Enabled [ ] Disabled

NMI pull-up*: [ ] Enabled [ ] Disabled

ADC Synchro*: [ ] Enabled [ ] Disabled

*except on ST6260B/63B

Comments:

Oscillator Frequency in the application: . . . . . .
Supply Operating Range in the application: . . . . . .
Notes: . . . . . .
Date: . . . . . .
Signature: . . . . . .