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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	53
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 8x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg232f16-qfp64t

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3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on $T_{AMB}=25^{\circ}C$ and $V_{DD}=3.0$ V, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 9) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 9).

Symbol	Parameter	Condition	Min	Тур	Max	Unit
T _{STG}	Storage tempera- ture range		-40		150 ¹	°C
T _S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	°C
V _{DDMAX}	External main sup- ply voltage		0		3.8	V
VIOPIN	Voltage on any I/O pin		-0.3		V _{DD} +0.3	V

Table 3.1. Absolute Maximum Ratings

¹Based on programmed devices tested for 10000 hours at 150°C. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Тур	Мах	Unit
T _{AMB}	Ambient temperature range	-40		85	°C
V _{DDOP}	Operating supply voltage	1.98		3.8	V
f _{APB}	Internal APB clock frequency			32	MHz
f _{AHB}	Internal AHB clock frequency			32	MHz

Figure 3.1. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.





Figure 3.2. EM3 current consumption.



Figure 3.3. EM4 current consumption.







3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 3.4. Energy Modes Transitions

Symbol	Parameter	Min	Тур	Max	Unit
t _{EM10}	Transition time from EM1 to EM0		0		HF- CORE- CLK cycles
t _{EM20}	Transition time from EM2 to EM0		2		μs
t _{EM30}	Transition time from EM3 to EM0		2		μs
t _{EM40}	Transition time from EM4 to EM0		163		μs

3.6 Power Management

The EFM32TG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 3.5. Power Management

Symbol	Parameter	Condition	Min	Тур	Max	Unit
V _{BODextthr} -	BOD threshold on falling external supply voltage		1.74		1.96	V
V _{BODextthr+}	BOD threshold on rising external sup- ply voltage			1.85	1.98	V
V _{PORthr+}	Power-on Reset (POR) threshold on rising external sup- ply voltage				1.98	V
t _{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μs
C _{DECOUPLE}	Voltage regulator decoupling capaci- tor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μF



Symbol	Parameter	Condition	Min	Тур	Max	Unit
		Sourcing 20 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.80V _{DD}			V
		Sinking 0.1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.20V _{DD}		V
		Sinking 0.1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.10V _{DD}		V
		Sinking 1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.10V _{DD}		V
Vice	Output low voltage (Production test	Sinking 1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.05V _{DD}		V
VIOOL	DRIVEMODE = STANDARD)	Sinking 6 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.30V _{DD}	V
		Sinking 6 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.20V _{DD}	V
		Sinking 20 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.35V _{DD}	V
		Sinking 20 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.20V _{DD}	V
I _{IOLEAK}	Input leakage cur- rent	High Impedance IO connected to GROUND or V_{DD}		±0.1	±100	nA
R _{PU}	I/O pin pull-up resis- tor			40		kOhm
R _{PD}	I/O pin pull-down re- sistor			40		kOhm
R _{IOESD}	Internal ESD series resistor			200		Ohm
t _{IOGLITCH}	Pulse width of puls- es to be removed by the glitch sup- pression filter		10		50	ns
tioos	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capaci- tance C_L =12.5-25pF.	20+0.1C _L		250	ns
tioof	Output fall time		20+0.1C _L		250	ns
V _{IOHYST}	I/O pin hysteresis (V _{IOTHR+} - V _{IOTHR-})	V _{DD} = 1.98 - 3.8 V	0.1V _{DD}			V

3.9 Oscillators

3.9.1 LFXO

Table 3.8. LFXO

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
f _{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR _{LFXO}	Supported crystal equivalent series re- sistance (ESR)			30	120	kOhm
C _{LFXOL}	Supported crystal external load range		X ¹		25	pF
I _{LFXO}	Current consump- tion for core and buffer after startup.	ESR=30 kOhm, C _L =10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t _{LFXO}	Start- up time.	ESR=30 kOhm, C _L =10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

¹See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio

For safe startup of a given crystal, the energyAware Designer in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

3.9.2 HFXO

Table 3.9. HFXO

Symbol	Parameter	Condition	Min	Тур	Max	Unit
f _{HFXO}	Supported nominal crystal Frequency		4		32	MHz
	Supported crystal	Crystal frequency 32 MHz		30	60	Ohm
ESR _{HFXO}	sistance (ESR)	Crystal frequency 4 MHz		400	1500	Ohm
9 _{mHFXO}	The transconduc- tance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C _{HFXOL}	Supported crystal external load range		5		25	pF
	Current consump- tion for HFXO after startup	4 MHz: ESR=400 Ohm, C _L =20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		μA
IHFXO		32 MHz: ESR=30 Ohm, C _L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		μA
t _{HFXO}	Startup time	32 MHz: ESR=30 Ohm, C _L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		μs



Symbol	Parameter	Condition	Min	Тур	Мах	Unit
		f _{HFRCO} = 14 MHz		104	120	μA
		f _{HFRCO} = 11 MHz		94	110	μA
		f _{HFRCO} = 6.6 MHz		63	90	μA
		f _{HFRCO} = 1.2 MHz		22	32	μA
TUNESTEP _{H-} FRCO	Frequency step for LSB change in TUNING value			0.3 ³		%

¹For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

 2 For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

³The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

Figure 3.11. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature



Figure 3.12. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature





3.10 Analog Digital Converter (ADC)

Table 3.14. ADC

Symbol	Parameter	Condition	Min	Тур	Max	Unit
		Single ended	0		V _{REF}	V
	Input voltage range	Differential	-V _{REF} /2		V _{REF} /2	V
V _{ADCREFIN}	Input range of exter- nal reference volt- age, single ended and differential		1.25		V _{DD}	V
V _{ADCREFIN_CH7}	Input range of ex- ternal negative ref- erence voltage on channel 7	See V _{ADCREFIN}	0		V _{DD} - 1.1	V
VADCREFIN_CH6	Input range of ex- ternal positive ref- erence voltage on channel 6	See V _{ADCREFIN}	0.625		V _{DD}	V
	Common mode in- put range		0		V _{DD}	V
	Input current	2pF sampling capacitors		<100		nA
CMRR _{ADC}	Analog input com- mon mode rejection ratio			65		dB
	Average active cur- rent	1 MSamples/s, 12 bit, external reference		377		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP- MODE in ADCn_CTRL set to 0b00		67		μA
I _{ADC}		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP- MODE in ADCn_CTRL set to 0b01		68		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP- MODE in ADCn_CTRL set to 0b10		71		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP- MODE in ADCn_CTRL set to 0b11		244		μA
I _{ADCREF}	Current consump- tion of internal volt- age reference	Internal voltage reference		65		μA
C _{ADCIN}	Input capacitance			2		pF
R _{ADCIN}	Input ON resistance		1			MOhm
R _{ADCFILT}	Input RC filter resis- tance			10		kOhm
CADCFILT	Input RC filter/de- coupling capaci- tance			250		fF



Symbol	Parameter	Condition	Min	Тур	Max	Unit
		200 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differ- ential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference		69		dB
		200 kSamples/s, 12 bit, differ- ential, 2xV _{DD} reference		70		dB
		1 MSamples/s, 12 bit, single ended, internal 1.25V refer- ence		58		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V _{DD} reference		64		dB
		1 MSamples/s, 12 bit, differen- tial, internal 1.25V reference		60		dB
	SIgnal-to-Noise And Distortion-ratio (SINAD)	1 MSamples/s, 12 bit, differen- tial, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differen- tial, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
SINADura		1 MSamples/s, 12 bit, differen- tial, 2xV _{DD} reference		68		dB
GINADADC		200 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V _{DD} reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differ- ential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, V _{DD} reference	62	68		dB
		200 kSamples/s, 12 bit, differ- ential, 2xV _{DD} reference		69		dB
SFDRADC	Spurious-Free Dy- namic Range (SF-	1 MSamples/s, 12 bit, single ended, internal 1.25V refer- ence		64		dBc
ST DIVADC	DR)	1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc

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at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

²Typical numbers given by abs(Mean) / (85 - 25).

³Max number given by (abs(Mean) + 3x stddev) / (85 - 25).

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.17 (p. 30) and Figure 3.18 (p. 30), respectively.

Figure 3.17. Integral Non-Linearity (INL)



Figure 3.18. Differential Non-Linearity (DNL)





Symbol	Parameter	Condition	Min	Тур	Max	Unit
		Continuous Mode			1000	kHz
f _{DAC}	DAC clock frequen-	Sample/Hold Mode			250	kHz
		Sample/Off Mode			250	kHz
CYC _{DACCONV}	Clock cyckles per conversion			2		
t _{DACCONV}	Conversion time		2			μs
t _{DACSETTLE}	Settling time			5		μs
SNR _{DAC}	Signal to Noise Ra-	500 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		58		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		59		dB
SNDR _{DAC}	Signal to Noise- pulse Distortion Ra- tio (SNDR)	500 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		57		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		54		dB
SFDR _{DAC}	Spurious-Free Dynamic	500 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		62		dBc
	Range(SFDR)	500 kSamples/s, 12 bit, single ended, internal 2.5V reference		56		dBc
VDACOFFSET	Offset voltage	After calibration, single ended		2		mV
DNL _{DAC}	Differential non-lin- earity	V_{DD} = 3.0 V, V_{DD} reference		±1		LSB
INL _{DAC}	Integral non-lineari- ty	V_{DD} = 3.0 V, V_{DD} reference		±5		LSB
MC _{DAC}	No missing codes			12		bits

3.12 Operational Amplifier (OPAMP)

The electrical characteristics for the Operational Amplifiers are based on simulations.

Table 3.16. OPAMP

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
I _{OPAMP}		OPA2 BIASPROG=0xF, HALFBIAS=0x0, Unity Gain		350	405	μA
	Active Current	OPA2 BIASPROG=0x7, HALFBIAS=0x1, Unity Gain		95	115	μA
		OPA2 BIASPROG=0x0, HALFBIAS=0x1, Unity Gain		13	17	μA
G _{OL}	Open Loop Gain	OPA2 BIASPROG=0xF, HALFBIAS=0x0		101		dB
		OPA2 BIASPROG=0x7, HALFBIAS=0x1		98		dB
		OPA2 BIASPROG=0x0, HALFBIAS=0x1		91		dB



Figure 3.28. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)



4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32TG232.

4.1 Pinout

The *EFM32TG232* pinout is shown in Figure 4.1 (p. 45) and Table 4.1 (p. 45). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32TG232 Pinout (top view, not to scale)



Table 4.1. Device Pinout

	QFP64 Pin# and Name	Pin Alternate Functionality / Description						
Pin #	Pin Name	Analog	Timers	Communication	Other			
1	PA0		TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0			
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0			

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Alternate			L	OCATIO.	N			
Functionality	0	1	2	3	4	5	6	Description
ACMP1_O	PF2		PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX.
BOOT_TX	PE10							Bootloader TX.
CMU_CLK0	PA2	PC12	PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
DAC0_N0 / OPAMP_N0	PC5							Operational Amplifier 0 external negative input.
DAC0_N1 / OPAMP_N1	PD7							Operational Amplifier 1 external negative input.
OPAMP_N2	PD3							Operational Amplifier 2 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 / OPAMP output channel number 0.
DAC0_OUT0ALT / OPAMP_OUT0ALT	PC0	PC1	PC2	PC3	PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1ALT / OPAMP_OUT1ALT	PC12	PC13	PC14	PC15	PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.
DAC0_P0 / OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
DAC0_P1 / OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
								Debug-interface Serial Wire clock input.
DBG_SWCLK	PF0	PF0						Note that this function is enabled to pin out of reset, and has a built-in pull down.
								Debug-interface Serial Wire data input / output.
DBG_SWDIO	PF1	PF1						Note that this function is enabled to pin out of reset, and has a built-in pull up.
								Debug-interface Serial Wire viewer Output.
DBG_SWO	PF2	PC15						Note that this function is not enabled after reset, and must be enabled by software to be used.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.

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Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
I2C0_SCL	PA1	PD7	PC7		PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6		PC0	PF0	PE12	I2C0 Serial Data input / output.
LES_ALTEX0	PD6							LESENSE alternate exite output 0.
LES_ALTEX1	PD7							LESENSE alternate exite output 1.
LES_ALTEX2	PA3							LESENSE alternate exite output 2.
LES_ALTEX3	PA4							LESENSE alternate exite output 3.
LES_ALTEX4	PA5							LESENSE alternate exite output 4.
LES_ALTEX5	PE11							LESENSE alternate exite output 5.
LES_ALTEX6	PE12							LESENSE alternate exite output 6.
LES_ALTEX7	PE13							LESENSE alternate exite output 7.
LES_CH0	PC0							LESENSE channel 0.
LES_CH1	PC1							LESENSE channel 1.
LES_CH2	PC2							LESENSE channel 2.
LES_CH3	PC3							LESENSE channel 3.
LES_CH4	PC4							LESENSE channel 4.
LES_CH5	PC5							LESENSE channel 5.
LES_CH6	PC6							LESENSE channel 6.
LES_CH7	PC7							LESENSE channel 7.
LES_CH8	PC8							LESENSE channel 8.
LES_CH9	PC9							LESENSE channel 9.
LES_CH10	PC10							LESENSE channel 10.
LES_CH11	PC11							LESENSE channel 11.
LES_CH12	PC12							LESENSE channel 12.
LES_CH13	PC13							LESENSE channel 13.
LES_CH14	PC14							LESENSE channel 14.
LES_CH15	PC15							LESENSE channel 15.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7		PF1	PC5				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15	PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13		PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1	PD7				Pulse Counter PCNT0 input number 1.
PRS_CH0	PA0	PF3						Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4						Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1	PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0		PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1		PD2	PC0	PF1		Timer 0 Capture Compare input / output channel 1.



Figure 4.2. Opamp Pinout



4.5 TQFP64 Package





Note:

- 1. All dimensions & tolerancing confirm to ASME Y14.5M-1994.
- 2. The top package body size may be smaller than the bottom package body size.
- 3. Datum 'A,B', and 'B' to be determined at datum plane 'H'.



Figure 5.2. TQFP64 PCB Solder Mask



Table 5.2. QFP64 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
а	1.72
b	0.42
С	0.50
d	11.50
е	11.50

7 Revision History

7.1 Revision 1.40

March 6th, 2015

Updated Block Diagram.

Updated Energy Modes current consumption.

Updated Power Management section.

Updated LFRCO and HFRCO sections.

Added AUXHFRCO to block diagram and Electrical Characteristics.

Corrected unit to kHz on LFRCO plots y-axis.

Updated ADC section and added clarification on conditions for INL_{ADC} and DNL_{ADC} parameters.

Updated DAC section and added clarification on conditions for INL_{DAC} and DNL_{DAC} parameters.

Updated OPAMP section.

Updated ACMP section and the response time graph.

Updated VCMP section.

Updated Digital Peripherals section.

7.2 Revision 1.30

July 2nd, 2014 Corrected single power supply voltage minimum value from 1.85V to 1.98V. Updated current consumption.

Updated transition between energy modes.

Updated power management data.

Updated GPIO data.

Updated LFXO, HFXO, HFRCO and ULFRCO data.

Updated LFRCO and HFRCO plots.

Updated ACMP data.

7.3 Revision 1.21

November 21st, 2013

Updated figures.

Updated errata-link.

Updated chip marking.

Added rising POR level and corrected Thermometer output gradient in Electrical Characteristics section.

Updated Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup.

Added Gain error drift and Offset error drift to ADC table.

Added reference to errata document.

7.9 Revision 0.92

July 22nd, 2011

Updated current consumption numbers from latest device characterization data.

Updated OPAMP electrical characteristics.

Made ADC plots render properly in Adobe Reader.

Corrected number of DAC channels available.

7.10 Revision 0.90

June 30th, 2011

Initial preliminary release.

A Disclaimer and Trademarks

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