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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	AC'97, Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj128gp202t-i-mm">https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj128gp202t-i-mm</a>

NOTES:

4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-2).

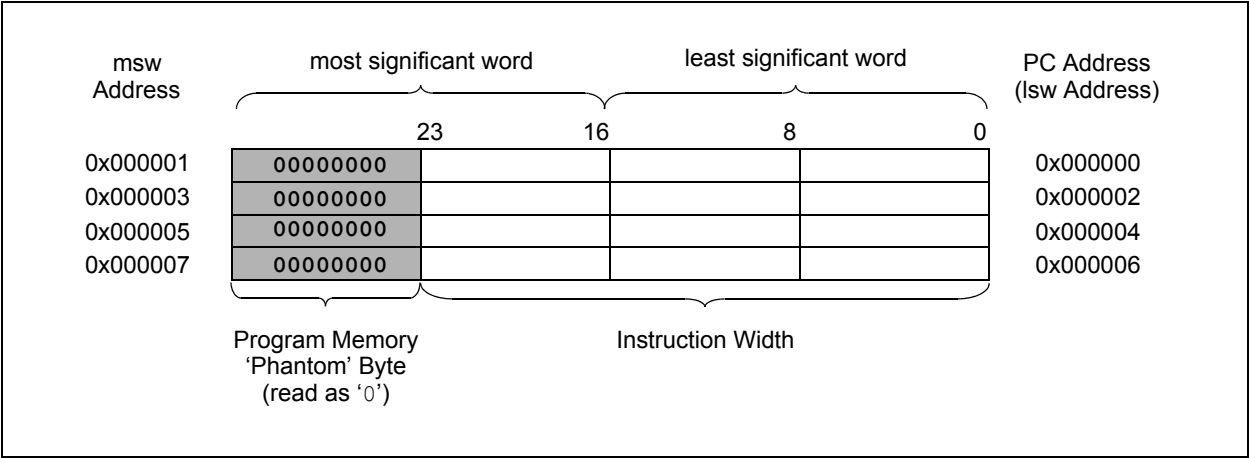
Program memory addresses are always word-aligned on the lower word, and addresses are incremented or decremented by two during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

4.1.2 INTERRUPT AND TRAP VECTORS

All dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 devices reserve the addresses between 0x00000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at 0x000000, with the actual address for the start of code at 0x000002.

dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 devices also have two interrupt vector tables, located from 0x000004 to 0x0000FF and 0x000100 to 0x0001FF. These vector tables allow each of the device interrupt sources to be handled by separate Interrupt Service Routines (ISRs). A more detailed discussion of the interrupt vector tables is provided in Section 7.1 “Interrupt Vector Table”.

FIGURE 4-2: PROGRAM MEMORY ORGANIZATION



**TABLE 4-5: TIMER REGISTER MAP**

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100	Timer1 Register																0000
PR1	0102	Period Register 1																FFFF
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	—	TSYNC	TCS	—	0000	
TMR2	0106	Timer2 Register																0000
TMR3HLD	0108	Timer3 Holding Register (for 32-bit timer operations only)																xxxx
TMR3	010A	Timer3 Register																0000
PR2	010C	Period Register 2																FFFF
PR3	010E	Period Register 3																FFFF
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	T32	—	TCS	—	0000	
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	—	—	TCS	—	0000	
TMR4	0114	Timer4 Register																0000
TMR5HLD	0116	Timer5 Holding Register (for 32-bit timer operations only)																xxxx
TMR5	0118	Timer5 Register																0000
PR4	011A	Period Register 4																FFFF
PR5	011C	Period Register 5																FFFF
T4CON	011E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	T32	—	TCS	—	0000	
T5CON	0120	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	—	—	TCS	—	0000	

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-6: INPUT CAPTURE REGISTER MAP**

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IC1BUF	0140	Input 1 Capture Register																xxxx
IC1CON	0142	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>		0000		
IC2BUF	0144	Input 2 Capture Register																xxxx
IC2CON	0146	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>		0000		
IC7BUF	0158	Input 7 Capture Register																xxxx
IC7CON	015A	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>		0000		
IC8BUF	015C	Input 8Capture Register																xxxx
IC8CON	015E	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>		0000		

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-16: DMA REGISTER MAP (CONTINUED)**

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DMA5PAD	03C4	PAD<15:0>																0000
DMA5CNT	03C6	—	—	—	—	—	—	CNT<9:0>										0000
DMA6CON	03C8	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000
DMA6REQ	03CA	FORCE	—	—	—	—	—	—	—	—	IRQSEL<6:0>							0000
DMA6STA	03CC	STA<15:0>																0000
DMA6STB	03CE	STB<15:0>																0000
DMA6PAD	03D0	PAD<15:0>																0000
DMA6CNT	03D2	—	—	—	—	—	—	CNT<9:0>										0000
DMA7CON	03D4	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000
DMA7REQ	03D6	FORCE	—	—	—	—	—	—	—	—	IRQSEL<6:0>							0000
DMA7STA	03D8	STA<15:0>																0000
DMA7STB	03DA	STB<15:0>																0000
DMA7PAD	03DC	PAD<15:0>																0000
DMA7CNT	03DE	—	—	—	—	—	—	CNT<9:0>										0000
DMACS0	03E0	PWCOL7	PWCOL6	PWCOL5	PWCOL4	PWCOL3	PWCOL2	PWCOL1	PWCOL0	XWCOL7	XWCOL6	XWCOL5	XWCOL4	XWCOL3	XWCOL2	XWCOL1	XWCOL0	0000
DMACS1	03E2	—	—	—	—	LSTCH<3:0>				PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0	0000
DSADR	03E4	DSADR<15:0>																0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**REGISTER 7-10: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0 (CONTINUED)**

- bit 2      **OC1IE:** Output Compare Channel 1 Interrupt Enable bit  
            1 = Interrupt request enabled  
            0 = Interrupt request not enabled
- bit 1      **IC1IE:** Input Capture Channel 1 Interrupt Enable bit  
            1 = Interrupt request enabled  
            0 = Interrupt request not enabled
- bit 0      **INT0IE:** External Interrupt 0 Flag Status bit  
            1 = Interrupt request enabled  
            0 = Interrupt request not enabled

**REGISTER 7-31: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER**

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	ILR<3:0>			
bit 15				bit 8			

U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	VECNUM<6:0>						
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **ILR<3:0>:** New CPU Interrupt Priority Level bits

1111 = CPU Interrupt Priority Level is 15

•  
•  
•

0001 = CPU Interrupt Priority Level is 1

0000 = CPU Interrupt Priority Level is 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **VECNUM<6:0>:** Vector Number of Pending Interrupt bits

0111111 = Interrupt Vector pending is number 135

•  
•  
•

0000001 = Interrupt Vector pending is number 9

0000000 = Interrupt Vector pending is number 8

**REGISTER 11-17: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0**

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP1R<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP0R<4:0>				
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'bit 12-8 **RP1R<4:0>:** Peripheral Output Function is Assigned to RP1 Output Pin bits (see [Table 11-2](#) for peripheral function numbers)bit 7-5 **Unimplemented:** Read as '0'bit 4-0 **RP0R<4:0>:** Peripheral Output Function is Assigned to RP0 Output Pin bits (see [Table 11-2](#) for peripheral function numbers)**REGISTER 11-18: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1**

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP3R<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP2R<4:0>				
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'bit 12-8 **RP3R<4:0>:** Peripheral Output Function is Assigned to RP3 Output Pin bits (see [Table 11-2](#) for peripheral function numbers)bit 7-5 **Unimplemented:** Read as '0'bit 4-0 **RP2R<4:0>:** Peripheral Output Function is Assigned to RP2 Output Pin bits (see [Table 11-2](#) for peripheral function numbers)



### 15.3 Output Compare Control Register

**REGISTER 15-1: OCxCON: OUTPUT COMPARE x CONTROL REGISTER (x = 1, 2, 3 OR 4)**

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	OCSIDL	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R-0 HC	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	OCFLT	OCTSEL	OCM<2:0>		
bit 7							bit 0

<b>Legend:</b>	HC = Cleared in Hardware	HS = Set in Hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

- bit 15-14      **Unimplemented:** Read as '0'
- bit 13      **OCSIDL:** Stop Output Compare in Idle Mode Control bit  
             1 = Output Compare x halts in CPU Idle mode  
             0 = Output Compare x continues to operate in CPU Idle mode
- bit 12-5      **Unimplemented:** Read as '0'
- bit 4      **OCFLT:** PWM Fault Condition Status bit  
             1 = PWM Fault condition has occurred (cleared in hardware only)  
             0 = No PWM Fault condition has occurred  
             (This bit is only used when OCM<2:0> = 111.)
- bit 3      **OCTSEL:** Output Compare Timer Select bit  
             1 = Timer3 is the clock source for Compare x  
             0 = Timer2 is the clock source for Compare x
- bit 2-0      **OCM<2:0>:** Output Compare Mode Select bits  
             111 = PWM mode on OCx, Fault pin enabled  
             110 = PWM mode on OCx, Fault pin disabled  
             101 = Initialize OCx pin low, generate continuous output pulses on OCx pin  
             100 = Initialize OCx pin low, generate single output pulse on OCx pin  
             011 = Compare event toggles OCx pin  
             010 = Initialize OCx pin high, compare event forces OCx pin low  
             001 = Initialize OCx pin low, compare event forces OCx pin high  
             000 = Output compare channel is disabled

## 16.0 SERIAL PERIPHERAL INTERFACE (SPI)

**Note 1:** This data sheet summarizes the features of the dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 18. “Serial Peripheral Interface (SPI)”** (DS70206) of the “dsPIC33F/PIC24H Family Reference Manual”, which is available from the Microchip website ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Serial Peripheral Interface (SPI) module is a synchronous serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, analog-to-digital converters, etc. The SPI module is compatible with Motorola® SPI and SIOP.

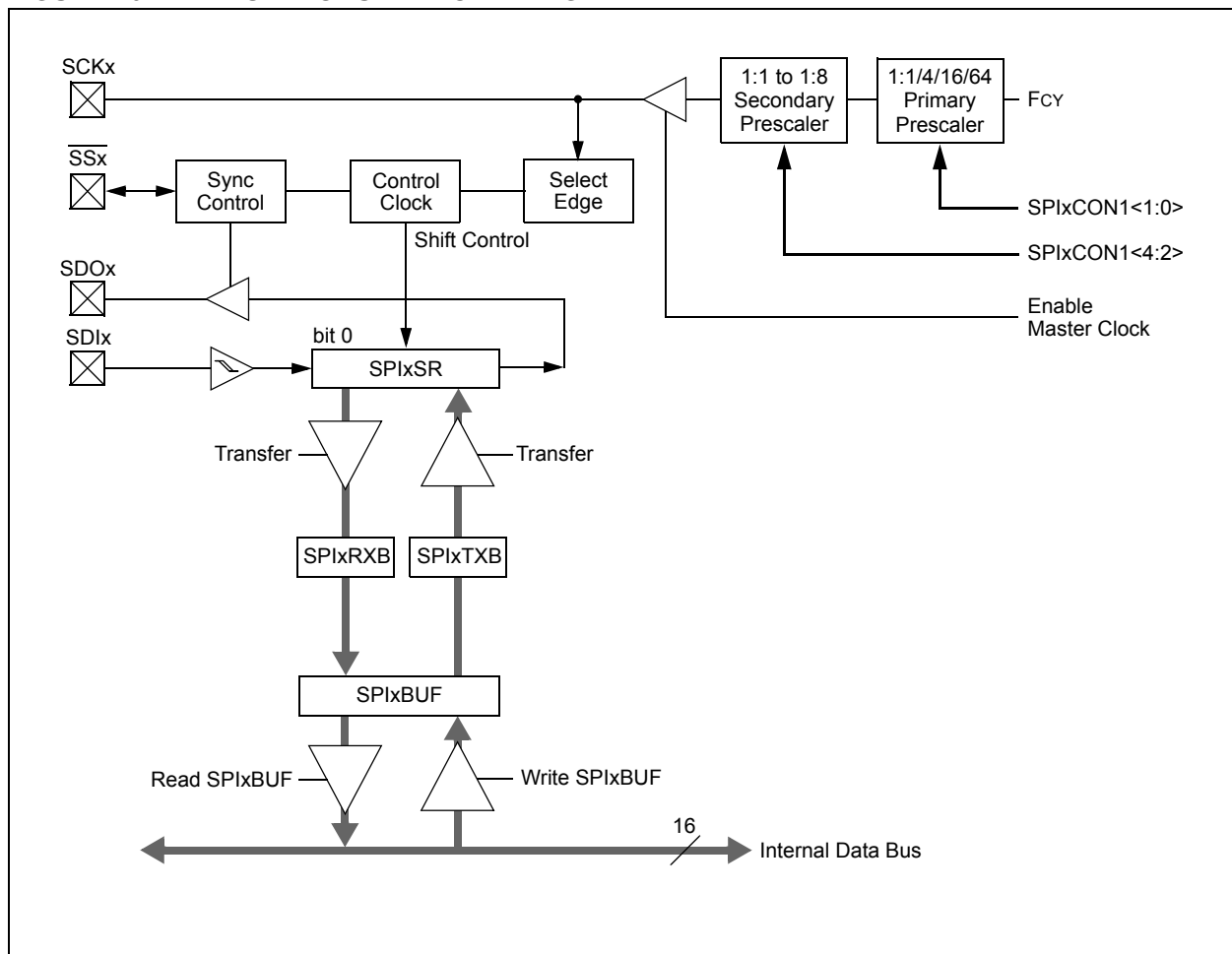
Each SPI module consists of a 16-bit shift register, SPIxSR (where x = 1 or 2), used for shifting data in and out, and a buffer register, SPIxBUF. A control register, SPIxCON, configures the module. Additionally, a status register, SPIxSTAT, indicates status conditions.

The serial interface consists of 4 pins:

- SDIx (serial data input)
- SDOx (serial data output)
- SCKx (shift clock input or output)
- SSx (active-low slave select).

In Master mode operation, SCK is a clock output. In Slave mode, it is a clock input.

**FIGURE 16-1: SPI MODULE BLOCK DIAGRAM**



**REGISTER 16-3: SPIxCON2: SPIx CONTROL REGISTER 2**

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
FRMEN	SPIFSD	FRMPOL	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	FRMDLY	—
bit 7						bit 0	

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15      **FRMEN:** Framed SPIx Support bit  
                  1 = Framed SPIx support enabled ( $\overline{SSx}$  pin used as frame sync pulse input/output)  
                  0 = Framed SPIx support disabled
- bit 14      **SPIFSD:** Frame Sync Pulse Direction Control bit  
                  1 = Frame sync pulse input (slave)  
                  0 = Frame sync pulse output (master)
- bit 13      **FRMPOL:** Frame Sync Pulse Polarity bit  
                  1 = Frame sync pulse is active-high  
                  0 = Frame sync pulse is active-low
- bit 12-2    **Unimplemented:** Read as '0'
- bit 1      **FRMDLY:** Frame Sync Pulse Edge Select bit  
                  1 = Frame sync pulse coincides with first bit clock  
                  0 = Frame sync pulse precedes first bit clock
- bit 0      **Unimplemented:** Read as '0'  
                  This bit must not be set to '1' by the user application.

**REGISTER 17-1: I2CxCON: I2Cx CONTROL REGISTER**

R/W-0	U-0	R/W-0	R/W-1 HC	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0 HC	R/W-0 HC	R/W-0 HC	R/W-0 HC	R/W-0 HC
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7						bit 0	

<b>Legend:</b>	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HS = Set in hardware	HC = Cleared in hardware
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15      **I2CEN:** I2Cx Enable bit  
1 = Enables the I2Cx module and configures the SDAx and SCLx pins as serial port pins  
0 = Disables the I2Cx module. All I<sup>2</sup>C™ pins are controlled by port functions
- bit 14      **Unimplemented:** Read as '0'
- bit 13      **I2CSIDL:** Stop in Idle Mode bit  
1 = Discontinue module operation when device enters an Idle mode  
0 = Continue module operation in Idle mode
- bit 12      **SCLREL:** SCLx Release Control bit (when operating as I<sup>2</sup>C slave)  
1 = Release SCLx clock  
0 = Hold SCLx clock low (clock stretch)  
If STREN = 1:  
Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.  
If STREN = 0:  
Bit is R/S (i.e., software can only write '1' to release clock). Hardware clear at beginning of slave transmission.
- bit 11      **IPMIEN:** Intelligent Peripheral Management Interface (IPMI) Enable bit  
1 = IPMI mode is enabled; all addresses Acknowledged  
0 = IPMI mode disabled
- bit 10      **A10M:** 10-bit Slave Address bit  
1 = I2CxADD is a 10-bit slave address  
0 = I2CxADD is a 7-bit slave address
- bit 9        **DISSLW:** Disable Slew Rate Control bit  
1 = Slew rate control disabled  
0 = Slew rate control enabled
- bit 8        **SMEN:** SMBus Input Levels bit  
1 = Enable I/O pin thresholds compliant with SMBus specification  
0 = Disable SMBus input thresholds
- bit 7        **GCEN:** General Call Enable bit (when operating as I<sup>2</sup>C slave)  
1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)  
0 = General call address disabled
- bit 6        **STREN:** SCLx Clock Stretch Enable bit (when operating as I<sup>2</sup>C slave)  
Used in conjunction with SCLREL bit.  
1 = Enable software or receive clock stretching  
0 = Disable software or receive clock stretching

**REGISTER 17-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)**

bit 3	<p><b>S:</b> Start bit</p> <p>1 = Indicates that a Start (or Repeated Start) bit has been detected last</p> <p>0 = Start bit was not detected last</p> <p>Hardware set or clear when Start, Repeated Start or Stop detected.</p>
bit 2	<p><b>R_W:</b> Read/Write Information bit (when operating as I<sup>2</sup>C slave)</p> <p>1 = Read – indicates data transfer is output from slave</p> <p>0 = Write – indicates data transfer is input to slave</p> <p>Hardware set or clear after reception of I<sup>2</sup>C device address byte.</p>
bit 1	<p><b>RBF:</b> Receive Buffer Full Status bit</p> <p>1 = Receive complete, I2CxRCV is full</p> <p>0 = Receive not complete, I2CxRCV is empty</p> <p>Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.</p>
bit 0	<p><b>TBF:</b> Transmit Buffer Full Status bit</p> <p>1 = Transmit in progress, I2CxTRN is full</p> <p>0 = Transmit complete, I2CxTRN is empty</p> <p>Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.</p>

## 18.1 UART Helpful Tips

1. In multi-node direct-connect UART networks, UART receive inputs react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the idle state, the default of which is logic high, (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a start bit detection and will cause the first byte received after the device has been initialized to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
  - a) If URXINV = 0, use a pull-up resistor on the RX pin.
  - b) If URXINV = 1, use a pull-down resistor on the RX pin.
2. The first character received on a wake-up from Sleep mode caused by activity on the UxRX pin of the UART module will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock relative to the incoming UxRX bit timing is no longer synchronized, resulting in the first character being invalid. This is to be expected.

## 18.2 UART Resources

Many useful resources related to UART are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this [link](http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en532311), contains the latest updates and additional information.

<b>Note:</b> In the event you are not able to access the product page using the link above, enter this URL in your browser: <a href="http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en532311">http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en532311</a>
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### 18.2.1 KEY RESOURCES

- **Section 17. “UART”** (DS70188)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

**REGISTER 19-7: CIINTE: ECAN™ INTERRUPT ENABLE REGISTER**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE
bit 7							bit 0

**Legend:**

C = Writable bit, but only '0' can be written to clear the bit  
R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
-n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

- bit 15-8      **Unimplemented:** Read as '0'
- bit 7      **IVRIE:** Invalid Message Received Interrupt Enable bit  
1 = Interrupt Request Enabled  
0 = Interrupt Request not enabled
- bit 6      **WAKIE:** Bus Wake-up Activity Interrupt Flag bit  
1 = Interrupt Request Enabled  
0 = Interrupt Request not enabled
- bit 5      **ERRIE:** Error Interrupt Enable bit  
1 = Interrupt Request Enabled  
0 = Interrupt Request not enabled
- bit 4      **Unimplemented:** Read as '0'
- bit 3      **FIFOIE:** FIFO Almost Full Interrupt Enable bit  
1 = Interrupt Request Enabled  
0 = Interrupt Request not enabled
- bit 2      **RBOVIE:** RX Buffer Overflow Interrupt Enable bit  
1 = Interrupt Request Enabled  
0 = Interrupt Request not enabled
- bit 1      **RBIE:** RX Buffer Interrupt Enable bit  
1 = Interrupt Request Enabled  
0 = Interrupt Request not enabled
- bit 0      **TBIE:** TX Buffer Interrupt Enable bit  
1 = Interrupt Request Enabled  
0 = Interrupt Request not enabled

## **22.5 DAC Resources**

Many useful resources related to DAC are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this [link](http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en532311), contains the latest updates and additional information.

<p><b>Note:</b> In the event you are not able to access the product page using the link above, enter this URL in your browser: <a href="http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en532311">http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en532311</a></p>
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### **22.5.1 KEY RESOURCES**

- **Section 33. “Audio Digital-to-Analog Converter (DAC)” (DS70211)**
- Code Samples
- Application Notes
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- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools



## 26.2 PMP Control Registers

**REGISTER 26-1: PMCON: PARALLEL MASTER PORT CONTROL REGISTER**

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PMPEN	—	PSIDL	ADMUX1	ADMUX0	PTBEEN	PTWREN	PTRDEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0 <sup>(1)</sup>	U-0	R/W-0 <sup>(1)</sup>	R/W-0	R/W-0	R/W-0
CSF1	CSF0	ALP	—	CS1P	BEP	WRSP	RDSP
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **PMPEN:** Parallel Master Port Enable bit

1 = PMP enabled

0 = PMP disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **PSIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 12-11 **ADMUX1:ADMUX0:** Address/Data Multiplexing Selection bits<sup>(1)</sup>

11 = Reserved

10 = All 16 bits of address are multiplexed on PMD<7:0> pins

01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper 3 bits are multiplexed on PMA<10:8>

00 = Address and data appear on separate pins

bit 10 **PTBEEN:** Byte Enable Port Enable bit (16-bit Master mode)

1 = PMBE port enabled

0 = PMBE port disabled

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit

1 = PMWR/PMENB port enabled

0 = PMWR/PMENB port disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit

1 = PMRD/PMWR port enabled

0 = PMRD/PMWR port disabled

bit 7-6 **CSF1:CSF0:** Chip Select Function bits

11 = Reserved

10 = PMCS1 functions as chip select

0x = PMCS1 functions as address bit 14

bit 5 **ALP:** Address Latch Polarity bit<sup>(1)</sup>

1 = Active-high (PMALL and PMALH)

0 = Active-low (PMALL and PMALH)

bit 4 **Unimplemented:** Read as '0'

bit 3 **CS1P:** Chip Select 1 Polarity bit<sup>(1)</sup>

1 = Active-high (PMCS1/PMCS1)

0 = Active-low (PMCS1/PMCS1)

**Note 1:** These bits have no effect when their corresponding pins are used as address lines.

## **29.2 MPLAB C Compilers for Various Device Families**

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

## **29.3 HI-TECH C for Various Device Families**

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, pre-processor, and one-step driver, and can run on multiple platforms.

## **29.4 MPASM Assembler**

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

## **29.5 MPLINK Object Linker/ MPLIB Object Librarian**

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/librarian features include:

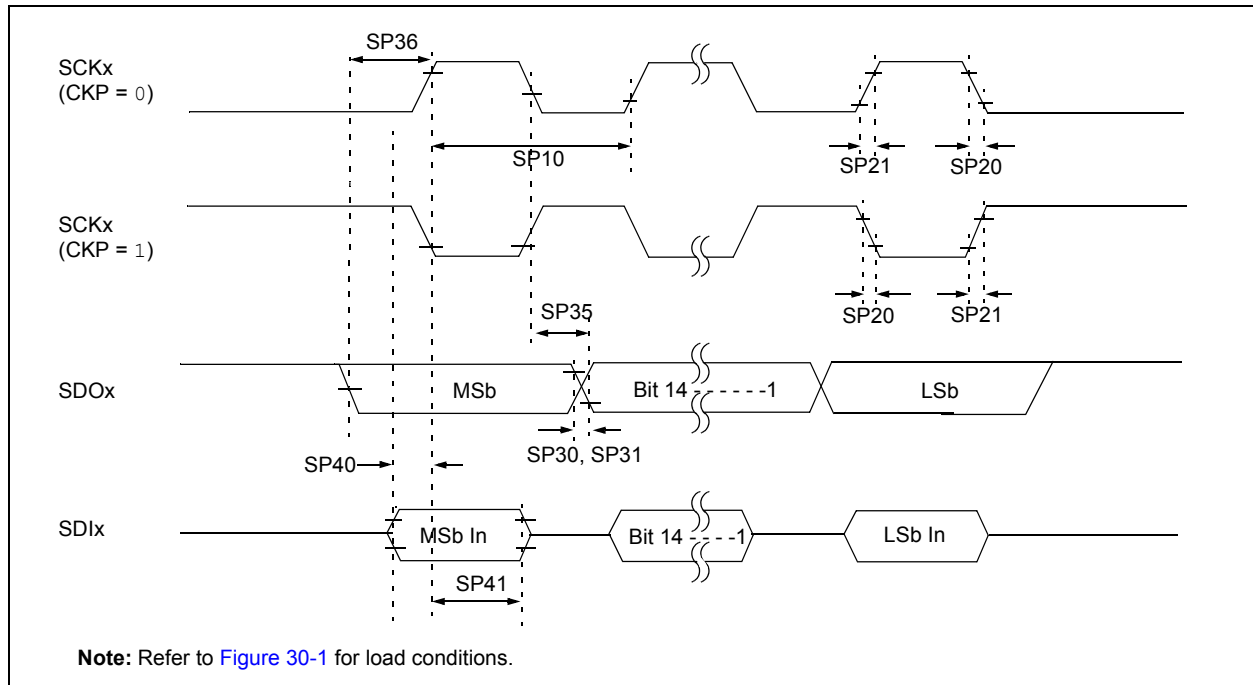
- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

## **29.6 MPLAB Assembler, Linker and Librarian for Various Device Families**

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

**FIGURE 30-11: SPIx MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS**



**TABLE 30-30: SPIx MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Typ <sup>(2)</sup>	Max	Units	Conditions
SP10	TscP	Maximum SCK Frequency	—	—	9	MHz	See Note 3
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See parameter DO32 and Note 4
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	—
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	—
SP40	TdiV2sch, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 111 ns. The clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

**TABLE 31-17: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS**

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
<b>Clock Parameters</b>							
HAD50	TAD	ADC Clock Period <sup>(1)</sup>	147	—	—	ns	—
<b>Conversion Rate</b>							
HAD56	FCNV	Throughput Rate <sup>(1)</sup>	—	—	400	Ksps	—

**Note 1:** These parameters are characterized but not tested in manufacturing.

**TABLE 31-18: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS**

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
<b>Clock Parameters</b>							
HAD50	TAD	ADC Clock Period <sup>(1)</sup>	104	—	—	ns	—
<b>Conversion Rate</b>							
HAD56	FCNV	Throughput Rate <sup>(1)</sup>	—	—	800	Ksps	—

**Note 1:** These parameters are characterized but not tested in manufacturing.

[illegible]