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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

⊡XFI

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	20 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DCI, DMA, I ² S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b/12b; D/A 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64gp802-h-mm

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.7 Arithmetic Logic Unit (ALU)

The dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/ X04, and dsPIC33FJ128GPX02/X04 ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the <u>SR register</u>. The <u>C and DC</u> Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157) for information on the SR bits affected by each instruction.

The dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit-divisor division.

3.7.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier of the DSP engine, the ALU supports unsigned, signed or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- · 8-bit unsigned x 8-bit unsigned

3.7.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 1. 32-bit signed/16-bit signed divide
- 2. 32-bit unsigned/16-bit unsigned divide
- 3. 16-bit signed/16-bit signed divide
- 4. 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. 16-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.8 DSP Engine

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a barrel shifter and a 40-bit adder/ subtracter (with two target accumulators, round and saturation logic).

The dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/ X04, and dsPIC33FJ128GPX02/X04 is a single-cycle instruction flow architecture; therefore, concurrent operation of the DSP engine with MCU instruction flow is not possible. However, some MCU ALU and DSP engine resources can be used concurrently by the same instruction (e.g., ED, EDAC).

The DSP engine can also perform inherent accumulator-to-accumulator operations that require no additional data. These instructions are ADD, SUB and NEG.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- · Fractional or integer DSP multiply (IF)
- Signed or unsigned DSP multiply (US)
- Conventional or convergent rounding (RND)
- Automatic saturation on/off for ACCA (SATA)
- Automatic saturation on/off for ACCB (SATB)
- Automatic saturation on/off for writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACC-SAT)

A block diagram of the DSP engine is shown in Figure 3-3.

TABLE 3-1:DSP INSTRUCTIONSSUMMARY

Instruction	Algebraic Operation	ACC Write Back
CLR	A = 0	Yes
ED	$A = (x - y)^2$	No
EDAC	$A = A + (x - y)^2$	No
MAC	$A = A + (x \bullet y)$	Yes
MAC	A = A + x2	No
MOVSAC	No change in A	Yes
MPY	$A = x \bullet y$	No
MPY	A = x 2	No
MPY.N	$A = -x \bullet y$	No
MSC	$A = A - x \bullet y$	Yes

TABLE 4-1: CPU CORE REGISTERS MAP (CONTINUED)

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
MODCON	0046	XMODEN	YMODEN		— — BWM<3:0> YWM<3:0> XWM<3:0>							0000						
XMODSRT	0048		XS<15:1>								0	XXXX						
XMODEND	004A		XE<15:1>								1	XXXX						
YMODSRT	004C		YS<15:1>								0	XXXX						
YMODEND	004E		YE<15:1> 1							1	XXXX							
XBREV	0050	BREN	BREN XB<14:0>								XXXX							
DISICNT	0052	_	— — Disable Interrupts Counter Register xx								XXXX							

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

5.0 FLASH PROGRAM MEMORY

- Note 1: This data sheet summarizes the features of the dsPIC33FJ32GP302/304 dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 5. "Flash Programming" (DS70191) of the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip website (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/ X04, and dsPIC33FJ128GPX02/X04 devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming[™] (ICSP[™]) programming capability
- Run-Time Self-Programming (RTSP)

ICSP allows any of the following devices, dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04, to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx), and three other lines for power (VDD), ground (Vss) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed devices and then program the digital signal controller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (table read) and TBLWT (table write) instructions. With RTSP, the user application can write program memory data either in blocks or 'rows' of 64 instructions (192 bytes) at a time or a single program memory word, and erase program memory in blocks or 'pages' of 512 instructions (1536 bytes) at a time.

5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the table read and table write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits <7:0> of the TBLPAG register and the Effective Address (EA) from a W register specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits <15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits <23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.





REGISTER 7-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1 (CONTINUED)

bit 2	CMIF: Comparator Interrupt Flag Status bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred

- bit 1 MI2C1IF: I2C1 Master Events Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 0 SI2C1IF: I2C1 Slave Events Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred

REGISTER	7-29: IPC17	: INTERRUPT	PRIORITY	Y CONTROL F	REGISTER 1	7						
U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0					
	—	—		—		C1TXIP<2:0>(1)						
bit 15							bit 8					
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0					
		DMA7IP<2:0>				DMA6IP<2:0>						
bit 7							bit (
Legend:												
R = Readab	ole bit	W = Writable I	bit	U = Unimpler	mented bit, rea	ad as '0'						
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown					
bit 15-11	Unimplemer	nted: Read as ')'									
bit 10-8	C1TXIP<2:0	>: FCAN1 Trans	smit Data Re	auest Interrupt	Priority bits ⁽¹⁾							
	111 = Interru	111 = Interrupt is priority 7 (highest priority interrupt)										
	•	•										
	•	•										
	•											
	001 = Interru 000 = Interru	upt is priority 1 upt source is disa	abled									
bit 7	Unimplemer	nted: Read as '()'									
bit 6-4	DMA7IP<2:0	>: DMA Channe	el 7 Data Tra	ansfer Complete	e Interrupt Prio	ritv bits						
	111 = Interru	111 = Interrupt is priority 7 (highest priority interrupt)										
	•	•										
	•											
	•	•										
	001 = Interru	001 = Interrupt is priority 1										
	000 = Interru	pt source is dis	abled									
bit 3	Unimplemer	nted: Read as '0)'									
bit 2-0	DMA6IP<2:0	>: DMA Channe	el 6 Data Tra	ansfer Complete	e Interrupt Prio	rity bits						
	111 = Interru	111 = Interrupt is priority 7 (highest priority interrupt)										
	•											
	•											
	•											
		ipt is priority 1	ablad									
	000 = Interru	ipi source is disa	aplea									

Note 1: Interrupts are disabled on devices without ECAN[™] modules.

11.2 Open-Drain Configuration

In addition to the PORT, LAT and TRIS registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V) on any desired 5V tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

Refer to **"Pin Diagrams"** for the available pins and their functionality.

11.3 Configuring Analog Port Pins

The AD1PCFGL and TRIS registers control the operation of the Analog-to-Digital (ADC) port pins. The port pins that are to function as analog inputs must have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) is converted.

The AD1PCFGL register has a default value of 0x0000; therefore, all pins that share ANx functions are analog (not digital) by default.

When the PORT register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

11.4 I/O Port Write/Read Timing

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be an NOP, as shown in Example 11-1.

11.5 Input Change Notification

The input change notification function of the I/O ports allows the dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/ X04 devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature can detect input change-ofstates even in Sleep mode, when the clocks are disabled. Depending on the device pin count, up to 21 external signals (CNx pin) can be selected (enabled) for generating an interrupt request on a change-ofstate.

Four control registers are associated with the CN module. The CNEN1 and CNEN2 registers contain the interrupt enable control bits for each of the CN input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CN pin also has a weak pull-up connected to it. The pull-ups act as a current source connected to the pin, and eliminate the need for external resistors when push-button or keypad devices are connected. The pull-ups are enabled separately using the CNPU1 and CNPU2 registers, which contain the control bits for each of the CN pins. Setting any of the control bits enables the weak pull-ups for the corresponding pins.

Note: Pull-ups on change notification pins should always be disabled when the port pin is configured as a digital output.

MOV0xFF00, W0; Configure PORTB<15:8> as inputsMOVW0, TRISBB; and PORTB<7:0> as outputsNOP; Delay 1 cyclebtssPORTB, #13; Next Instruction

PORT WRITE/READ EXAMPLE

EXAMPLE 11-1:

11.6.2.2 Output Mapping

In contrast to inputs, the outputs of the peripheral pin select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 5-bit fields, with each set associated with one RPn pin (see Register 11-17 through Register 11-29). The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 11-2 and Figure 11-3).

The list of peripherals for output mapping also includes a null value of '00000' because of the mapping technique. This permits any given pin to remain unconnected from the output of any of the pin selectable peripherals.



Function RPnR<4:0> **Output Name** NULL RPn tied to default port pin 00000 C10UT RPn tied to Comparator1 Output 00001 C2OUT RPn tied to Comparator2 Output 00010 U1TX 00011 RPn tied to UART1 Transmit **U1RTS** 00100 RPn tied to UART1 Ready To Send U2TX RPn tied to UART2 Transmit 00101 U2RTS 00110 RPn tied to UART2 Ready To Send SDO1 RPn tied to SPI1 Data Output 00111 SCK1 01000 RPn tied to SPI1 Clock Output SS1 01001 RPn tied to SPI1 Slave Select Output SDO2 RPn tied to SPI2 Data Output 01010 RPn tied to SPI2 Clock Output SCK2 01011 SS2 RPn tied to SPI2 Slave Select Output 01100 CSDO 01101 RPn tied to DCI Serial Data Output CSCK RPn tied to DCI Serial Clock Output 01110 COFS RPn tied to DCI Frame Sync Output 01111 C1TX 10000 RPn tied to ECAN1 Transmit OC1 RPn tied to Output Compare 1 10010 OC2 RPn tied to Output Compare 2 10011 OC3 RPn tied to Output Compare 3 10100

RPn tied to Output Compare 4

TABLE 11-2: OUTPUT SELECTION FOR REMAPPABLE PIN (RPn)

10101

OC4

dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, AND dsPIC33FJ128GPX02/X04

REGISTER 11-2:	RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1
----------------	---

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
—	—	_	_	—	—	—	_		
bit 15							bit 8		
U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1		
—	—	—			INT2R<4:0>				
bit 7							bit 0		
Legend:									
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'					
-n = Value at POR '1' = Bit is set				'0' = Bit is cle	ared	x = Bit is unkr	nown		

bit 15-5 Unimplemented: Read as '0'

bit 4-0 INT2R<4:0>: Assign External Interrupt 2 (INTR2) to the corresponding RPn pin

11111 = Input tied to Vss 11001 = Input tied to RP25

•

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00001 = Input tied to RP1 00000 = Input tied to RP0

REGISTER 11-9: RI	PINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19
-------------------	---

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1				
—	—	—			U2CTSR<4:0)>					
bit 15							bit 8				
U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1				
_					U2RXR<4:0	>					
bit 7							bit 0				
Legend:											
R = Readabl	le bit	W = Writable	bit	U = Unimplei	mented bit, rea	ad as '0'					
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown				
bit 15-13	Unimplemen	ted: Read as ')'								
bit 12-8	U2CTSR<4:0>: Assign UART2 Clear to Send (U2CTS) to the corresponding RPn pin										
	11111 = Input tied to Vss										
	11001 = Inpu	ut tied to RP25									
	•										
	•										
	•										
	00001 = Input tied to RP1										
bit 7-5		ited: Read as 'i	ר י								
bit 4_0			2 Receive (LI	2RX) to the co	rresponding R	Pn nin					
	11111 = Inni	It fied to Vss			responding re	i ii pili					
	11001 = Inp	11001 = Input tied to VSS									
	•										
	•										
	•										
	00001 = Inpu	ut tied to RP1									
	00000 = Inp u	ut tied to RP0									

8 ⁽¹⁾

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—	—			RP17R<4:0>	>		
bit 15							bit 8	
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—	—			RP16R<4:0>	>		
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable b			bit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set				'0' = Bit is cleared x = Bit is unknown				

bit 15-13	Unimplemented: Read as '0'
bit 12-8	RP17R<4:0>: Peripheral Output Function is Assigned to RP17 Output Pin bits (see Table 11-2 for peripheral function numbers)
bit 7-5	Unimplemented: Read as '0'
bit 4-0	RP16R<4:0>: Peripheral Output Function is Assigned to RP16 Output Pin bits (see Table 11-2 for peripheral function numbers)

Note 1: This register is implemented in 44-pin devices only.

REGISTER 11-26: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9⁽¹⁾

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—			RP19R<4:0>				
bit 15							bit 8	
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—	—			RP18R<4:0>			
bit 7							bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 Unimplemented: Read as '0'

bit 12-8 **RP19R<4:0>:** Peripheral Output Function is Assigned to RP19 Output Pin bits (see Table 11-2 for peripheral function numbers)

bit 7-5 Unimplemented: Read as '0'

bit 4-0 **RP18R<4:0>:** Peripheral Output Function is Assigned to RP18 Output Pin bits (see Table 11-2 for peripheral function numbers)

Note 1: This register is implemented in 44-pin devices only.

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—			RP25R<4:0>	>	
bit 15		-					bit 8
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—		—			RP24R<4:0>	>	
bit 7	•						bit 0
Legend:							
R = Readable bit W = Writable b		bit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set			'0' = Bit is cle	ared	x = Bit is unkr	nown	

REGISTER 11-29: RPOR12: PERIPHERAL PIN SELECT OUTPUT REGISTER 12⁽¹⁾

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **RP25R<4:0>:** Peripheral Output Function is Assigned to RP25 Output Pin bits (see Table 11-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP24R<4:0>:** Peripheral Output Function is Assigned to RP24 Output Pin bits (see Table 11-2 for peripheral function numbers)

Note 1: This register is implemented in 44-pin devices only.

REGISTER 18-2: UXSTA: UARTX STATUS AND CONTROL REGISTER	REGISTER 18-2:
---	----------------

R/W-0	R/W-0	R/W-0	U-0	R/W-0 HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN ⁽¹⁾	UTXBF	TRMT
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISE	URXISEL<1:0> AI		RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0
Legend: HC = Hardware cleared				C = Clea	ar only bit		
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set		'0' = Bit is cleared x = Bit is unknown		nown			

bit 15,13	UTXISEL<1:0>: Transmission Interrupt Mode Selection bits
	11 = Reserved; do not use
	10 = Interrupt when a character is transferred to the Transmit Shift register, and as a result, the
	transmit buffer becomes empty
	operations are completed
	00 = Interrupt when a character is transferred to the Transmit Shift register (this implies there is at least one character open in the transmit buffer)
bit 14	UTXINV: Transmit Polarity Inversion bit
	<u>If IREN = 0:</u>
	1 = UxTX Idle state is '0'
	$\frac{\text{If IREN = 1:}}{1}$
	1 = IrDA [®] encoded UxTX Idle state is '1'
h:: 10	
DIT	UIXBRK: Iransmit Break bit
	\perp = Send Sync Break on next transmission – Start bit, followed by twelve \cup bits, followed by Stop bit; cleared by bardware upon completion
	0 = Sync Break transmission disabled or completed
bit 10	UTXEN: Transmit Enable bit ⁽¹⁾
	1 = Transmit enabled, UxTX pin controlled by UARTx
	0 = Transmit disabled, any pending transmission is aborted and buffer is reset. UxTX pin controlled
	by port
bit 9	UTXBF: Transmit Buffer Full Status bit (read-only)
	1 = Transmit buffer is full
	0 = Iransmit buffer is not full, at least one more character can be written
bit 8	TRMT: Transmit Shift Register Empty bit (read-only)
	 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed) 0 = Transmit Shift Register is not empty, a transmission is in progress or queued
bit 7-6	URXISEL<1:0>: Receive Interrupt Mode Selection bits
	11 = Interrupt is set on UxRSR transfer making the receive buffer full (i.e., has 4 data characters)
	10 = Interrupt is set on UxRSR transfer making the receive buffer 3/4 full (i.e., has 3 data characters)
	Ux = Interrupt is set when any character is received and transferred from the UXRSR to the receive buffer. Receive buffer has one or more characters

Note 1: Refer to **Section 17. "UART"** (DS70188) in the *"dsPIC33F/PIC24H Family Reference Manual"* for information on enabling the UART module for transmit operation.

20.3 DCI Control Registers

DCICON1: DCI CONTROL REGISTER 1 REGISTER 20-1: U-0 R/W-0 U-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 DCIEN DCISIDL DLOOP CSCKD CSCKE COFSD ____ ___ bit 15 R/W-0 R/W-0 R/W-0 U-0 U-0 U-0 R/W-0 R/W-0 UNFM CSDOM DJST ____ ___ COFSM<1:0> ____ bit 7

t W = Writable hit	[] = []nimplemented bit	read as '0'
$\mathbf{R} \qquad (1) = \text{Bit is set}$	$0^{\circ} = \text{Bit is cleared}$	x = Bit is unknown
CIEN: DCI Module Enable bit		
= Module is enabled		
Jnimplemented: Read as '0'		
DCISIDL: DCI Stop in Idle Control bit = Module will halt in CPU Idle mode = Module will continue to operate in (CPU Idle mode	
Jnimplemented: Read as '0'		
DLOOP: Digital Loopback Mode Contr	ol bit	
= Digital Loopback mode is enabled.	CSDI and CSDO pins intern	ally connected.
CSCKD: Sample Clock Direction Conti	rol bit	
= CSCK pin is an input when DCI mo	odule is enabled	
) = CSCK pin is an output when DCI m	nodule is enabled	
CSCKE: Sample Clock Edge Control b	bit	
 = Data changes on serial clock falling = Data changes on serial clock rising 	g edge, sampled on serial clo edge, sampled on serial clo	ock rising edge ck falling edge
COFSD: Frame Synchronization Direct	tion Control bit	
 = COFS pin is an input when DCI mo = COFS pin is an output when DCI m 	odule is enabled nodule is enabled	
JNFM: Underflow Mode bit		
 Transmit last value written to the transmit '0's on a transmit underflow 	ansmit registers on a transm w	it underflow
CSDOM: Serial Data Output Mode bit		
 = CSDO pin will be tri-stated during of = CSDO pin drives '0's during disable 	lisabled transmit time slots ed transmit time slots	
DJST: DCI Data Justification Control bi	it	
 Data transmission/reception is beg synchronization pulse 	gun during the same serial cl	ock cycle as the frame
D = Data transmission/reception is begins	gun one serial clock cycle afte	er frame synchronization pulse
Jnimplemented: Read as '0'		
COFSM<1:0>: Frame Sync Mode bits		
1 = 20-bit AC-Link mode		
10 = 16-bit AC-Link mode		
1 = If'S Frame Sync mode		
	t W = Writable bit r1' = Bit is set CIEN: DCI Module Enable bit 1 = Module is enabled 0 = Module is disabled Jnimplemented: Read as '0' CISIDL: DCI Stop in Idle Control bit 1 = Module will halt in CPU Idle mode 0 = Module will continue to operate in O Jnimplemented: Read as '0' DLOOP: Digital Loopback Mode Control 1 = Digital Loopback mode is enabled. 0 = Digital Loopback mode is disabled CSCKD: Sample Clock Direction Control 1 = Data changes on serial clock falling 0 = Data changes on serial clock falling 0 = Dops pin is an input when DCI m CGFSD: Frame Synchronization Direct 1 = COFS pin is an output when DCI m DIFM: Underflow Mode bit 1 = Transmit last value written to the trady 0 = CSDO pin will be tri-stated during to 0 = CSDO pin will be tri-stated during to 0 = CSDO pin drives '0's during disable 0 = Data transmission/reception is begin synchronization pulse 0 = Data transmission/reception is begin synchronization pulse 0 = Data transmission/reception is begin synchronization pulse 0 = Data transmission/reception is begin synchronization pulse	t W = Writable bit U = Unimplemented bit, R '1' = Bit is set '0' = Bit is cleared DCIEN: DCI Module Enable bit - 1 = Module is enabled - 0 = Module is disabled - Jimplemented: Read as '0' - DCISIDL: DCI Stop in Idle Control bit - 1 = Module will continue to operate in CPU Idle mode - 0 = Module will continue to operate in CPU Idle mode - Jimplemented: Read as '0' - DLOOP: Digital Loopback Mode Control bit - 1 = Digital Loopback mode is enabled. CSDI and CSDO pins interr - 0 = Digital Loopback mode is disabled - CSCKD: Sample Clock Direction Control bit - 1 = CSCK pin is an input when DCI module is enabled - 0 = CSCKE: Sample Clock Edge Control bit - 1 = Data changes on serial clock rising edge, sampled on serial cloc - CSCFSD: Frame Synchronization Direction Control bit - 1 = COFS pin is an input when DCI module is enabled - 0 = COFS pin is an output when DCI module is enabled - 0 = COFS pin is an output when DCI module is enabled - 0 = COFS

bit 8

bit 0

REGISTER 21-4: AD1CO	4: ADC1 CON	ITROL REGISTER 4
----------------------	-------------	-------------------------

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—		—	—	—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	DMABL<2:0>		
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'			
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown

bit 15-3 Unimplemented: Read as '0'

bit 2-0 DMABL<2:0>: Selects Number of DMA Buffer Locations per Analog Input bits

111 = Allocates 128 words of buffer to each analog input

110 = Allocates 64 words of buffer to each analog input

101 = Allocates 32 words of buffer to each analog input

100 = Allocates 16 words of buffer to each analog input

011 = Allocates 8 words of buffer to each analog input

010 = Allocates 4 words of buffer to each analog input

001 = Allocates 2 words of buffer to each analog input

000 = Allocates 1 word of buffer to each analog input

dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, AND dsPIC33FJ128GPX02/X04

REGISTER 24-6: RTCVAL (WHEN RTCPTR<1:0> = 01): WKDYHR: WEEKDAY AND HOURS VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—		WDAY<2:0>	
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—		HRTEN<1:0>			HRON	E<3:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11	Unimplemented: Read as '0'
bit 10-8	WDAY<2:0>: Binary Coded Decimal Value of Weekday Digit; contains a value from 0 to 6
bit 7-6	Unimplemented: Read as '0'
bit 5-4	HRTEN<1:0>: Binary Coded Decimal Value of Hour's Tens Digit; contains a value from 0 to 2
bit 3-0	HRONE<3:0>: Binary Coded Decimal Value of Hour's Ones Digit; contains a value from 0 to 9

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 24-7: RTCVAL (WHEN RTCPTR<1:0> = 00): **MINUTES AND SECONDS VALUE REGISTER**

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
_		MINTEN<2:0>			MINON	IE<3:0>	
bit 15							bit 8
U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x

—	SECTEN<2:0>	SECONE<3:0>
bit 7		bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	Unimplemented: Read as '0'
bit 14-12	MINTEN<2:0>: Binary Coded Decimal Value of Minute's Tens Digit; contains a value from 0 to 5
bit 11-8	MINONE<3:0>: Binary Coded Decimal Value of Minute's Ones Digit; contains a value from 0 to 9
bit 7	Unimplemented: Read as '0'
bit 6-4	SECTEN<2:0>: Binary Coded Decimal Value of Second's Tens Digit; contains a value from 0 to 5
bit 3-0	SECONE<3:0>: Binary Coded Decimal Value of Second's Ones Digit; contains a value from 0 to 9

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NOTES:

27.0 SPECIAL FEATURES

- Note 1: This data sheet summarizes the features of the dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33F/PIC24H Family Reference Manual". Please see the Microchip web site (www.microchip.com) for the latest dsPIC33F/PIC24H Family Reference Manual sections.
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- · Flexible configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard[™] Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming[™] (ICSP[™])
- In-Circuit emulation

27.1 Configuration Bits

The dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/ X04, and dsPIC33FJ128GPX02/X04 devices provide nonvolatile memory implementation for device configuration bits. Refer to **Section 25. "Device Configuration"** (DS70194), in the *"dsPIC33F/PIC24H Family Reference Manual"* for more information on this implementation.

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped starting at program memory location 0xF80000.

The individual Configuration bit descriptions for the Configuration registers are shown in Table 27-2.

Note that address 0xF80000 is beyond the user program memory space. It belongs to the configuration memory space (0x800000-0xFFFFFF), which can only be accessed using table reads and table writes.

The Device Configuration register map is shown in Table 27-1.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xF80000	FBS	RBS<	:1:0>	_	—		BSS<2:0>		BWRP
0xF80002	FSS ⁽¹⁾	RSS<	:1:0>	_	—		SSS<2:0> SV		
0xF80004	FGS	—			—	—	GSS<1	:0>	GWRP
0xF80006	FOSCSEL	IESO	—	_	_	-	FNOSC<2:0>		
0xF80008	FOSC	FCKSM	1<1:0>	IOL1WAY	—	—	OSCIOFNC POSCMD<1		ID<1:0>
0xF8000A	FWDT	FWDTEN	WINDIS	_	WDTPRE		WDTPOST<3:0>		
0xF8000C	FPOR		Reserved	(2)	ALTI2C	—	FPWRT<2:0>		
0xF8000E	FICD	Reser	ved ⁽³⁾	JTAGEN	—	—	— ICS<1:0>		:1:0>
0xF80010	FUID0				User Unit ID) Byte 0			
0xF80012	FUID1		User Unit ID Byte 1						
0xF80014	FUID2		User Unit ID Byte 2						
0xF80016	FUID3		User Unit ID Byte 3						

TABLE 27-1: DEVICE CONFIGURATION REGISTER MAP

Legend: — = unimplemented bit, read as '0'.

Note 1: This Configuration register is not available and reads as 0xFF on dsPIC33FJ32GP302/304 devices.

2: These bits are reserved and always read as '1'.

3: These bits are reserved for use by development tools and must be programmed as '1'.

TABLE 30-33:SPIX SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING
REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				/ to 3.6V 85°C for Industrial 125°C for Extended
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур ⁽²⁾	Max	Units	Conditions
SP70	TscP	Maximum SCK Input Frequency	—	_	11	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	—	_	_	ns	See parameter DO32 and Note 4
SP73	TscR	SCKx Input Rise Time	—			ns	See parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—			ns	See parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—			ns	See parameter DO31 and Note 4
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	—
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30			ns	_
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_		ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	_	_	ns	—
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx \uparrow or SCKx Input	120			ns	_
SP51	TssH2doZ	SSx	10		50	ns	_
SP52	TscH2ssH TscL2ssH	SSx after SCKx Edge	1.5 TCY + 40	_	_	ns	See Note 4
SP60	TssL2doV	SDOx Data Output Valid after SSx Edge	—	_	50	ns	—

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

3: The minimum clock period for SCKx is 91 ns. Therefore, the SCK clock generated by the Master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







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RCON (Reset Control)
RSCON (DCI Receive Slot Control)
SPIxCON1 (SPIx Control 1)
SPIxCON2 (SPIx Control 2)
SPIxSTAT (SPIx Status and Control)
SR (CPU Status)
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