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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

E·XFI

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	20 MIPS
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DCI, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K × 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b/12b; D/A 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64gp802-h-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

#### 28-Pin QFN-S<sup>(2)</sup> Pins are up to 5V tolerant AN10/DAC1LP/RTCC/RP14<sup>(1)</sup>/CN12/PMWR/RB14 AN9/DAC1LN/RP15(1)/CN11/PMCS1/RB15 AN0/VREF+/CN2/RA0 AN1/NREF-/CN3/RA1 MCLR AVDD AVSS 27 [ 26 [ 25 [ 28 24 [ 23 [ 22 [ PGED1/AN2/C2IN-/RP0<sup>(1)</sup>/CN4/RB0 1 AN11/DAC1RN/RP13<sup>(1)</sup>/CN13/PMRD/RB13 21 PGEC1/AN3/C2IN+/RP1(1)/CN5/RB1 2 AN12/DAC1RP/RP12<sup>(1)</sup>/CN14/PMD0/RB12 20 AN4/C1IN-/RP2<sup>(1)</sup>/CN6/RB2 PGEC2/TMS/RP11<sup>(1)</sup>/CN15/PMD1/RB11 3 dsPIC33FJ64GP802 19 PGED2/TDI/RP10<sup>(1)</sup>/CN16/PMD2/RB10 AN5/C1IN+/RP3(1)/CN7/RB3 4 dsPIC33FJ128GP802 18 Vss 5 VCAP 17 OSC1/CLKI/CN30/RA2 6 16 Vss TDO/SDA1/RP9(1)/CN21/PMD3/RB9 OSC2/CLKO/CN29/PMA0/RA3 7 15 9 2 33 4 PGEC3/ASCL1/RP6<sup>(1)</sup>/CN24/PMD6/RB6 INT0/RP7<sup>(1)</sup>/CN23/PMD5/RB7 PGED3/ASDA1/RP5<sup>(1)</sup>/CN27/PMD7/RB5 TCK/SCL1/RP8<sup>(1)</sup>/CN22/PMD4/RB8 SOSCI/RP4<sup>(1)</sup>/CN1/PMBE/RB4 VDD SOSCO/T1CK/CN0/PMA1/RA4 The RPx pins can be used by any remappable peripheral. See Table 1 in this section for the list of available peripherals. Note 1: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally. 2:

#### Pin Diagrams (Continued)

# 3.0 CPU

- Note 1: This data sheet summarizes the features of the dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 2. "CPU" (DS70204) of the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip website (www.microchip.com).
  - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

# 3.1 Overview

The dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/ X04, and dsPIC33FJ128GPX02/X04 CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for DSP. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. The actual amount of program memory implemented varies by device. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any time.

The dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/ X04, and dsPIC33FJ128GPX02/X04 devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can serve as a data, address or address offset register. The 16th working register (W15) operates as a software Stack Pointer (SP) for interrupts and calls.

There are two classes of instruction in the dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 devices: MCU and DSP. These two instruction classes are seamlessly integrated into a single CPU. The instruction set includes many addressing modes and is designed for optimum C compiler efficiency. For most instructions, the dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 is capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and

a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing A + B = C operations to be executed in a single cycle.

A block diagram of the CPU is shown in Figure 3-1, and the programmer's model for the dsPIC33FJ32GP302/ 304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 is shown in Figure 3-2.

# 3.2 Data Addressing Overview

The data space can be addressed as 32K words or 64 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear data space. Certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device-specific.

Overhead-free circular buffers (Modulo Addressing mode) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. Furthermore, the X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms.

The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page (PSVPAG) register. The program-to-data-space mapping feature lets any instruction access program space as if it were data space.

# 3.3 DSP Engine Overview

The DSP engine features a high-speed 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bidirectional barrel shifter. The barrel shifter is capable of shifting a 40-bit value up to 16 bits right or left, in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal realtime performance. The MAC instruction and other associated instructions can concurrently fetch two data operands from memory while multiplying two W registers and accumulating and optionally saturating the result in the same cycle. This instruction functionality requires that the RAM data space be split for these instructions and linear for all others. Data space partitioning is achieved in a transparent and flexible manner through dedicating certain working registers to each address space.

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#### 4.4.1 SOFTWARE STACK

In addition to its use as a working register, the W15 register in the dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 devices is also used as a software Stack Pointer. The Stack Pointer always points to the first available free word and grows from lower to higher addresses. It pre-decrements for stack pops and post-increments for stack pushes, as shown in Figure 4-6. For a PC push during any CALL instruction, the MSb of the PC is zero-extended before the push, ensuring that the MSb is always clear.

Note: A PC push during exception processing concatenates the SRL register to the MSb of the PC prior to the push.

The Stack Pointer Limit register (SPLIM) associated with the Stack Pointer sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '0' because all stack operations must be word aligned.

Whenever an EA is generated using W15 as a source or destination pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal and a push operation is performed, a stack error trap does not occur. The stack error trap occurs on a subsequent push operation. For example, to cause a stack error trap when the stack grows beyond address 0x2000 in RAM, initialize the SPLIM with the value 0x1FFE.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0x0800. This prevents the stack from interfering with the Special Function Register (SFR) space.

A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.

FIGURE 4-6: CALL STACK FRAME



### 4.4.2 DATA RAM PROTECTION FEATURE

The dsPIC33F product family supports Data RAM protection features that enable segments of RAM to be protected when used in conjunction with Boot and Secure Code Segment Security. BSRAM (Secure RAM segment for BS) is accessible only from the Boot Segment Flash code when enabled. SSRAM (Secure RAM segment for RAM) is accessible only from the Secure Segment Flash code when enabled. See Table 4-1 for an overview of the BSRAM and SSRAM SFRs.

## 4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-37 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

#### 4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (near data space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire data space.

### 4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2 where:

Operand 1 is always a working register (that is, the addressing mode can only be register direct), which is referred to as Wb.

Operand 2 can be a W register, fetched from data memory, or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- · Register Indirect
- · Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-bit or 10-bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.



#### FIGURE 6-2: SYSTEM RESET TIMING

- **Note 1: POR:** A POR circuit holds the device in Reset when the power supply is turned on. The POR circuit is active until VDD crosses the VPOR threshold and the delay TPOR has elapsed.
  - 2: BOR: The on-chip voltage regulator has a BOR circuit that keeps the device in Reset until VDD crosses the VBOR threshold and the delay TBOR has elapsed. The delay TBOR ensures the voltage regulator output becomes stable.
  - **3: PWRT Timer:** The programmable power-up timer continues to hold the processor in Reset for a specific period of time (TPWRT) after a BOR. The delay TPWRT ensures that the system power supplies have stabilized at the appropriate level for full-speed operation. After the delay TPWRT has elapsed, the SYSRST becomes inactive, which in turn enables the selected oscillator to start generating clock cycles.
  - 4: Oscillator Delay: The total delay for the clock to be ready for various clock source selections are given in Table 6-1. Refer to Section 9.0 "Oscillator Configuration" for more information.
  - **5:** When the oscillator clock is ready, the processor begins execution from location 0x000000. The user application programs a GOTO instruction at the reset address, which redirects program execution to the appropriate start-up routine.
  - 6: The Fail-Safe Clock Monitor (FSCM), if enabled, begins to monitor the system clock when the system clock is ready and the delay TFSCM elapsed.

Symbol	Parameter	Value
VPOR	POR threshold	1.8V nominal
TPOR	POR extension time	30 μs maximum
VBOR	BOR threshold	2.5V nominal
TBOR	BOR extension time	100 μs maximum
TPWRT	Programmable power-up time delay	0-128 ms nominal
TFSCM	Fail-Safe Clock Monitor Delay	900 μs maximum

TABLE 6-2:	OSCILLATOR DELAY

When the device exits the Reset condi-Note: tion (begins normal operation), the device operating parameters (voltage, frequency, temperature, etc.) must be within their operating ranges, otherwise the device may not function correctly. The user application must ensure that the delay between the time power is first applied, and the time SYSRST becomes inactive, is long enough to get all operating parameters within specification.

## 6.4 Power-on Reset (POR)

A Power-on Reset (POR) circuit ensures the device is reset from power-on. The POR circuit is active until VDD crosses the VPOR threshold and the delay TPOR has elapsed. The delay TPOR ensures the internal device bias circuits become stable.

The device supply voltage characteristics must meet the specified starting voltage and rise rate requirements to generate the POR. Refer to Section 30.0 "Electrical Characteristics" for details.

The POR status bit (POR) in the Reset Control register (RCON<0>) is set to indicate the Power-on Reset.

# 6.4.1 Brown-out Reset (BOR) and Power-up timer (PWRT)

The on-chip regulator has a Brown-out Reset (BOR) circuit that resets the device when the VDD is too low (VDD < VBOR) for proper device operation. The BOR circuit keeps the device in Reset until VDD crosses VBOR threshold and the delay TBOR has elapsed. The delay TBOR ensures the voltage regulator output becomes stable.

The BOR status bit (BOR) in the Reset Control register (RCON<1>) is set to indicate the Brown-out Reset.

The device will not run at full speed after a BOR as the VDD should rise to acceptable levels for full-speed operation. The PWRT provides power-up time delay (TPWRT) to ensure that the system power supplies have stabilized at the appropriate levels for full-speed operation before the SYSRST is released.

The power-up timer delay (TPWRT) is programmed by the Power-on Reset Timer Value Select bits (FPWRT<2:0>) in the POR Configuration register (FPOR<2:0>), which provides eight settings (from 0 ms to 128 ms). Refer to **Section 27.0 "Special Features"** for further details.

Figure 6-3 shows the typical brown-out scenarios. The reset delay (TBOR + TPWRT) is initiated each time VDD rises above the VBOR trip point

# 7.0 INTERRUPT CONTROLLER

- Note 1: This data sheet summarizes the features of the dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 32. "Interrupts (Part III)" (DS70214) of the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip website (www.microchip.com).
  - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/ X04, and dsPIC33FJ128GPX02/X04 interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/ X04, and dsPIC33FJ128GPX02/X04 CPU.

The interrupt controller has the following features:

- Up to eight processor exceptions and software traps
- Eight user-selectable priority levels
- Interrupt Vector Table (IVT) with up to 118 vectors
- A unique vector for each interrupt or exception source
- · Fixed priority within a specified user priority level
- Alternate Interrupt Vector Table (AIVT) for debug support
- Fixed interrupt entry and return latencies

# 7.1 Interrupt Vector Table

The Interrupt Vector Table (IVT), shown in Figure 7-1, resides in program memory, starting at location 000004h. The IVT contains 126 vectors consisting of eight nonmaskable trap vectors plus up to 118 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with vector 0 takes priority over interrupts at any other vector address.

dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 devices implement up to 53 unique interrupts and five nonmaskable traps. These are summarized in Table 7-1.

#### 7.1.1 ALTERNATE INTERRUPT VECTOR TABLE

The Alternate Interrupt Vector Table (AIVT) is located after the IVT, as shown in Figure 7-1. Access to the AIVT is provided by the ALTIVT control bit (INTCON2<15>). If the ALTIVT bit is set, all interrupt and exception processes use the alternate vectors instead of the default vectors. The alternate vectors are organized in the same manner as the default vectors.

The AIVT supports debugging by providing a means to switch between an application and a support environment without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time. If the AIVT is not needed, the AIVT should be programmed with the same addresses used in the IVT.

# 7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 device clears its registers in response to a Reset, which forces the PC to zero. The digital signal controller then begins program execution at location 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

**Note:** Any unimplemented or unused vector locations in the IVT and AIVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

### FIGURE 7-1: dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, AND dsPIC33FJ128GPX02/ X04 INTERRUPT VECTOR TABLE

I	Poact come Instruction		
	Reset - GOTO Instruction		
	Reset – GOTO Address	0x000002	
	Reserved	0x000004	
	Oscillator Fail Trap Vector		
	Address Error Trap Vector		
	Stack Error Trap Vector		
	Math Error Trap Vector		
	DMA Error Trap Vector		
	Reserved		
	Reserved		-
	Interrupt Vector 0	0x000014	
	Interrupt Vector 1		
	~		
	~		
	~		
	Interrupt Vector 52	0x00007C	Interrupt Vector Table (IVT) <sup>(1)</sup>
~	Interrupt Vector 53	0x00007E	
ority	Interrupt Vector 54	0x000080	
Pric	~		
er F	~	_	
Drde	~		
	Interrupt Vector 116	0x0000FC	1
nre	Interrupt Vector 117	0x0000FE	
Vat	Reserved	0x000100	
l Di	Reserved	0x000102	
Isir	Reserved	_	
rea	Oscillator Fail Trap Vector	_	
)ec	Address Error Trap Vector	_	
	Stack Error Trap Vector	_	
	Math Error Trap Vector	_	
	DMA Error Trap vector		7
	Reserved	_	
	Reserved	0.000444	
	Interrupt Vector U	0x000114	
	Interrupt vector 1	_	
	~	_	
	~	_	Alternate intermed $V_{0}$ star Table (AIV/T)(1)
		0.000170	Alternate interrupt vector Table (AIVI)
	Interrupt Vector 52	0x00017C	
	Interrupt Vector 53	0x00017E	
	Interrupt vector 54	0000180	
	~	_	
	~	-	
	Interrupt Vector 116		1
	Interrupt Vector 116		
★	Start of Code		
Ť	Stall OF CODE	0x000200	
Note 1	Soo Table 7.1 for the list of implement	ontod intorrunt	vectors
NOTE 1	See Table (-1 for the list of impleme	enteu interrupt	

# REGISTER 7-10: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0 (CONTINUED)

bit 2	OC1IE: Output Compare Channel 1 Interrupt Enable bit
	<ul><li>1 = Interrupt request enabled</li><li>0 = Interrupt request not enabled</li></ul>
bit 1	IC1IE: Input Capture Channel 1 Interrupt Enable bit
	1 = Interrupt request enabled
	0 = Interrupt request not enabled
bit 0	INTOIE: External Interrupt 0 Flag Status bit
	<ul><li>1 = Interrupt request enabled</li><li>0 = Interrupt request not enabled</li></ul>

The DMA controller features eight identical data transfer channels.

Each channel has its own set of control and status registers. Each DMA channel can be configured to copy data either from buffers stored in dual port DMA RAM to peripheral SFRs, or from peripheral SFRs to buffers in DMA RAM.

The DMA controller supports the following features:

- Eight DMA channels
- Register Indirect With Post-increment Addressing mode
- Register Indirect Without Post-increment Addressing mode
- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU interrupt after half or full block transfer complete

- · Byte or word transfers
- · Fixed priority channel arbitration
- Manual (software) or Automatic (peripheral DMA requests) transfer initiation
- One-Shot or Auto-Repeat block transfer modes
- Ping-Pong mode (automatic switch between two DPSRAM start addresses after each block transfer complete)
- DMA request for each channel can be selected from any supported interrupt source
- · Debug support features

For each DMA channel, a DMA interrupt request is generated when a block transfer is complete. Alternatively, an interrupt can be generated when half of the block has been filled.



### FIGURE 8-1: TOP LEVEL SYSTEM ARCHITECTURE USING A DEDICATED TRANSACTION BUS

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	SELACLK	AOSCI	MD<1:0>		APSTSCLR<2:0	>
bit 15							bit
R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
ASRCSEL	_	—	—		—		—
bit 7							bit
Legend:							
R = Readabl	le bit	W = Writable b	bit	U = Unimpler	nented bit, rea	ad as '0'	
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-14	Unimplemen	ted: Read as '0	,				
bit 13	SELACLK: S	elect Auxiliary (	Clock Source	for Auxiliary C	lock Divider		
	1 = Auxiliary	Oscillators provi	des the sour	ce clock for Au	xiliary Clock D	livider	
	0 = PLL outp	ut (Fosc) provid	es the source	e clock for the A	Auxiliary Clock	Divider	
bit 12-11	AOSCMD<1:	0>: Auxiliary Os	cillator Mode	9			
	11 = EC Exte	rnal Clock Mod	e Select				
		illator Mode Sele	ect				
		/ Oscillator Disa	bled				
bit 10-8	APSTSCLR<	2:0>: Auxiliary	Clock Output	t Divider			
	111 = divided	d by 1					
	110 = divideo	d by 2					
	101 = divideo	d by 4					
	100 <b>= divide</b>	by 8					
		1 by 16					
		1 Dy 32 1 by 64					
		d by 256 (defaul <sup>:</sup>	t)				
bit 7	ASRCSEL: S	Select Reference	, Clock Sour	ce for Auxiliarv	Clock		
	1 = Primarv C	Oscillator is the (	Clock Source	e	-		
	0 = Auxiliary	Oscillator is the	Clock Sourc	е			

# REGISTER 9-5: ACLKCON: AUXILIARY CONTROL REGISTER<sup>(1)</sup>

Note 1: This register is reset only on a Power-on Reset (POR).

Unimplemented: Read as '0'

bit 6-0

REGISTER	11-3: RPINF	R3: PERIPHE	RAL PIN SE	ELECT INPUT	REGISTER	3	
U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
_	—	_			T3CKR<4:0>	>	
bit 15							bit 8
11-0	11_0	11-0		D/\\/_1	D/\\/_1	D/\\/_1	P/\\/_1
0-0	0-0	0-0	1\/ VV-1	10/00-1		10.00-1	10.00-1
 bit 7		_			12000-4.02		bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimpler	mented bit, rea	d as '0'	
-n = Value a	It POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown
bit 15-13	Unimplemer	nted: Read as '	0'				
bit 12-8	T3CKR<4:0>	-: Assign Timer	3 External Cl	ock (T3CK) to t	he correspond	ing RPn pin	
	11111 <b>= Inp</b> i	ut tied to Vss					
	11001 <b>= Inp</b>	ut tied to RP25					
	•						
	•						
	•						
	00001 = Inpi 00000 = Inpi	ut tied to RP1 ut tied to RP0					
bit 7-5	Unimplemer	nted: Read as '	0'				

T2CKR<4:0>: Assign Timer2 External Clock (T2CK) to the corresponding RPn pin

bit 4-0

11111 = Input tied to Vss 11001 = Input tied to RP25

00001 = Input tied to RP1 00000 = Input tied to RP0

REGISTER 11-12:	<b>RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22</b>
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U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—				SCK2R<4:0	>	
bit 15							bit 8
U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
_		_			SDI2R<4:0	>	
bit 7	•	•					bit (
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-13	Unimpleme	nted: Read as '	0'				
bit 12-8	SCK2R<4:0	>: Assign SPI2	Clock Input (S	SCK2) to the co	prresponding F	RPn pin	
	11111 <b>= Ing</b>	out tied to Vss		,			
	11001 <b>= Inp</b>	out tied to RP25					
	•						
	•						
	•						
	00001 <b>= Inc</b>	out tied to RP1					
	00000 = Inp	out tied to RP0					
bit 7-5	Unimpleme	nted: Read as '	0'				
bit 4-0	SDI2R<4:0>	Assign SPI2 D	ata Input (SD	(2) to the corre	sponding RPr	n pin	
	11111 = Inr	ut tied to Vss	a.upat (02	) to the conc	iepenianig i i i	· P…	
	11001 <b>= Ing</b>	out tied to RP25					
	•						
	•						
	•						
	00001 <b>= Inr</b>	out tied to RP1					
	00000 = Inp	out tied to RP0					

# 14.2 Input Capture Registers

# **REGISTER 14-1:** ICxCON: INPUT CAPTURE x CONTROL REGISTER (x = 1, 2, 7 OR 8)

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	ICSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0
ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'				
bit 13	ICSIDL: Input Capture Module Stop in Idle Control bit				
	<ul> <li>1 = Input capture module halts in CPU Idle mode</li> <li>0 = Input capture module continues to operate in CPU Idle mode</li> </ul>				
bit 12-8	Unimplemented: Read as '0'				
bit 7	ICTMR: Input Capture Timer Select bits				
	<ul> <li>1 = TMR2 contents are captured on capture event</li> <li>0 = TMR3 contents are captured on capture event</li> </ul>				
bit 6-5	ICI<1:0>: Select Number of Captures per Interrupt bits				
	<ul> <li>11 = Interrupt on every fourth capture event</li> <li>10 = Interrupt on every third capture event</li> <li>01 = Interrupt on every second capture event</li> <li>00 = Interrupt on every capture event</li> </ul>				
bit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)				
	<ul> <li>1 = Input capture overflow occurred</li> <li>0 = No input capture overflow occurred</li> </ul>				
bit 3	ICBNE: Input Capture Buffer Empty Status bit (read-only)				
	<ul> <li>1 = Input capture buffer is not empty, at least one more capture value can be read</li> <li>0 = Input capture buffer is empty</li> </ul>				
bit 2-0	ICM<2:0>: Input Capture Mode Select bits				
	<ul> <li>111 = Input capture functions as interrupt pin only when device is in Sleep or Idle mode (Rising edge detect only, all other control bits are not applicable.)</li> <li>110 = Unused (module disabled)</li> <li>101 = Capture mode, every 16th rising edge</li> <li>100 = Capture mode, every 4th rising edge</li> <li>011 = Capture mode, every rising edge</li> <li>010 = Capture mode, every falling edge</li> <li>010 = Capture mode, every falling edge</li> <li>011 = Capture mode, every edge (rising and falling)</li> <li>(ICI&lt;1:0&gt; bits do not control interrupt generation for this mode.)</li> </ul>				
	000 = Input capture module turned off				

# 15.0 OUTPUT COMPARE

- This data sheet summarizes the features Note 1: of the dsPIC33FJ32GP302/304. dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 13. "Output Compare" (DS70209) of the "dsPIC33F/ PIC24H Family Reference Manual", which is available from the Microchip website (www.microchip.com).
  - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Output Compare module can select either Timer2 or Timer3 for its time base. The module compares the value of the timer with the value of one or two compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the compare register value. The Output Compare module generates either a single output pulse or a sequence of output pulses, by changing the state of the output pin on the compare match events. The Output Compare module can also generate interrupts on compare match events.

The Output Compare module has multiple operating modes:

- Active-Low One-Shot mode
- Active-High One-Shot mode
- Toggle mode
- · Delayed One-Shot mode
- Continuous Pulse mode
- PWM mode without Fault protection
- PWM mode with Fault protection

## FIGURE 15-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



NOTES:

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
48 MPY		MPY Wm*Wn,Acc,Wx,Wxd,Wy,Wyd		Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		MPY Wm*Wm,A	cc,Wx,Wxd,Wy,Wyd	Square Wm to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
49	MPY.N	MPY.N Wm*Wn,Acc,Wx,Wxd,Wy,Wyd		-(Multiply Wm by Wn) to Accumulator	1	1	None
50	MSC	MSC Wm*Wm, Acc, Wx, Wxd, Wy, Wyd , AWB		Multiply and Subtract from Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
51	MUL	MUL.SS	Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1	1	None
		MUL.SU	Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.US	Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.UU	Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.SU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.UU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL	f	W3:W2 = f * WREG	1	1	None
52	NEG	NEG	Acc	Negate Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		NEG	f	$f = \overline{f} + 1$	1	1	C,DC,N,OV,Z
		NEG	f,WREG	WREG = $\overline{f}$ + 1	1	1	C,DC,N,OV,Z
		NEG	Ws,Wd	$Wd = \overline{Ws} + 1$	1	1	C,DC,N,OV,Z
53	NOP	NOP		No Operation	1	1	None
		NOPR		No Operation	1	1	None
54	POP	POP	f	Pop f from Top-of-Stack (TOS)	1	1	None
		POP	Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
		POP.D	Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1)	1	2	None
		POP.S		Pop Shadow Registers	1	1	All
55	PUSH	PUSH	f	Push f to Top-of-Stack (TOS)	1	1	None
		PUSH	Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
		PUSH.D	Wns	Push W(ns):W(ns + 1) to Top-of-Stack (TOS)	1	2	None
		PUSH.S		Push Shadow Registers	1	1	None
56	PWRSAV	PWRSAV	#lit1	Go into Sleep or Idle mode	1	1	WDTO,Sleep
57	RCALL	RCALL	Expr	Relative Call	1	2	None
		RCALL	Wn	Computed Call	1	2	None
58	REPEAT	REPEAT	#lit14	Repeat Next Instruction lit14 + 1 times	1	1	None
		REPEAT	Wn	Repeat Next Instruction (Wn) + 1 times	1	1	None
59	RESET	RESET Software device Reset		Software device Reset	1	1	None
60	RETFIE	RETFIE Return from interrupt		1	3 (2)	None	
61	RETLW	RETLW	#lit10,Wn	Return with literal in Wn	1	3 (2)	None
62	RETURN	RETURN		Return from Subroutine	1	3 (2)	None
63	RLC	RLC	f	f = Rotate Left through Carry f	1	1	C,N,Z
		RLC	f,WREG	WREG = Rotate Left through Carry f	1	1	C,N,Z
		RLC	Ws,Wd	Wd = Rotate Lett through Carry Ws	1	1	C,N,Z
64	RLNC	RLNC	t	T = Rotate Lett (No Carry) f	1	1	N,Z
		RLNC	f,WREG	WREG = Rotate Lett (No Carry) f	1	1	N,Z
05		RLNC	Ws,Wd	wd = Rotate Lett (No Carry) Ws	1	1	N,Z
60	RRC	RRC	I E MDEC	I = Rotate Right through Carry f	1	1	C,N,Z
		RRC	I, WKEG	Wd = Pototo Pight through Carry Ma	1	1	
	1	KKC	ws,wa	wu - Rolate Right through Gally WS			U,IN,Z

# TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature-40°C ≤TA ≤+85°C for Industrial-40°C ≤TA ≤+125°C for Extended				
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	СКР	SMP	
15 MHz	Table 30-29	—	_	0,1	0,1	0,1	
9 MHz	_	Table 30-30	—	1	0,1	1	
9 MHz	_	Table 30-31	—	0	0,1	1	
15 MHz	_	—	Table 30-32	1	0	0	
11 MHz	_	—	Table 30-33	1	1	0	
15 MHz		_	Table 30-34	0	1	0	
11 MHz		_	Table 30-35	0	0	0	

#### TABLE 30-28: SPIX MAXIMUM DATA/CLOCK RATE SUMMARY

# FIGURE 30-9: SPIX MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY CKE = 0) TIMING CHARACTERISTICS



# FIGURE 30-10: SPIX MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY CKE = 1) TIMING CHARACTERISTICS



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AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)         Operating temperature       -40°C ≤TA ≤+150°C for High Temperature					
Param No.	Symbol	Characteristic	Min	Тур	Мах	Units	Conditions
	AD	C Accuracy (10-bit Mode)	– Measu	rements	with Ex	ternal V	REF+/VREF- <sup>(1)</sup>
HAD20b	Nr	Resolution <sup>(3)</sup>	1	0 data bi	ts	bits	—
HAD21b	INL	Integral Nonlinearity	-3	—	3	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
HAD22b	DNL	Differential Nonlinearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
HAD23b	Gerr	Gain Error	-5	—	6	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
HAD24b	EOFF	Offset Error	-1	—	5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
ADC Accuracy (10-bit Mode) – Measurements with Internal VREF+/VREF- <sup>(1)</sup>							
HAD20b	Nr	Resolution <sup>(3)</sup>	1	0 data bi	ts	bits	_
HAD21b	INL	Integral Nonlinearity	-2	_	2	LSb	VINL = AVSS = 0V, AVDD = 3.6V
HAD22b	DNL	Differential Nonlinearity	> -1		< 1	LSb	VINL = AVSS = 0V, AVDD = 3.6V
HAD23b	Gerr	Gain Error	-5	_	15	LSb	VINL = AVSS = 0V, AVDD = 3.6V
HAD24b	EOFF	Offset Error	-1.5	—	7	LSb	VINL = AVSS = 0V, AVDD = 3.6V
Dynamic Performance (10-bit Mode) <sup>(2)</sup>							
HAD33b	FNYQ	Input Signal Bandwidth	_	_	400	kHz	_

# TABLE 31-16: ADC MODULE SPECIFICATIONS (10-BIT MODE)

**Note 1:** These parameters are characterized, but are tested at 20 ksps only.

**2:** These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



# RECOMMENDED LAND PATTERN

	N	<b>ILLIMETER</b>	S	
Dimension Limits		MIN	NOM	MAX
Contact Pitch E			0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing			11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

## Revision F (August 2011)

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in the following table.

### TABLE A-5: MAJOR SECTION UPDATES

Section Name	Update Description
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers"	Updated the Recommendation Minimum Connection (see Figure 2-1).
Section 27.0 "Special Features"	Added Note 3 to the Connections for the On-chip Voltage Regulator diagram (see Figure 27-1).
Section 30.0 "Electrical Characteristics"	Removed Voltage on VCAP with respect to Vss from the Absolute Maximum Ratings.
	Removed Note 3 and parameter DC10 (VCORE) from the DC Temperature and Voltage Specifications (see Table 30-4).
	Updated the Characteristics definition and Conditions for parameter BO10 in the Electrical Characteristics: BOR (see Table 30-11).
	Added Note 1 to the Internal Voltage Regulator Specifications (see Table 30-13).

## **Revision G (April 2012)**

This revision includes typographical and formatting changes throughout the data sheet text.

In addition, where applicable, new sections were added to each peripheral chapter that provide information and links to related resources, as well as helpful tips. For examples, see Section 9.2 "Oscillator Resources" and Section 21.4 "ADC Helpful Tips".

All other major changes are referenced by their respective section in the following table.

#### TABLE A-6: MAJOR SECTION UPDATES

Section Name	Update Description
Section 2.0 "Guidelines for Getting Started	Added two new tables:
with 16-bit Digital Signal Controllers"	<ul> <li>Crystal Recommendations (see Table 2-1)</li> </ul>
	<ul> <li>Resonator Recommendations (see Table 2-2)</li> </ul>
Section 30.0 "Electrical Characteristics"	Updated parameters DO10 and DO20 and removed parameters DO16 and DO26 in the DC Characteristics: I/O Pin Output Specifications (see Table 30-10)