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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, Microwire, MMC/SD, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	83
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc18s10fbd144e

- Up to 164 General-Purpose Input/Output (GPIO) pins with configurable pull-up/pull-down resistors.
- GPIO registers are located on the AHB for fast access. GPIO ports have DMA support.
- Up to eight GPIO pins can be selected from all GPIO pins as edge and level sensitive interrupt sources.
- Two GPIO group interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
- Four general-purpose timer/counters with capture and match capabilities.
- One motor control PWM for three-phase motor control.
- One Quadrature Encoder Interface (QEI).
- Repetitive Interrupt timer (RI timer).
- Windowed watchdog timer.
- Ultra-low power Real-Time Clock (RTC) on separate power domain with 256 bytes of battery powered backup registers.
- Alarm timer; can be battery powered.

- Analog peripherals:
  - One 10-bit DAC with DMA support and a data conversion rate of 400 kSamples/s.
  - Two 10-bit ADCs with DMA support and a data conversion rate of 400 kSamples/s. Up to eight input channels per ADC.
- Unique ID for each device.
- Power:
  - Single 3.3 V (2.2 V to 3.6 V) power supply with on-chip internal voltage regulator for the core supply and the RTC power domain.
  - RTC power domain can be powered separately by a 3 V battery supply.
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Processor wake-up from Sleep mode via wake-up interrupts from various peripherals.
  - Wake-up from Deep-sleep, Power-down, and Deep power-down modes via external interrupts and interrupts generated by battery powered blocks in the RTC power domain.
  - Brownout detect with four separate thresholds for interrupt and forced reset.
  - Power-On Reset (POR).
- Available as 144-pin LQFP packages and as 256-pin, 180-pin, and 100-pin BGA packages.

3. Applications

- Communication hubs
- Automotive aftermarket
- Power management
- Consumer health devices
- Embedded audio applications
- Industrial control
- Industrial automation
- white goods

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Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P1_5	R5	N3	J4	48	[2]	N; PU	I/O	**GPIO1[8] —** General purpose digital input/output pin.
							O	**CTOUT_10 —** SCTimer/PWM output 10. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC_CS0}}$ —** LOW active Chip Select 0 signal.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							-	**R —** Function reserved.
							O	**SD_POW —** SD/MMC card power monitor output.
P1_6	T4	P3	K4	49	[2]	N; PU	I/O	**GPIO1[9] —** General purpose digital input/output pin.
							I	**CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC_WE}}$ —** LOW active Write Enable signal.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_CMD —** SD/MMC command signal.
P1_7	T5	N4	G4	50	[2]	N; PU	I/O	**GPIO1[0] —** General purpose digital input/output pin.
							I	**U1_DSR —** Data Set Ready input for UART1.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							I/O	**EMC_D0 —** External memory data line 0.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the $\overline{\text{USB_PPWR}}$ used on other NXP LPC parts.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

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Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P6_6	L14	K12	-	83	[2]	N; PU	I/O	**GPIO0[5] —** General purpose digital input/output pin.
							O	**$\overline{\text{EMC_BLS1}}$ —** LOW active Byte Lane select signal 1.
							-	**R —** Function reserved.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							-	**R —** Function reserved.
							I	**T2_CAP3 —** Capture input 3 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_7	J13	H11	-	85	[2]	N; PU	-	**R —** Function reserved.
							I/O	**EMC_A15 —** External memory address line 15.
							-	**R —** Function reserved.
							O	**USB0_IND1 —** USB0 port indicator LED control output 1.
							I/O	**GPIO5[15] —** General purpose digital input/output pin.
							O	**T2_MAT0 —** Match output 0 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_8	H13	F12	-	86	[2]	N; PU	-	**R —** Function reserved.
							I/O	**EMC_A14 —** External memory address line 14.
							-	**R —** Function reserved.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
							I/O	**GPIO5[16] —** General purpose digital input/output pin.
							O	**T2_MAT1 —** Match output 1 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_9	J15	H13	F8	97	[2]	N; PU	I/O	**GPIO3[5] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC_DYCS0}}$ —** SDRAM chip select 0.
							-	**R —** Function reserved.
							O	**T2_MAT2 —** Match output 2 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

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Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PD_16	R14	P12	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A16 —** External memory address line 16.
							-	**R —** Function reserved.
							I/O	**GPIO6[30] —** General purpose digital input/output pin.
							O	**SD_VOLT2 —** SD/MMC bus voltage select output 2.
							O	**CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3.
							-	**R —** Function reserved.
PE_0	P14	N12	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A18 —** External memory address line 18.
							I/O	**GPIO7[0] —** General purpose digital input/output pin.
							O	**CAN1_TD —** CAN1 transmitter output.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_1	N14	M12	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A19 —** External memory address line 19.
							I/O	**GPIO7[1] —** General purpose digital input/output pin.
							I	**CAN1_RD —** CAN1 receiver input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_2	M14	L12	-	-	[2]	N; PU	I	**ADCTRIG0 —** ADC trigger input 0.
							I	**CAN0_RD —** CAN receiver input.
							-	**R —** Function reserved.
							I/O	**EMC_A20 —** External memory address line 20.
							I/O	**GPIO7[2] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

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Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PE_15	E13	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_0 —** SCTimer/PWM output 0. Match output 0 of timer 0.
							I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
							O	**EMC_CKEOUT3 —** SDRAM clock enable 3.
							I/O	**GPIO7[15] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PF_0	D12	-	-	-	[2]	OL; PU	I/O	**SSP0_SCK —** Serial clock for SSP0.
							I	**GP_CLKIN —** General-purpose clock input to the CGU.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**I2S1_TX_MCLK —** I^2S1 transmit master clock.
PF_1	E11	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							-	**R —** Function reserved.
							I/O	**GPIO7[16] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PF_2	D11	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**U3_TXD —** Transmitter output for USART3.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							-	**R —** Function reserved.
							I/O	**GPIO7[17] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

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Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
Clock pins								
CLK0	N5	M4	K3	45	[4]	O; PU	O	**EMC_CLK0 —** SDRAM clock 0.
							O	**CLKOUT —** Clock output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_CLK —** SD/MMC card clock.
							O	**EMC_CLK01 —** SDRAM clock 0 and clock 1 combined.
							I/O	**SSP1_SCK —** Serial clock for SSP1.
							I	**ENET_TX_CLK (ENET_REF_CLK) —** Ethernet Transmit Clock (MII interface) or Ethernet Reference Clock (RMII interface).
CLK1	T10	-	-	-	[4]	O; PU	O	**EMC_CLK1 —** SDRAM clock 1.
							O	**CLKOUT —** Clock output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**CGU_OUT0 —** CGU spare clock output 0.
							-	**R —** Function reserved.
							O	**I2S1_TX_MCLK —** I^2S1 transmit master clock.
CLK2	D14	P10	K6	99	[4]	O; PU	O	**EMC_CLK3 —** SDRAM clock 3.
							O	**CLKOUT —** Clock output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_CLK —** SD/MMC card clock.
							O	**EMC_CLK23 —** SDRAM clock 2 and clock 3 combined.
							O	**I2S0_TX_MCLK —** I^2S transmit master clock.
							I/O	**I2S1_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
CLK3	P12	-	-	-	[4]	O; PU	O	**EMC_CLK2 —** SDRAM clock 2.
							O	**CLKOUT —** Clock output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**CGU_OUT1 —** CGU spare clock output 1.
							-	**R —** Function reserved.
							I/O	**I2S1_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.

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7. Functional description

7.1 Architectural overview

The ARM Cortex-M3 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus. The I-code and D-code core buses allow for concurrent code and data accesses from different slave ports.

The LPC18S50/S30/S10 use a multi-layer AHB matrix to connect the ARM Cortex-M3 buses and other bus masters to peripherals. Flexible connections allow different bus masters to access peripherals that are on different slave ports of the matrix simultaneously.

7.2 ARM Cortex-M3 processor

The ARM Cortex-M3 is a general purpose, 32-bit microprocessor, which offers high performance and low-power consumption. The ARM Cortex-M3 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware division, hardware single-cycle multiply, interruptable/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM Cortex-M3 processor is described in detail in the Cortex-M3 Technical Reference Manual.

7.3 System Tick timer (SysTick)

The ARM Cortex-M3 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval.

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7.14.1.1 Features

- Maximum UART data bit rate of 8 MBit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).
- Support for RS-485/9-bit/EIA-485 mode (UART1).
- DMA support.

7.14.2 USART

Remark: The LPC18S50/S30/S10 contain three USARTs. In addition to standard transmit and receive data lines, the USARTs support a synchronous mode and a smart card mode.

The USARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.14.2.1 Features

- Maximum UART data bit rate of 8 MBit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit/EIA-485 mode.
- USART3 includes an IrDA mode to support infrared communication.
- All USARTs have DMA support.
- Support for synchronous mode at a data bit rate of up to 8 Mbit/s.
- Smart card mode conforming to ISO7816 specification

7.14.3 SSP serial I/O controller

Remark: The LPC18S50/S30/S10 contain two SSP controllers.

The SSP controller can operate on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full-duplex

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- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position-compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clk and direction).

7.15.4 Repetitive Interrupt (RI) timer

The repetitive interrupt timer provides a free-running 32-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer compare function can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

7.15.4.1 Features

- 32-bit counter. Counter can be free-running or be reset by a generated interrupt.
- 32-bit compare value.
- 32-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This mechanism allows for combinations not possible with a simple compare.

7.15.5 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.15.5.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.

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- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) uses the IRC as the clock source.

7.16 Analog peripherals

7.16.1 Analog-to-Digital Converter

Remark: The LPC18S50/S30/S10 contain two 10-bit ADCs.

7.16.1.1 Features

- 10-bit successive approximation analog to digital converter.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 to VDDA.
- Sampling frequency up to 400 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on ADCTRIG0 or ADCTRIG1 pins, combined timer outputs 8 or 15, or the PWM output MCOA2.
- Individual result registers for each A/D channel to reduce interrupt overhead.
- DMA support.

7.16.2 Digital-to-Analog Converter (DAC)

7.16.2.1 Features

- 10-bit resolution
- Monotonic by design (resistor string architecture)
- Controllable conversion speed
- Low-power consumption

7.17 Peripherals in the RTC power domain

7.17.1 RTC

The Real-Time Clock (RTC) is a set of counters for measuring time when system power is on, and optionally when it is off. It uses little power when the CPU does not access its registers, especially in the reduced power modes. A separate 32 kHz oscillator clocks the RTC. The oscillator produces a 1 Hz internal time reference and is powered by its own power supply pin, VBAT.

7.17.1.1 Features

- Measures the passage of time to maintain a calendar and clock. Provides seconds, minutes, hours, day of month, month, year, day of week, and day of year.
- Ultra-low power design to support battery powered systems. Uses power from the CPU power supply when it is present.
- Dedicated battery power supply pin.

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11.15 SD/MMC

Table 30. Dynamic characteristics: SD/MMC

T_{amb} = −40 °C to 85 °C, 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V, C_L = 20 pF. SAMPLE_DELAY = 0x9, DRV_DELAY = 0xD in the SDDELAY register sampled at 90 % and 10 % of the signal level, EHS = 1 for SD_CLK pin, EHS = 1 for SD_DATn and SD_CMD pins. Simulated values.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode		52	MHz
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs	3.9	-	ns
		on pins SD_CMD as inputs	5.2	-	ns
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs	0.4	-	ns
		on pins SD_CMD as inputs	0		ns
$t_{d(QV)}$	data output valid delay time	on pins SD_DATn as outputs	-	15.3	ns
		on pins SD_CMD as outputs	-	16	ns
$t_{h(Q)}$	data output hold time	on pins SD_DATn as outputs	4	-	ns
		on pins SD_CMD as outputs	4	-	ns

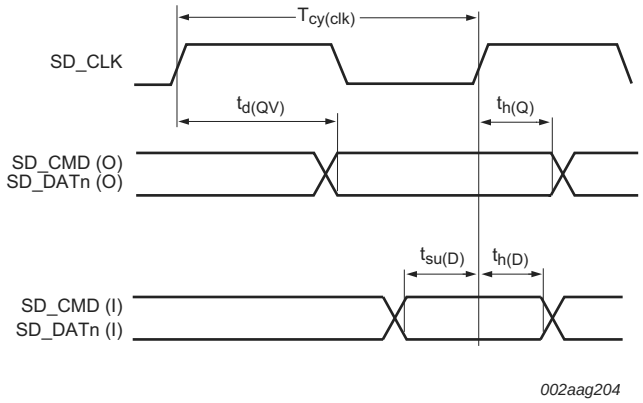

Fig 37. SD/MMC timing

11.16 LCD

Table 31. Dynamic characteristics: LCD

T_{amb} = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Simulated values.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	on pin LCD_DCLK	-	50	-	MHz
$t_{d(QV)}$	data output valid delay time			-	17	ns
$t_{h(Q)}$	data output hold time		8.5	-		ns

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12. ADC/DAC electrical characteristics

Table 33. ADC characteristics

$V_{DDA(3V3)}$ over specified ranges; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	$V_{DDA(3V3)}$	V
C_{ia}	analog input capacitance			-	-	2	pF
E_D	differential linearity error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1][2]	-	±0.8	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	LSB
$E_{L(adj)}$	integral non-linearity	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[3]	-	±0.8	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.5	-	LSB
E_O	offset error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[4]	-	±0.15	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±0.15	-	LSB
E_G	gain error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[5]	-	±0.3	-	%
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±0.35	-	%
E_T	absolute error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[6]	-	±3	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±4	-	LSB
R_{vsi}	voltage source interface resistance	see Figure 40		-	-	$1/(7 \times f_{clk(ADC)} \times C_{ia})$	kΩ
R_i	input resistance		[7][8]	-	-	1.2	MΩ
$f_{clk(ADC)}$	ADC clock frequency			-	-	4.5	MHz
f_s	sampling frequency	10-bit resolution; 11 clock cycles		-	-	400	kSamples/s
		2-bit resolution; 3 clock cycles				1.5	MSamples/s

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 39.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 39.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 39.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 39.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 39.

[7] T_{amb} = 25 °C.

[8] Input resistance R_i depends on the sampling frequency fs: $R_i = 2\ k\Omega + 1 / (f_s \times C_{ia})$.

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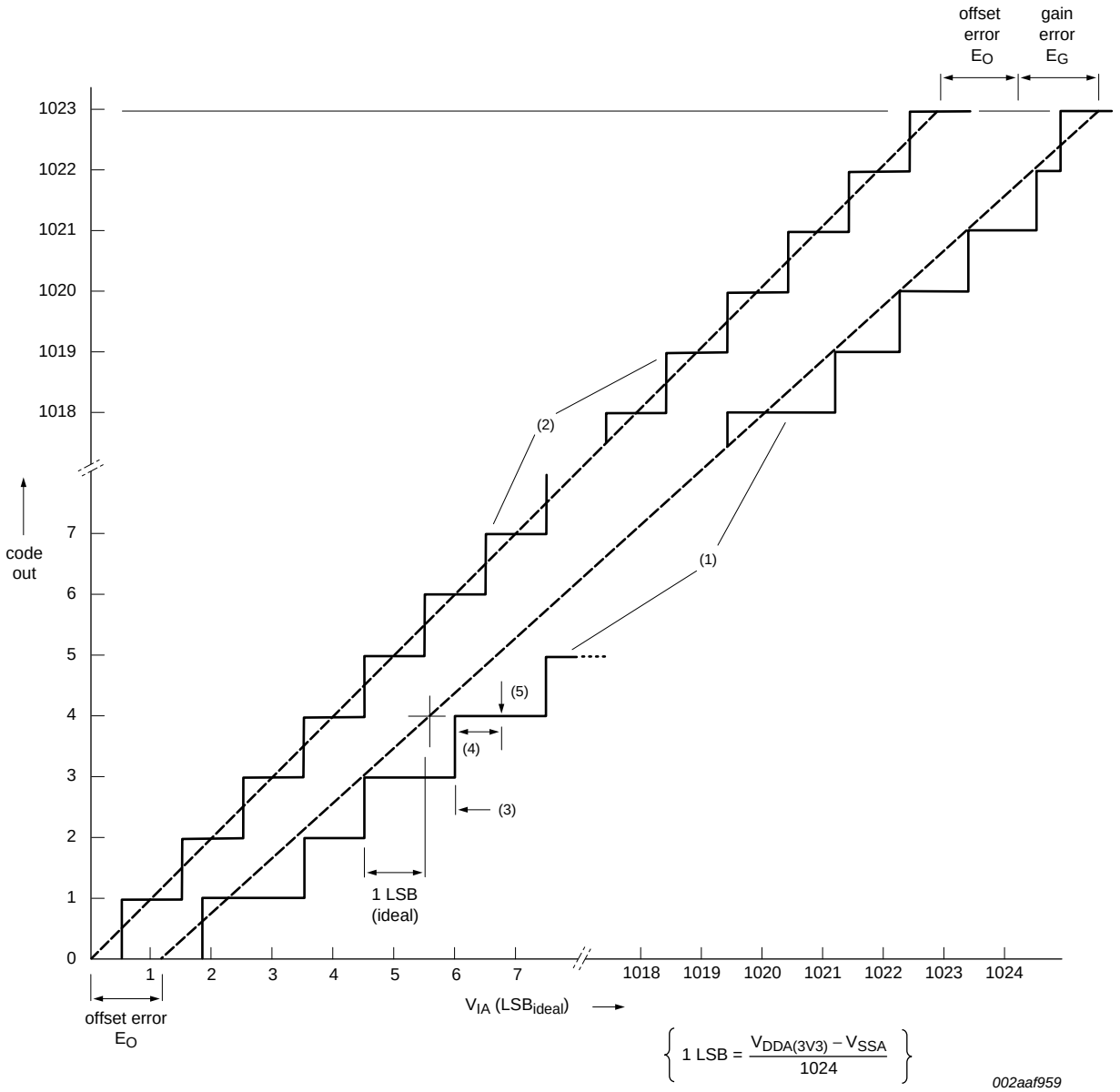

(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 39. 10-bit ADC characteristics

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On the LPC18S50/S30/S10, USBn_VBUS pins are 5 V tolerant only when VDDIO is applied and at operating voltage level. Therefore, if the USBn_VBUS function is connected to the USB connector and the device is self-powered, the USBn_VBUS pins must be protected for situations when VDDIO = 0 V.

If VDDIO is always at operating level while VBUS = 5 V, the USBn_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where VDDIO can be 0 V and VBUS is directly applied to the USBn_VBUS pins, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USBn_VBUS pins in this case.

One method is to use a voltage divider to connect the USBn_VBUS pins to VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin will be greater than 0.7VDDIO to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

$VBUS_{max}$ = 5.25 V

VDDIO = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

For bus-powered devices, a regulator powered by USB can provide 3.3 V to VDDIO whenever bus power is present and ensure that power to the USBn_VBUS pins is always present when the 5 V VBUS signal is applied. See Figure 47.

Remark: Applying 5 V to the USBn_VBUS pins for a short time while the regulator ramps up might compromise the long-term reliability of the part but does not affect its function.

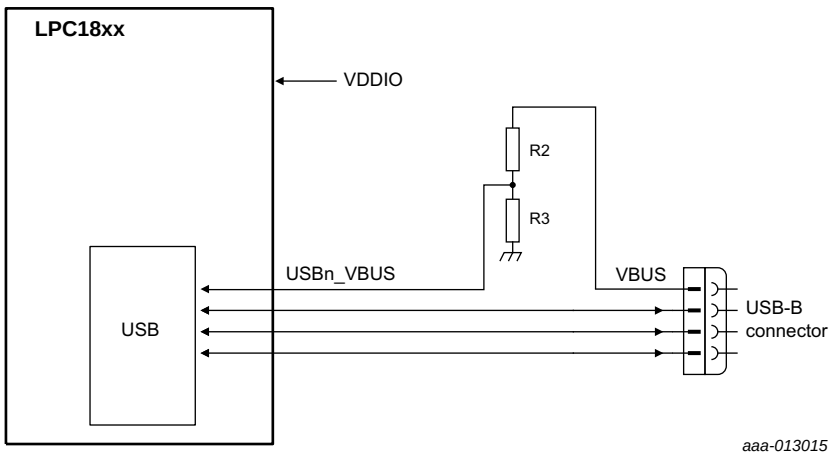

Fig 46. USB interface on a self-powered device where USBn_VBUS = 5 V

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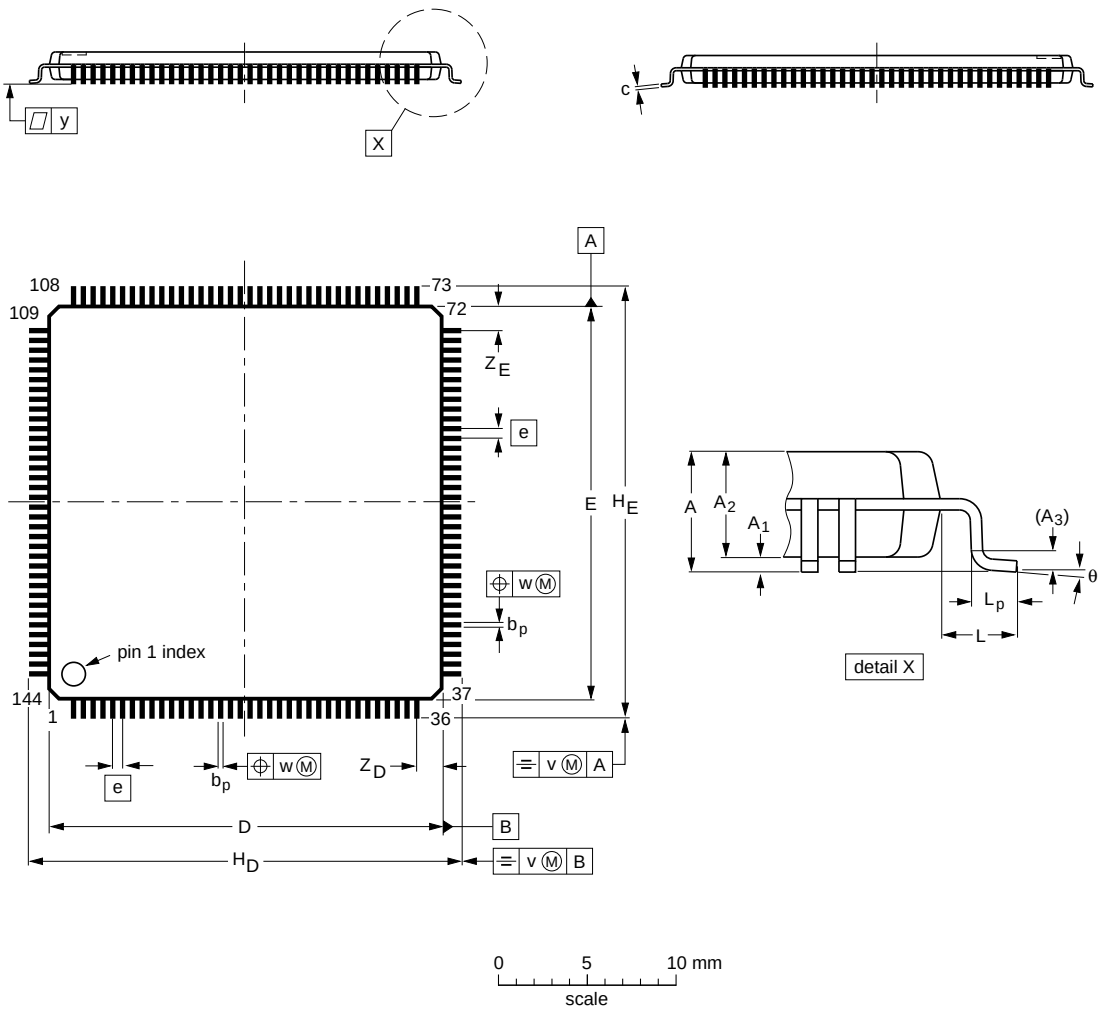
LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 52. Package outline for the LQFP144 package

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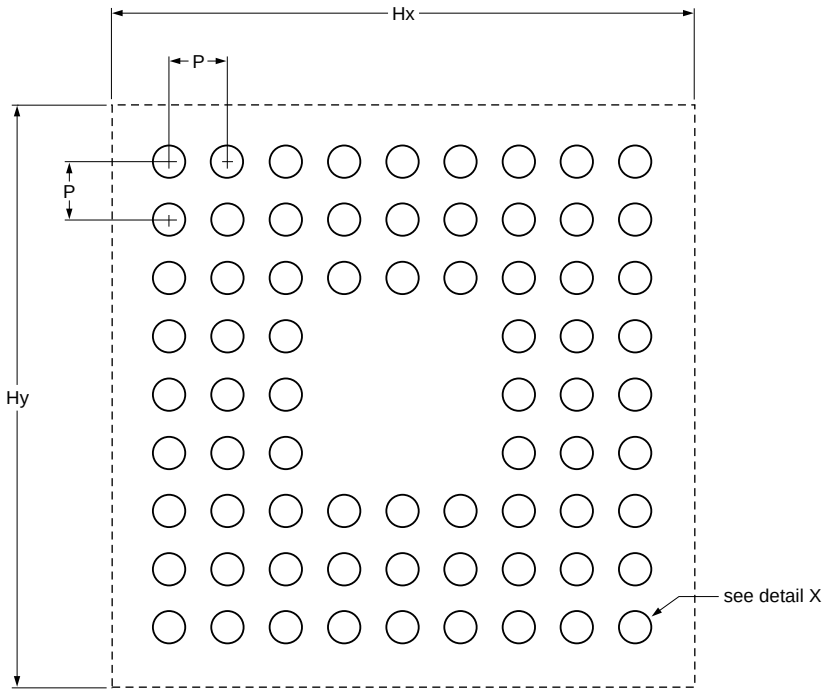
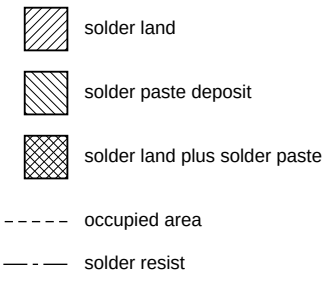
15. Soldering

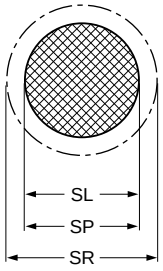
Footprint information for reflow soldering of LBGA256 package **SOT740-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout





detail X

DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
1.00	0.450	0.450	0.600	17.500	17.500

sot740-2_fr

Fig 53. Reflow soldering of the LBGA256 package

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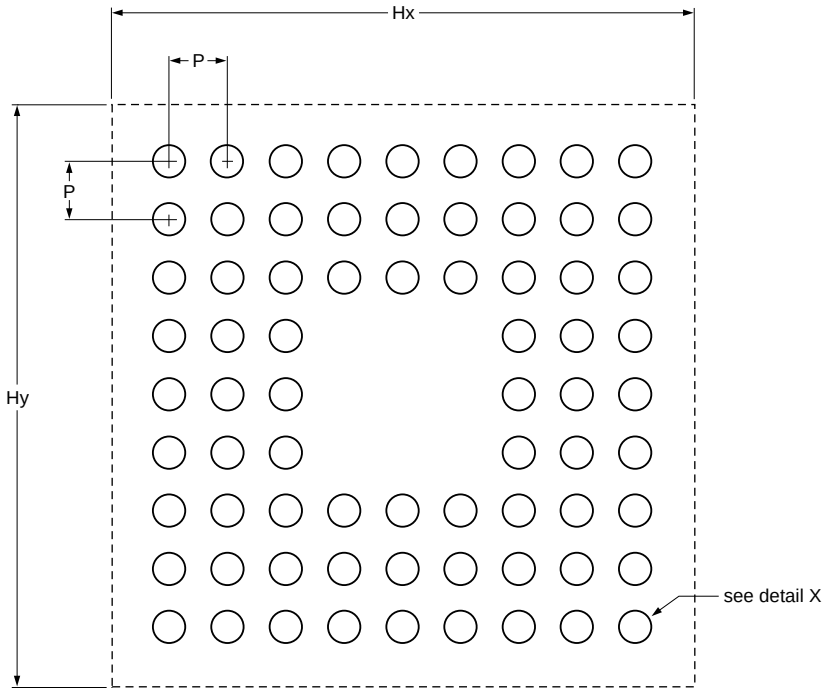
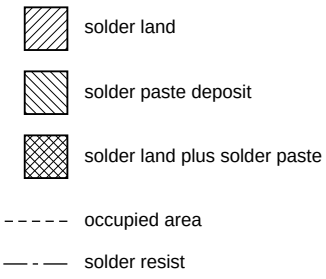
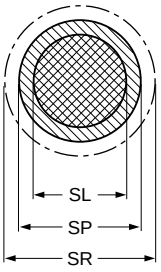
Footprint information for reflow soldering of TFBGA100 package **SOT926-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout





detail X

DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
0.80	0.330	0.400	0.480	9.400	9.400

sot926-1_fr

Fig 56. Reflow soldering of the TFBGA100 package

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16. Abbreviations

Table 40. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
BOD	BrownOut Detection
BGA	Ball Grid Array
CAN	Controller Area Network
CMAC	Cipher-based Message Authentication Code
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
EOP	End Of Packet
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macrocell
GPIO	General-Purpose Input/Output
IRC	Internal RC
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LQFP	Low Quad Flat Package
MAC	Media Access Control
MCU	MicroController Unit
MIIM	Media Independent Interface Management
n.c.	not connected
OTG	On-The-Go
PHY	PHYsical layer
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RMII	Reduced Media Independent Interface
SDRAM	Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TCP/IP	Transmission Control Protocol/Internet Protocol
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface

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Table 40. Abbreviations *…continued*

Acronym	Description
USART	Universal Synchronous Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
UTMI	USB 2.0 Transceiver Macrocell Interface

17. References

[1] LPC18xx User manual UM10430: http://www.nxp.com/documents/user_manual/UM10430.pdf

[2] LPC18SX0 Errata sheet

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18. Revision history

Table 41. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC18S50_S30_S10 v.1.2	20160303	Product data sheet	-	LPC18S50_S30_S10 v.1.1
	• Updated Table 25 “Dynamic characteristics: Dynamic external memory interface”: Read cycle parameters $t_{h(D)}$ min value is 2.2 ns and max value is “-”.			
LPC18S50_S30_S10 v.1.1	20151116	Product data sheet	2015110031	LPC18S50_S30_S10 v.1.0
Modifications:	• Updated SSP slave and SSP master values in Table 23 “Dynamic characteristics: SSP pins in SPI mode”. Updated footnote 2 to: $T_{cy(clk)} \geq 12 \times T_{cy(PCLK)}$. – removed $t_{v(Q)}$, data output valid time in SPI mode, minimum value of 3 ´ (1/PCLK) from SSP slave mode. – added units to t_d, delay time, for SSP slave and master mode. • Added GPCLKIN section and table. See Section 11.6 “GPCLKIN” and Table 18 “Dynamic characteristic: GPCLKIN”.			
LPC18S50_S30_S10 v.1.0	20150210	Product data sheet	-	-

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