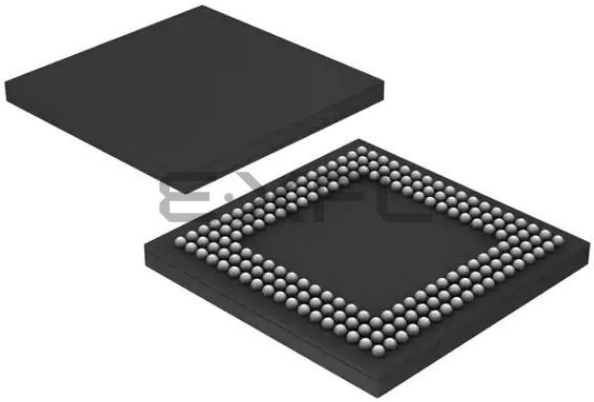

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, QEI, MMC/SD, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	118
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc18s50fet180e

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P1_8	R7	M5	H5	51	[2]	N; PU	I/O	**GPIO1[1] —** General purpose digital input/output pin.
							O	**U1_DTR —** Data Terminal Ready output for UART1.
							O	**CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3.
							I/O	**EMC_D1 —** External memory data line 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**SD_VOLT0 —** SD/MMC bus voltage select output 0.
P1_9	T7	N5	J5	52	[2]	N; PU	I/O	**GPIO1[2] —** General purpose digital input/output pin.
							O	**U1_RTS —** Request to Send output for UART1.
							O	**CTOUT_11 —** SCTimer/PWM output 11. Match output 3 of timer 2.
							I/O	**EMC_D2 —** External memory data line 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_DAT0 —** SD/MMC data bus line 0.
P1_10	R8	N6	H6	53	[2]	N; PU	I/O	**GPIO1[3] —** General purpose digital input/output pin.
							I	**U1_RI —** Ring Indicator input for UART1.
							O	**CTOUT_14 —** SCTimer/PWM output 14. Match output 2 of timer 3.
							I/O	**EMC_D3 —** External memory data line 3.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_DAT1 —** SD/MMC data bus line 1.
P1_11	T9	P8	J7	55	[2]	N; PU	I/O	**GPIO1[4] —** General purpose digital input/output pin.
							I	**U1_CTS —** Clear to Send input for UART1.
							O	**CTOUT_15 —** SCTimer/PWM output 15. Match output 3 of timer 3.
							I/O	**EMC_D4 —** External memory data line 4.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_DAT2 —** SD/MMC data bus line 2.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P2_12	E15	D13	B9	106	[2]	N; PU	I/O	**GPIO1[12] —** General purpose digital input/output pin.
							O	**CTOUT_4 —** SCTimer/PWM output 4. Match output 3 of timer 3.
							-	**R —** Function reserved.
							I/O	**EMC_A3 —** External memory address line 3.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**U2_UCLK —** Serial clock input/output for USART2 in synchronous mode.
P2_13	C16	E14	A10	108	[2]	N; PU	I/O	**GPIO1[13] —** General purpose digital input/output pin.
							I	**CTIN_4 —** SCTimer/PWM input 4. Capture input 2 of timer 1.
							-	**R —** Function reserved.
							I/O	**EMC_A4 —** External memory address line 4.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**U2_DIR —** RS-485/EIA-485 output enable/direction control for USART2.
P3_0	F13	D12	A8	112	[2]	N; PU	I/O	**I2S0_RX_SCK —** I^2S receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							O	**I2S0_RX_MCLK —** I^2S receive master clock.
							I/O	**I2S0_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
							O	**I2S0_TX_MCLK —** I^2S transmit master clock.
							I/O	**SSP0_SCK —** Serial clock for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P4_6	C1	B1	-	11	[2]	N; PU	I/O	**GPIO2[6] —** General purpose digital input/output pin.
							O	**CTOUT_4 —** SCTimer/PWM output 4. Match output 3 of timer 3.
							O	**LCD_ENAB/LCDM —** STN AC bias drive or TFT data enable input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P4_7	H4	F4	-	14	[2]	O; PU	O	**LCD_DCLK —** LCD panel clock.
							I	**GP_CLKIN —** General-purpose clock input to the CGU.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
							I/O	**I2S0_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
P4_8	E2	D2	-	15	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2.
							O	**LCD_VD9 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[12] —** General purpose digital input/output pin.
							O	**LCD_VD22 —** LCD data.
							O	**CAN1_TD —** CAN1 transmitter output.
							-	**R —** Function reserved.
P4_9	L2	J2	-	33	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3.
							O	**LCD_VD11 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[13] —** General purpose digital input/output pin.
							O	**LCD_VD15 —** LCD data.
							I	**CAN1_RD —** CAN1 receiver input.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P4_10	M3	L3	-	35	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_2 —** SCTimer/PWM input 2. Capture input 2 of timer 0.
							O	**LCD_VD10 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[14] —** General purpose digital input/output pin.
							O	**LCD_VD14 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_0	N3	L2	-	37	[2]	N; PU	I/O	**GPIO2[9] —** General purpose digital input/output pin.
							O	**MCOB2 —** Motor control PWM channel 2, output B.
							I/O	**EMC_D12 —** External memory data line 12.
							-	**R —** Function reserved.
							I	**U1_DSR —** Data Set Ready input for UART1.
							I	**T1_CAP0 —** Capture input 0 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_1	P3	M1	-	39	[2]	N; PU	I/O	**GPIO2[10] —** General purpose digital input/output pin.
							I	**MCI2 —** Motor control PWM channel 2, input.
							I/O	**EMC_D13 —** External memory data line 13.
							-	**R —** Function reserved.
							O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							I	**T1_CAP1 —** Capture input 1 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_2	R4	M3	-	46	[2]	N; PU	I/O	**GPIO2[11] —** General purpose digital input/output pin.
							I	**MCI1 —** Motor control PWM channel 1, input.
							I/O	**EMC_D14 —** External memory data line 14.
							-	**R —** Function reserved.
							O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							I	**T1_CAP2 —** Capture input 2 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P7_4	C8	C6	-	132	[5]	N; PU	I/O	**GPIO3[12] —** General purpose digital input/output pin.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**LCD_VD16 —** LCD data.
							O	**LCD_VD4 —** LCD data.
							O	**TRACEDATA[0] —** Trace data, bit 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC0_4 —** ADC0 and ADC1, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P7_5	A7	A7	-	133	[5]	N; PU	I/O	**GPIO3[13] —** General purpose digital input/output pin.
							O	**CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**LCD_VD8 —** LCD data.
							O	**LCD_VD23 —** LCD data.
							O	**TRACEDATA[1] —** Trace data, bit 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC0_3 —** ADC0 and ADC1, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P7_6	C7	F5	-	134	[2]	N; PU	I/O	**GPIO3[14] —** General purpose digital input/output pin.
							O	**CTOUT_11 —** SCTimer/PWM output 1. Match output 3 of timer 2.
							-	**R —** Function reserved.
							O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
							-	**R —** Function reserved.
							O	**TRACEDATA[2] —** Trace data, bit 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P7_7	B6	D5	-	140	[5]	N; PU	I/O	**GPIO3[15] —** General purpose digital input/output pin.
							O	**CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2.
							-	**R —** Function reserved.
							O	**LCD_PWR —** LCD panel power enable.
							-	**R —** Function reserved.
							O	**TRACEDATA[3] —** Trace data, bit 3.
							O	**ENET_MDC —** Ethernet MIIM clock.
							-	**R —** Function reserved.
							AI	**ADC1_6 —** ADC1 and ADC0, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P8_0	E5	E4	-	-	[3]	N; PU	I/O	**GPIO4[0] —** General purpose digital input/output pin.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							-	**R —** Function reserved.
							I	**MCI2 —** Motor control PWM channel 2, input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T0_MAT0 —** Match output 0 of timer 0.
P8_1	H5	G4	-	-	[3]	N; PU	I/O	**GPIO4[1] —** General purpose digital input/output pin.
							O	**USB0_IND1 —** USB0 port indicator LED control output 1.
							-	**R —** Function reserved.
							I	**MCI1 —** Motor control PWM channel 1, input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T0_MAT1 —** Match output 1 of timer 0.
P8_2	K4	J4	-	-	[3]	N; PU	I/O	**GPIO4[2] —** General purpose digital input/output pin.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
							-	**R —** Function reserved.
							I	**MCI0 —** Motor control PWM channel 0, input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T0_MAT2 —** Match output 2 of timer 0.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PB_6	A6	C5	-	-	[5]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D3 —** ULPI link bidirectional data line 3.
							O	**LCD_VD13 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[26] —** General purpose digital input/output pin.
							I	**CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3.
							O	**LCD_VD19 —** LCD data.
							-	**R —** Function reserved.
							AI	**ADC0_6 —** ADC0 and ADC1, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PC_0	D4	-	-	-	[5]	N; PU	-	**R —** Function reserved.
							I	**USB1_ULPI_CLK —** ULPI link CLK signal. 60 MHz clock generated by the PHY.
							-	**R —** Function reserved.
							I/O	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface).
							O	**LCD_DCLK —** LCD panel clock.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_CLK —** SD/MMC card clock.
							AI	**ADC1_1 —** ADC1 and ADC0, input channel 1. Configure the pin as input (USB_ULPI_CLK) and use the ADC function select register in the SCU to select the ADC.
PC_1	E4	-	-	-	[2]	N; PU	I/O	**USB1_ULPI_D7 —** ULPI link bidirectional data line 7.
							-	**R —** Function reserved.
							I	**U1_RI —** Ring Indicator input for UART1.
							O	**ENET_MDC —** Ethernet MIIM clock.
							I/O	**GPIO6[0] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP0 —** Capture input 0 of timer 3.
							O	**SD_VOLT0 —** SD/MMC bus voltage select output 0.
PC_2	F6	-	-	-	[2]	N; PU	I/O	**USB1_ULPI_D6 —** ULPI link bidirectional data line 6.
							-	**R —** Function reserved.
							I	**U1_CTS —** Clear to Send input for UART1.
							O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
							I/O	**GPIO6[1] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**SD_RST —** SD/MMC reset signal for MMC4.4 card.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PD_16	R14	P12	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A16 —** External memory address line 16.
							-	**R —** Function reserved.
							I/O	**GPIO6[30] —** General purpose digital input/output pin.
							O	**SD_VOLT2 —** SD/MMC bus voltage select output 2.
							O	**CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3.
							-	**R —** Function reserved.
PE_0	P14	N12	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A18 —** External memory address line 18.
							I/O	**GPIO7[0] —** General purpose digital input/output pin.
							O	**CAN1_TD —** CAN1 transmitter output.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_1	N14	M12	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A19 —** External memory address line 19.
							I/O	**GPIO7[1] —** General purpose digital input/output pin.
							I	**CAN1_RD —** CAN1 receiver input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_2	M14	L12	-	-	[2]	N; PU	I	**ADCTRIG0 —** ADC trigger input 0.
							I	**CAN0_RD —** CAN receiver input.
							-	**R —** Function reserved.
							I/O	**EMC_A20 —** External memory address line 20.
							I/O	**GPIO7[2] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PE_3	K12	K10	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CAN0_TD —** CAN transmitter output.
							I	**ADCTRIG1 —** ADC trigger input 1.
							I/O	**EMC_A21 —** External memory address line 21.
							I/O	**GPIO7[3] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_4	K13	J11	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**NMI —** External interrupt input to NMI.
							-	**R —** Function reserved.
							I/O	**EMC_A22 —** External memory address line 22.
							I/O	**GPIO7[4] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_5	N16	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_3 —** SCTimer/PWM output 3. Match output 3 of timer 0.
							O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							I/O	**EMC_D24 —** External memory data line 24.
							I/O	**GPIO7[5] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_6	M16	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_2 —** SCTimer/PWM output 2. Match output 2 of timer 0.
							I	**U1_RI —** Ring Indicator input for UART1.
							I/O	**EMC_D25 —** External memory data line 25.
							I/O	**GPIO7[6] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PF_3	E10	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**U3_RXD —** Receiver input for USART3.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							-	**R —** Function reserved.
							I/O	**GPIO7[18] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PF_4	D10	D6	H4	120	[2]	OL; PU	I/O	**SSP1_SCK —** Serial clock for SSP1.
							I	**GP_CLKIN —** General-purpose clock input to the CGU.
							O	**TRACECLK —** Trace clock.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**I2S0_TX_MCLK —** I^2S transmit master clock.
							I/O	**I2S0_RX_SCK —** I^2S receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
PF_5	E9	-	-	-	[5]	N; PU	-	**R —** Function reserved.
							I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							O	**TRACEDATA[0] —** Trace data, bit 0.
							I/O	**GPIO7[19] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC1_4 —** ADC1 and ADC0, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

7.8.1 ISP (In-System Programming) mode

In-System Programming (ISP) means programming or reprogramming the on-chip SRAM memory, using the boot loader software and the USART0 serial port. ISP can be performed when the part resides in the end-user board. ISP loads data into on-chip SRAM and execute code from on-chip SRAM.

7.9 Boot ROM

The internal ROM memory is used to store the boot code of the LPC18S50/S30/S10. After a reset, the ARM processor will start its code execution from this memory.

The boot ROM memory includes the following features:

- The ROM memory size is 64 kB.
- Supports booting from external static memory such as NOR flash, SPI flash, quad SPI flash, USB0, and USB1.
- Includes API for OTP programming.
- Includes a flexible USB device stack that supports Human Interface Device (HID), Mass Storage Class (MSC), and Device Firmware Upgrade (DFU) drivers.

Several boot modes are available depending on the values of the OTP bits BOOT_SRC. If the OTP memory is not programmed or the BOOT_SRC bits are all zero, the boot mode is determined by the states of the boot pins P2_9, P2_8, P1_2, and P1_1.

Table 4. Boot mode when OTP BOOT_SRC bits are programmed

Boot mode	BOOT_SRC bit 3	BOOT_SRC bit 2	BOOT_SRC bit 1	BOOT_SRC bit 0	Description
Pin state	0	0	0	0	Boot source is defined by the reset state of P1_1, P1_2, P2_8, and P2_9 pins. See Table 5.
USART0	0	0	0	1	Boot from device connected to USART0 using pins P2_0 and P2_1.
SPIFI	0	0	1	0	Boot from Quad SPI flash connected to the SPIFI interface using pins P3_3 to P3_8.
EMC 8-bit	0	0	1	1	Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus.
EMC 16-bit	0	1	0	0	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus.
EMC 32-bit	0	1	0	1	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus.
USB0	0	1	1	0	Boot from USB0.
USB1	0	1	1	1	Boot from USB1.
SPI (SSP0)	1	0	0	0	Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI)[1].
USART3	1	0	0	1	Boot from device connected to USART3 using pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.
Remark: Pin functions for SPIFI and SSP0 boot are different.

The I²S-bus provides a standard communication interface for digital audio applications.

The *I²S-bus specification* defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I²S-bus connection has one master, which is always the master, and one slave. The I²S-bus interface provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

7.14.5.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 192 kHz (16, 22.05, 32, 44.1, 48, 96, 192) kHz.
- Support for an audio master clock.
- Configurable word select period in master mode (separately for I²S-bus input and output).
- Two 8-word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. The DMA requests are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I²S-bus input and I²S-bus output.

7.14.6 C_CAN

Remark: The LPC18S50/S30/S10 contain two C_CAN controllers.

Controller Area Network (CAN) is the definition of a high performance communication protocol for serial data communication. The C_CAN controller is designed to provide a full implementation of the CAN protocol according to the CAN Specification Version 2.0B. The C_CAN controller can build powerful local networks with low-cost multiplex wiring by supporting distributed real-time control with a high level of reliability.

7.14.6.1 Features

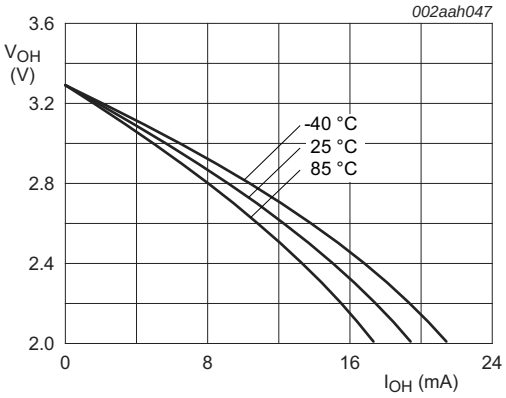
- Conforms to protocol version 2.0 parts A and B.
- Supports bit rate of up to 1 Mbit/s.
- Supports 32 Message Objects.
- Each Message Object has its own identifier mask.
- Provides programmable FIFO mode (concatenation of Message Objects).
- Provides maskable interrupts.
- Supports Disabled Automatic Retransmission (DAR) mode for time-triggered CAN applications.
- Provides programmable loop-back mode for self-test operation.

10. Static characteristics

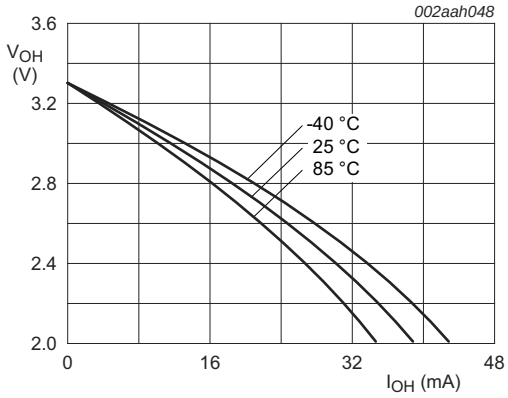
Table 10. Static characteristics

T_{amb} = −40 °C to +85 °C unless otherwise specified.

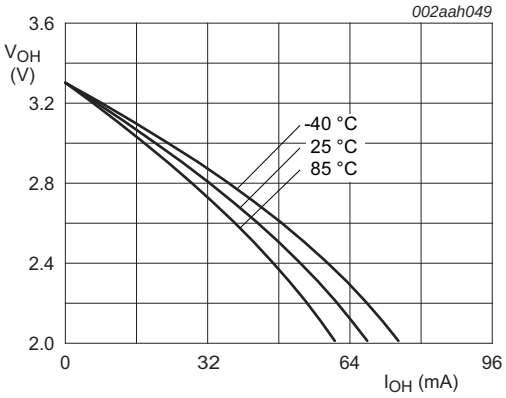
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(IO)}$	input/output supply voltage			2.2	-	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)		[2]	2.2	-	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pin VDDA		2.2	-	3.6	V
		on pins USB0_VDDA3V3_DRIVER and USB0_VDDA3V3		3.0	3.3	3.6	V
V_{BAT}	battery supply voltage		[2]	2.2	-	3.6	V
$V_{prog(pf)}$	polyfuse programming voltage	on pin VPP (for OTP)	[3]	2.7	-	3.6	V
$I_{prog(pf)}$	polyfuse programming current	on pin VPP; OTP programming time ≤ 1.6 ms		-	-	30	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	Active mode; code `while(1){}` executed from RAM; all peripherals disabled; PLL1 enabled					
		CCLK = 12 MHz	[4]	-	6.6	-	mA
		CCLK = 60 MHz	[4]		25.3	-	mA
		CCLK = 120 MHz	[4]	-	48.4	-	mA
		CCLK = 180 MHz	[4]	-	72.0	-	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	after WFE/WFI instruction executed from RAM; all peripherals disabled					
		sleep mode	[4][5]	-	5.0	-	mA
		deep-sleep mode	[4]	-	30	-	µA
		power-down mode	[4]	-	15	-	µA
		deep power-down mode	[4][6]	-	0.03	-	µA
		deep power-down mode; VBAT floating	[4]	-	2	-	µA
I_{BAT}	battery supply current	active mode; V_{BAT} = 3.2 V; $V_{DD(REG)(3V3)}$ = 3.6 V.	[7]	-	0	-	nA
I_{BAT}	battery supply current	$V_{DD(REG)(3V3)}$ = 3.3 V; V_{BAT} = 3.6 V	[9]			-	
		deep-sleep mode		-	2		µA
		power-down mode	[9]	-	2	-	µA
		deep power-down mode	[9]	-	2	-	µA



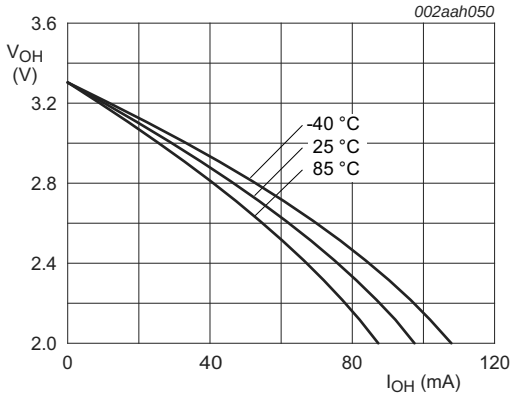
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; normal-drive; EHD = 0x0.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; medium-drive; EHD = 0x1.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; high-drive; EHD = 0x2.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; ultra high-drive; EHD = 0x3.

Fig 22. High-drive pins; typical HIGH level output voltage V_{OH} versus HGH level output current I_{OH}

[9] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

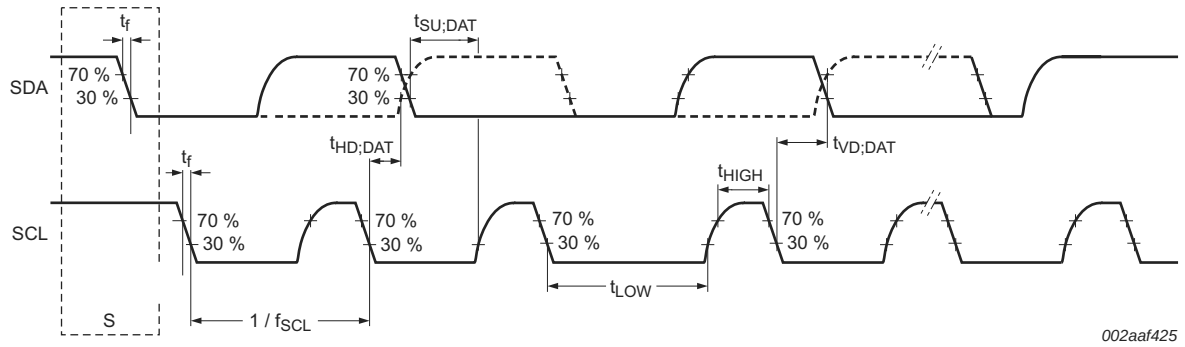


Fig 26. I^2C-bus pins clock timing

11.9 I^2S-bus interface

Table 21. Dynamic characteristics: I^2S-bus interface pins

T_{amb} = 25 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Conditions and data refer to I2S0 and I2S1 pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
common to input and output							
t_r	rise time			-	4	-	ns
t_f	fall time			-	4	-	ns
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
output							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[1]	-	4.4	-	ns
		on pin I2Sx_TX_WS		-	4.3	-	ns
input							
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[1]	-	0	-	ns
		on pin I2Sx_RX_WS			0.20		ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[1]	-	3.7	-	ns
		on pin I2Sx_RX_WS		-	3.9	-	ns

[1] Clock to the I^2S-bus interface BASE_APB1_CLK = 150 MHz; peripheral clock to the I^2S-bus interface PCLK = BASE_APB1_CLK / 12. I^2S clock cycle time $T_{cy(clk)}$ = 79.2 ns; corresponds to the SCK signal in the *I^2S-bus specification*.

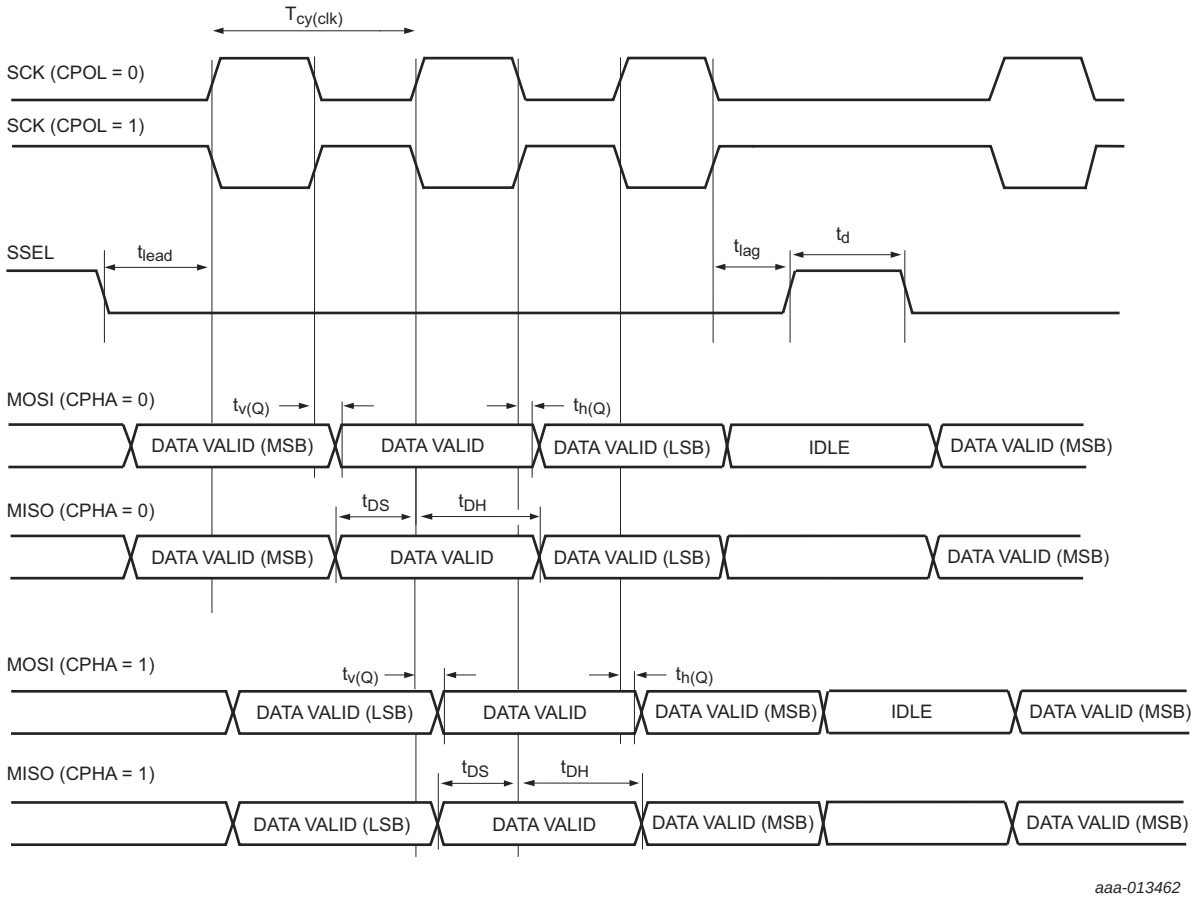


Fig 30. SSP master mode timing (SPI mode)

11.12 External memory interface

Table 24. Dynamic characteristics: Static asynchronous external memory interface

C_L = 22 pF for EMC_Dn C_L = 20 pF for all others; T_{amb} = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; values guaranteed by design. Timing parameters are given for single memory access cycles. In a normal read operation, the EMC changes the address while CS is asserted resulting in multiple memory accesses.

Symbol	Parameter[1]	Conditions		Min	Typ	Max	Unit
Read cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time			−3.1	-	1.6	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		[2]	−0.6 + $T_{cy(clk)}$ × WAITOEN	-	1.3 + $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	PB = 1		−0.7	-	1.8	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time		[2]	−0.6 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	-	−0.4 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	ns
t_{am}	memory access time			-	-	−16 + (WAITRD − WAITOEN +1) × $T_{cy(clk)}$	ns
$t_{h(D)}$	data input hold time			−16	-	-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1		−0.4	-	1.9	ns
t_{CSHOEH}	CS HIGH to $\overline{OE}$ HIGH time			−0.4	-	1.4	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid	PB = 1		−2.0	-	2.6	ns
t_{CSHEOR}	$\overline{CS}$ HIGH to end of read time		[3]	−2.0	-	0	ns
t_{CSLSOR}	$\overline{CS}$ LOW to start of read time		[4]	0	-	1.8	ns
Write cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time			−3.1	-	1.6	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time			−3.1	-	1.5	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	PB = 1		−1.5	-	0.2	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	PB = 1		−0.7	-	1.8	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	PB = 1	[2]	−0.6 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	−0.4 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	PB = 1	[2]	−0.9 + $T_{cy(clk)}$	-	2.3 + $T_{cy(clk)}$	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	PB = 1	[2] [5]	−0.4 + $T_{cy(clk)}$	-	−0.3 + $T_{cy(clk)}$	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW	PB = 0		−0.7	-	1.8	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 0	[2]	−0.9 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	−0.1 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns

Table 28. Static characteristics: USB0 PHY pins[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
High-speed mode							
P_{cons}	power consumption		[2]	-	68	-	mW
$I_{DDA(3V3)}$	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER; total supply current	[3]	-	18	-	mA
		during transmit		-	31	-	mA
		during receive		-	14	-	mA
		with driver tri-stated		-	14	-	mA
I_{DDD}	digital supply current			-	7	-	mA
Full-speed/low-speed mode							
P_{cons}	power consumption		[2]	-	15	-	mW
$I_{DDA(3V3)}$	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER; total supply current		-	3.5	-	mA
		during transmit		-	5	-	mA
		during receive		-	3	-	mA
		with driver tri-stated		-	3	-	mA
I_{DDD}	digital supply current			-	3	-	mA
Suspend mode							
$I_{DDA(3V3)}$	analog supply current (3.3 V)			-	24	-	μA
		with driver tri-stated		-	24	-	μA
		with OTG functionality enabled		-	3	-	mA
I_{DDD}	digital supply current			-	30	-	μA
VBUS detector outputs							
V_{th}	threshold voltage	for VBUS valid		4.4	-	-	V
		for session end		0.2	-	0.8	V
		for A valid		0.8	-	2	V
		for B valid		2	-	4	V
V_{hys}	hysteresis voltage	for session end		-	150	10	mV
		A valid		-	200	10	mV
		B valid		-	200	10	mV

[1] Characterized but not implemented as production test.

[2] Total average power consumption.

[3] The driver is active only 20 % of the time.

11.14 Ethernet

Remark: The timing characteristics of the ENET_MDC and ENET_MDIO signals comply with the *IEEE standard 802.3*.

12. ADC/DAC electrical characteristics

Table 33. ADC characteristics

$V_{DDA(3V3)}$ over specified ranges; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	$V_{DDA(3V3)}$	V
C_{ia}	analog input capacitance			-	-	2	pF
E_D	differential linearity error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1][2]	-	±0.8	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	LSB
$E_{L(adj)}$	integral non-linearity	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[3]	-	±0.8	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.5	-	LSB
E_O	offset error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[4]	-	±0.15	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±0.15	-	LSB
E_G	gain error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[5]	-	±0.3	-	%
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±0.35	-	%
E_T	absolute error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[6]	-	±3	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±4	-	LSB
R_{vsi}	voltage source interface resistance	see Figure 40		-	-	$1/(7 \times f_{clk(ADC)} \times C_{ia})$	kΩ
R_i	input resistance		[7][8]	-	-	1.2	MΩ
$f_{clk(ADC)}$	ADC clock frequency			-	-	4.5	MHz
f_s	sampling frequency	10-bit resolution; 11 clock cycles		-	-	400	kSamples/s
		2-bit resolution; 3 clock cycles				1.5	MSamples/s

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 39.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 39.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 39.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 39.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 39.

[7] T_{amb} = 25 °C.

[8] Input resistance R_i depends on the sampling frequency fs: $R_i = 2\ k\Omega + 1 / (f_s \times C_{ia})$.

Table 38. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
12 MHz	< 160 Ω	18 pF, 18 pF
	< 160 Ω	39 pF, 39 pF
16 MHz	< 120 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF
20 MHz	< 100 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF

Table 39. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{x2}
15 MHz	< 80 Ω	18 pF, 18 pF
20 MHz	< 80 Ω	39 pF, 39 pF
	< 100 Ω	47 pF, 47 pF

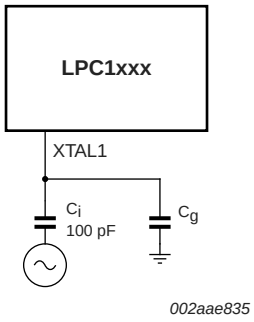


Fig 41. Slave mode operation of the on-chip oscillator

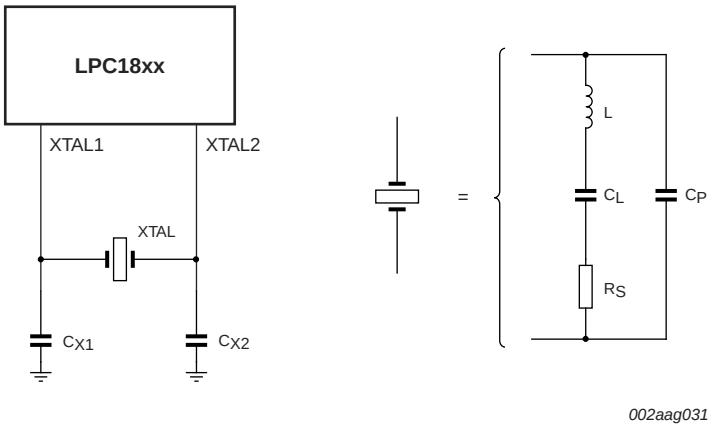


Fig 42. Oscillator modes with external crystal model used for C_{X1}/C_{X2} evaluation