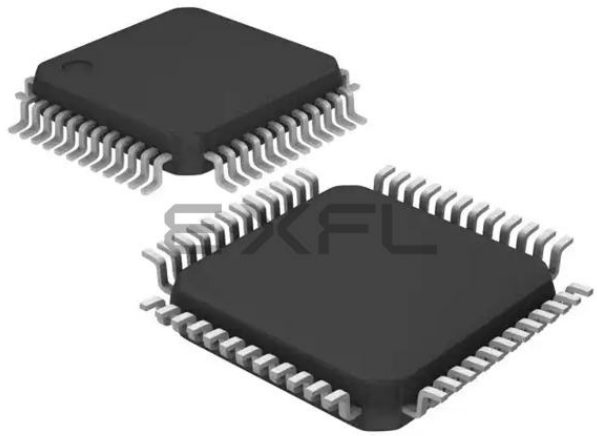

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f84550vlfr

1 Overview

1.1 MC56F844xx/5xx/7xx product family

The following table lists major features, including features that differ among members of the family. Features not listed are shared by all members of the family.

Table 1. 56F844xx/5xx/7xx family

Part Number	MC56F84																	
	789	786	769	766	763	553	550	543	540	587	585	567	565	462	452	451	442	441
Core freq. (MHz)	100	100	100	100	100	80	80	80	80	80	80	80	80	60	60	60	60	60
Flash memory (KB)	256	256	128	128	128	96	96	64	64	256	256	128	128	128	96	96	64	64
FlevNVM/ FlexRAM (KB)	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2
Total flash memory (KB)[1]	288	288	160	160	160	128	128	96	96	288	288	160	160	160	128	128	96	96
RAM (KB)	32	32	24	24	24	16	16	8	8	32	32	24	24	24	16	16	8	8
Memory resource protection	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
External Watchdog	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12-bit Cyclic ADC Channels (ADCA and ADCB)	2x8	2x8	2x8	2x8	2x8	2x8	2x5	2x8	2x5	2x8	2x8	2x8	2x8	2x8	2x8	2x5	2x8	2x5
12-bit Cyclic ADC Conversion time (ADCA and ADCB)	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	600 ns	600 ns	600 ns	600 ns	600 ns	600 ns	600 ns	600 ns	600 ns
16-bit SAR ADC (with Temperature Sensor) channels (ADCC)	16	10	16	10	8	8	–	8	–	16	10	16	10	–	8	–	8	–
PWMA High-res channels	8	8	8	8	8	8	6	8	6	0	0	0	0	0	0	0	0	0

Table continues on the next page...

- 32-bit internal primary data buses support 8-bit, 16-bit, and 32-bit data movement, plus addition, subtraction, and logical operations
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves
- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, which effectively supports DSP and Fast Fourier Transform algorithms
- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers correspond to nine address registers (R0, R1, R2, R3, R4, R5, N, N3, M01)
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions enable compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack, with the stack's depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

1.3 Operation parameters

- Up to 80 MHz operation at -40 °C to 105 °C ambient temperature
- Single 3.3 V power supply
- Supply range: V_{DD} - V_{SS} = 2.7 V to 3.6 V, V_{DDA} - V_{SSA} = 2.7 V to 3.6 V

1.4 On-chip memory and memory protection

- Modified dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access
- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- The dual-ported RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses, by the DSC core.

2 MC56F8455x signal and pin descriptions

After reset, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses, must be programmed through the GPIO module peripheral enable registers (GPIO_x_PER) and the SIM module GPIO peripheral select (GPSx) registers. All GPIO ports can be individually programmed as an input or output (using bit manipulation).

- There are 2 PWM modules: PWM**A**, PWM**B**. Each PWM module has 4 submodules: PWMA has PWMA_**0**, PWMA_**1**, PWMA_**2**, PWMA_**3**; PWMB has PWMB_0, PWMB_1, PWMB_2, PWMB_3. Each PWM module's submodules have 3 pins (A, B, X) each, with the syntax for the pins being PWMA_0**A**, PWMA_0**B**, PWMA_0**X**, and PWMA_1A, PWMA_1B, PWMA_1X, and so on. Each submodule pin can be configured as a PWM output or as a capture input.
- EWM_OUT_B is the output of the External Watchdog Module (EWM), and is active low (denoted by the "_B" part of the syntax).

For the MC56F84**55X** products, which use 48-pin LQFP and 64-pin LQFP packages:

Table 2. Signal descriptions

Signal Name	64 LQFP	48 LQFP	Type	State During Reset[1]	Signal Description
V_{DD}	29	-	Supply	Supply	I/O Power — Supplies 3.3 V power to the chip I/O interface.
V_{DD}	44	32			
V_{DD}	60	44			
V_{SS}	30	22	Supply	Supply	I/O Ground — Provide ground for the device I/O interface.
V_{SS}	43	31			
V_{SS}	61	45			
V_{DDA}	22	15	Supply	Supply	Analog Power — Supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
V_{SSA}	23	16	Supply	Supply	Analog Ground — Supplies an analog ground to the analog modules. It must be connected to a clean power supply.
V_{CAP}	26	19	On-chip regulator output voltage	On-chip regulator output voltage	Connect a 2.2uF or greater bypass capacitor between this pin and V_{SS} to stabilize the core voltage regulator output required for proper device operation. V_{CAP} is used to observe core voltage.
V_{CAP}	57	43			

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	Type	State During Reset[1]	Signal Description
GPIOC2	5	5	Input/Output	Input	GPIO Port C2: After reset, the default state is GPIOC2.
(TXD0)			Output		SCI0 transmit data output or transmit/receive in single-wire operation
(TB0)			Input/Output		Quad timer module B channel 0 input/output
(XB_IN2)			Input		Crossbar module input 2
(CLKO0)			Output		Buffered clock output 0: the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
GPIOC3	7	6	Input/ Output	Input	GPIO Port C3: After reset, the default state is GPIOC3.
(TA0)			Input/ Output		Quad timer module A channel 0 input/output
(CMPA_O)			Output		Analog comparator A output
(RXD0)			Input		SCI0 receive data input
(CLKIN1)			Input		External clock input 1
GPIOC4	8	7	Input/ Output	Input	GPIO Port C4: After reset, the default state is GPIOC4.
(TA1)			Input/ Output		Quad timer module A channel 1 input/output
(CMPB_O)			Output		Analog comparator B output
(XB_IN8)			Input		Crossbar module input 8
(EWM_OUT_B)			Output		External Watchdog Module output
GPIOC5	18	13	Input/ Output	Input	GPIO Port C5: After reset, the default state is GPIOC5.
(DACO)			Analog Output		12-bit digital-to-analog output
(XB_IN7)			Input		Crossbar module input 7
GPIOC6	31	23	Input/ Output	Input,	GPIO Port C6: After reset, the default state is GPIOC6.
(TA2)			Input/ Output		Quad timer module A channel 2 input/output
(XB_IN3)			Input		Crossbar module input 3
(CMP_REF)			Analog Input		Positive input 5 of analog comparator A and B and C and D. Note: MC56F84550 and MC56F84540 do not have CMPD.
GPIOC7	32	24	Input/ Output	Input	GPIO Port C7: After reset, the default state is GPIOC7.
($\overline{SS0\_B}$)			Input/ Output		In slave mode, $\overline{SS0\_B}$ indicates to the SPI module 0 that the current transfer is to be received.
(TXD0)			Output		SCI0 transmit data output or transmit/receive in single-wire operation

Table continues on the next page...

8.2 AC electrical characteristics

Tests are conducted using the input levels specified in Table 8. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 3.

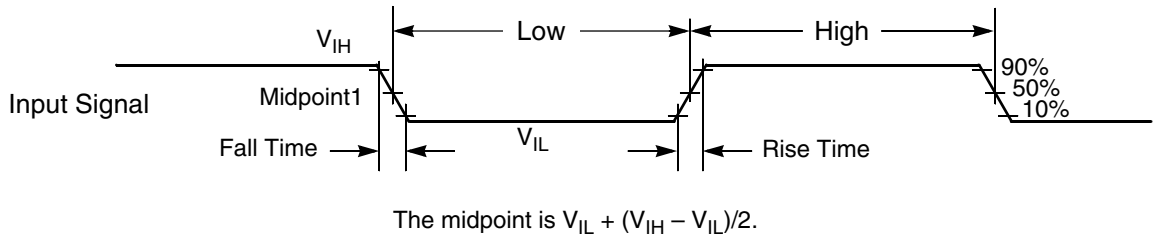


Figure 3. Input signal measurement references

Figure 4 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

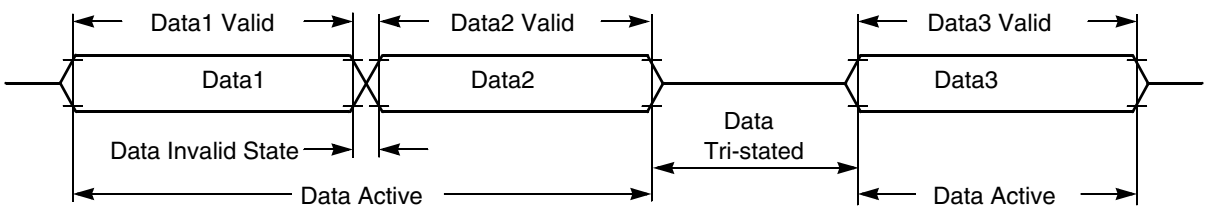


Figure 4. Signal states

8.3 Nonswitching electrical specifications

8.3.1 Voltage and current operating requirements

This section includes information about recommended operating conditions.

NOTE

Recommended V_{DD} ramp rate is between 1 ms and 200 ms.

Table 6. Recommended Operating Conditions (V_{REFLx}=0V, V_{SSA}=0V, V_{SS}=0V)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit
Supply voltage[2]	V_{DD}, V_{DDA}		2.7	3.3	3.6	V

Table continues on the next page...

Table 6. Recommended Operating Conditions (V_{REFLx}=0V, V_{SSA}=0V, V_{SS}=0V) (continued)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit
ADC (Cyclic) Reference Voltage High	V_{REFHA} V_{REFHB}		3.0		V_{DDA}	V
ADC (SAR) Reference Voltage High	V_{REFHC}		2.0		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔVDD		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔVSS		-0.1	0	0.1	V
Input Voltage High (digital inputs)	V_{IH}	Pin Group 1	0.7 x V_{DD}		5.5	V
$\overline{\text{RESET}}$ Voltage High	V_{IH_RESET}	Pin Group 2	0.7 x V_{DD}	—	V_{DD}	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2			0.35 x V_{DD}	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
Output Source Current High (at V_{OH} min.)[3, 4] • Programmed for low drive strength • Programmed for high drive strength	I_{OH}	Pin Group 1 Pin Group 1	— —		-2 -9	mA
Output Source Current Low (at V_{OL} max.)[3, 4] • Programmed for low drive strength • Programmed for high drive strength	I_{OL}	Pin Groups 1, 2 Pin Groups 1, 2	— —		2 9	mA

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
2. ADC (Cyclic) specifications are not guaranteed when V_{DDA} is below 3.0 V.
3.
4. Contiguous pin DC injection current of regional limit—including sum of negative injection currents or sum of positive injection currents of 16 contiguous pins—is 25 mA.

8.3.2 LVD and POR operating requirements

Table 7. PMC Low-Voltage Detection (LVD) and Power-On Reset (POR) Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
POR Assert Voltage[1]	POR		2.0		V
POR Release Voltage[2]	POR		2.7		V
LVI_2p7 Threshold Voltage			2.73		V
LVI_2p2 Threshold Voltage			2.23		V

1. During 3.3-volt V_{DD} power supply ramp down
2. During 3.3-volt V_{DD} power supply ramp up (gated by LVI_2p7)

Table 11. Current Consumption (continued)

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25°C		Maximum at 3.6 V, 105°C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
LPSTOP (LsSTOP)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator (ROSC) • ROSC in standby mode • Regulators are in standby • PLL disabled • Only PITs and COP enabled; other peripheral modules disabled and clocks gated off[3] • Processor core in stop mode	1.06 mA	13.10 µA	14.74 mA	43.2 µA
VLPRUN	200 kHz	• 32 kHz Device Clock • Clocked by a 32 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled • Repeat NOP instructions • All peripheral modules, except COP and EWM, disabled and clocks gated off • Simple loop running from platform instruction buffer	0.57 mA	12.20 µA	8.39 mA	17.40 µA
VLPWAIT	200 kHz	• 32 kHz Device Clock • Clocked by a 32 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled • All peripheral modules, except COP, disabled and clocks gated off • Processor core in wait mode	0.56 mA	11.44 µA	8.30 mA	15.00 µA
VLPSTOP	200 kHz	• 32 kHz Device Clock • Clocked by a 32 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled • All peripheral modules, except COP, disabled and clocks gated off • Processor core in stop mode	0.56 mA	10.44 µA	8.21 mA	13.14 µA

1. No output switching, all ports configured as inputs, all inputs low, no DC loads
2. ADC power consumption at higher frequency can be found in Table 28
3. In all chip LP modes and flash memory VLP modes, the maximum frequency for flash memory operation is 250 kHz, because of the fixed frequency ratio of 1:4 between the CPU clock and the flash clock (when using a 2 MHz external input clock and the CPU is operating at 1 MHz).

9.2 System modules

9.2.1 Voltage regulator specifications

The voltage regulator supplies approximately 1.2 V to the MC56F84xxx's core logic. For proper operations, the voltage regulator requires an external 2.2 µF capacitor on each V_{CAP} pin. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator are shown in Table 17.

Table 17. Regulator 1.2 V parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage[1]	V_{CAP}	—	1.22	—	V
Short Circuit Current[2]	I_{SS}	—	600	—	mA
Short Circuit Tolerance (V_{CAP} shorted to ground)	T_{RSC}	—	—	30	Minutes

1. Value is after trim
2. Guaranteed by design

Table 18. Bandgap electrical specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Reference Voltage (after trim)	V_{REF}	—	1.21	—	V

9.3 Clock modules

9.3.1 External clock operation timing

Parameters listed are guaranteed by design.

Table 19. External clock operation timing requirements

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	—	—	50	MHz
Clock pulse width[2]	t_{PW}	8			ns
External clock input rise time[3]	t_{rise}	—	—	1	ns
External clock input fall time[4]	t_{fall}	—	—	1	ns
Input high voltage overdrive by an external clock	V_{ih}	$0.85V_{DD}$	—	—	V
Input low voltage overdrive by an external clock	V_{il}	—	—	$0.3V_{DD}$	V

9.3.4 Relaxation oscillator timing

Table 22. Relaxation oscillator electrical specifications

Characteristic	Symbol	Min	Typ	Max	Unit
8 MHz Output Frequency[1] RUN Mode • 0°C to 105°C • -40°C to 105°C Standby Mode (IRC trimmed @ 8 MHz) • -40°C to 105°C		 7.84 7.76 266.8	 8 8 402	 8.16 8.24 554.3	 MHz kHz
8 MHz Frequency Variation RUN Mode Due to temperature • 0°C to 105°C • -40°C to 105°C			 +/- 1.5 +/- 1.5	 +/-2 +/-3	 %
32 kHz Output Frequency[2] RUN Mode • -40°C to 105°C		 30.1	 32	 33.9	 kHz
32 kHz Output Frequency Variation RUN Mode Due to temperature • -40°C to 105°C			 +/-2.5	 +/-4	 %
Stabilization Time • 8 MHz output[3] • 32 kHz output[4]	tstab		0.12 14.4	0.4 16.2	µs
Output Duty Cycle		48	50	52	%

1. Frequency after application of 8 MHz trim
2. Frequency after application of 32 kHz trim
3. Standby to run mode transition
4. Power down to run mode transition

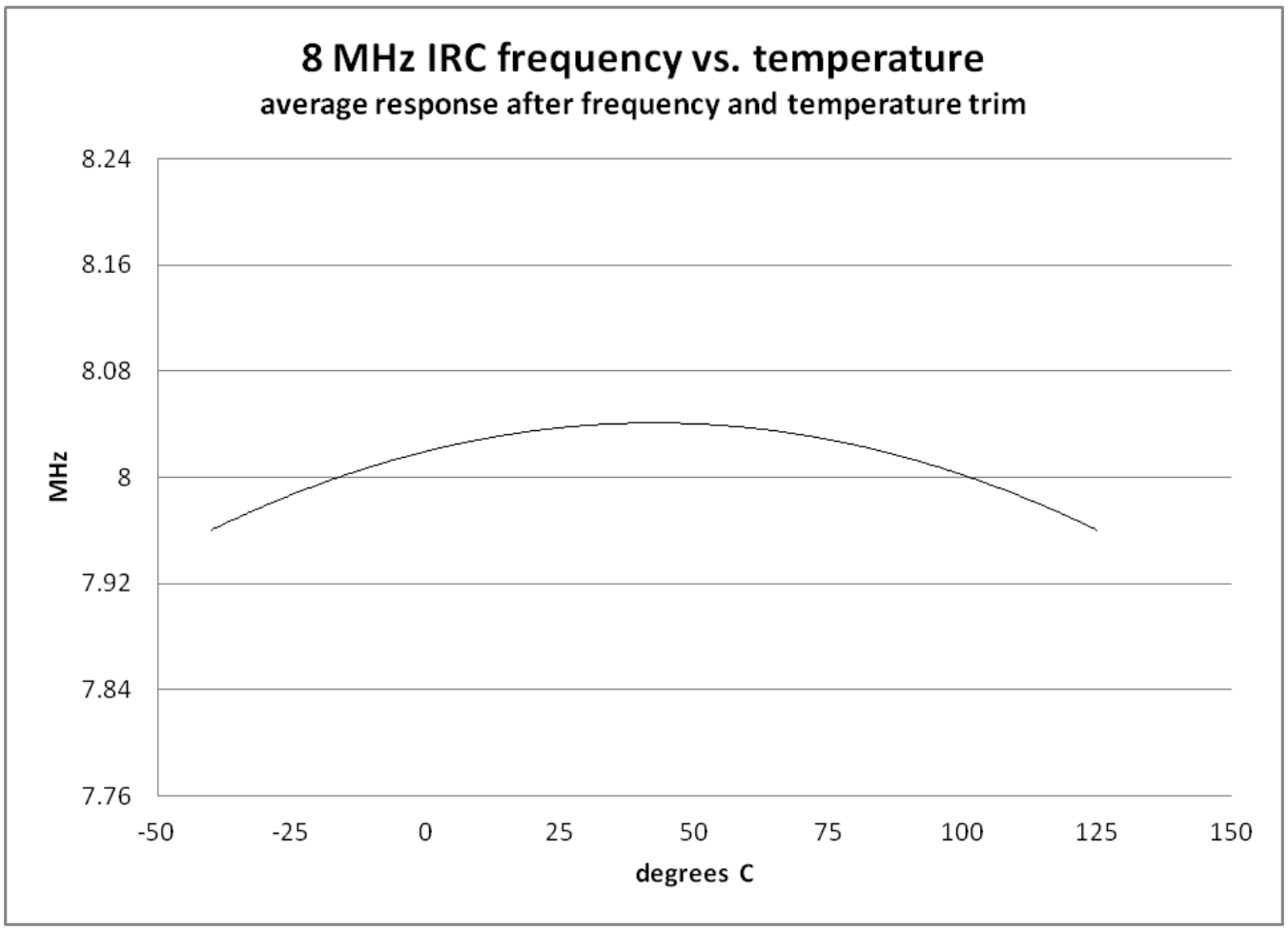


Figure 8. Relaxation oscillator temperature variation (typical) after trim (preliminary)

9.4 Memories and memory interfaces

9.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

9.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—

Table continues on the next page...

9.4.1.4 Reliability specifications

Table 26. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	Program Flash					
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
	Data Flash					
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
	FlexRAM as EEPROM					
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	—
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	—
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
$n_{nvmwree4k}$	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
$n_{nvmwree8k}$	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ T_j ≤ 125 °C.
3. Write endurance represents the number of writes to each FlexRAM location at -40 °C ≤Tj ≤ 125 °C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup. Minimum and typical values assume all byte-writes to FlexRAM.

9.5 Analog

9.5.1 12-bit cyclic Analog-to-Digital Converter (ADC) parameters

Table 27. 12-bit ADC electrical specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Recommended Operating Conditions					
Supply Voltage[1]	V_{DDA}	2.7	3.3	3.6	V
Vrefh Supply Voltage[2]	Vrefhx	3.0		V_{DDA}	V
ADC Conversion Clock[3]	f_{ADCCLK}	0.6		20	MHz
Conversion Range	R_{AD}	V_{REFL}		V_{REFH}	V

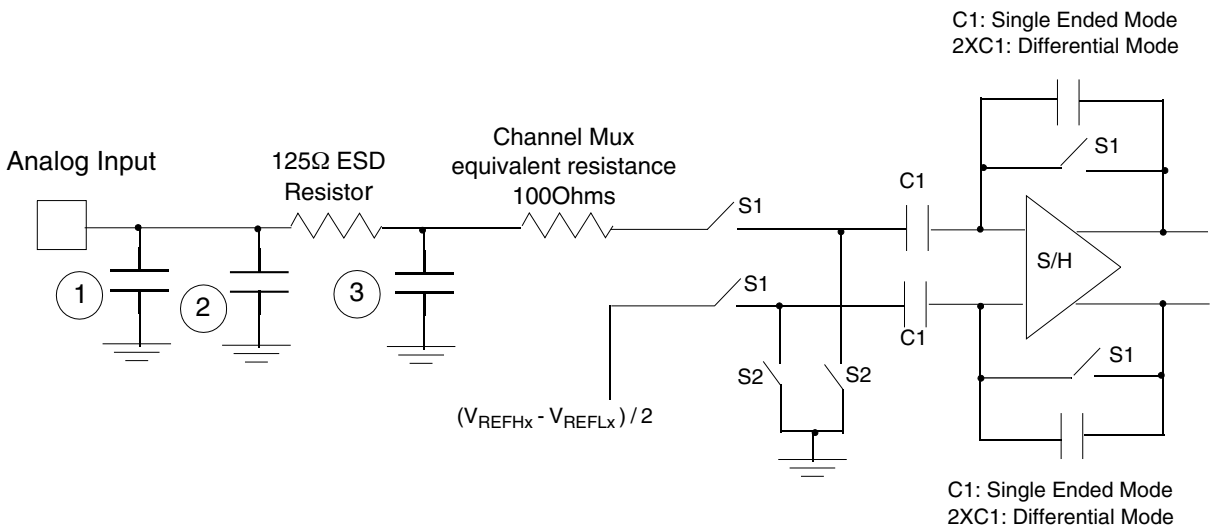
Table continues on the next page...

1. If the ADC's reference is from V_{DDA}: When V_{DDA} is below 3.0 V, then the ADC functions, but the ADC specifications are not guaranteed.
2. When the input is at the V_{refl} level, then the resulting output will be all zeros (hex 000), plus any error contribution due to offset and gain error. When the input is at the V_{refh} level, then the output will be all ones (hex FFF), minus any error contribution due to offset and gain error.
3. ADC clock duty cycle min/max is 45/55%
4. I_{NL} measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$.
5. LSB = Least Significant Bit = 0.806 mV at 3.3 V VDDA, x1 Gain Setting
6. Offset over the conversion range of 0025 to 4080, with internal/external reference.
7. Measured when converting a 1 kHz input Full Scale sine wave.
8. The current that can be *injected into* or *sourced from* an unselected ADC input, without affecting the performance of the ADC.

9.5.1.1 Equivalent circuit for ADC inputs

The following figure shows the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases, and both S1 and S2 operate at the ADC clock frequency. The following equation gives equivalent input impedance when the input is selected.

$$\frac{1}{(\text{ADC ClockRate}) \times 1.4 \times 10^{-12}} + 100ohm + 125ohm$$



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling = 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing = 2.04pF
3. 8 pF noise damping capacitor
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 (4.8pF) is normally disconnected from the input, and is only connected to the input at sampling time.
5. S1 and S2 switch phases are non-overlapping and operate at the ADC clock frequency

9.6.2 Quad Timer timing

Parameters listed are guaranteed by design.

Table 33. Timer timing

Characteristic	Symbol	Min[1]	Max	Unit	See Figure
Timer input period	P_{IN}	2T + 6	—	ns	Figure 14
Timer input high/low period	P_{INHL}	1T + 3	—	ns	Figure 14
Timer output period	P_{OUT}	25	—	ns	Figure 14
Timer output high/low period	P_{OUTHL}	12.5	—	ns	Figure 14

1. T = clock cycle. For 80 MHz operation, T = 12.5 ns.

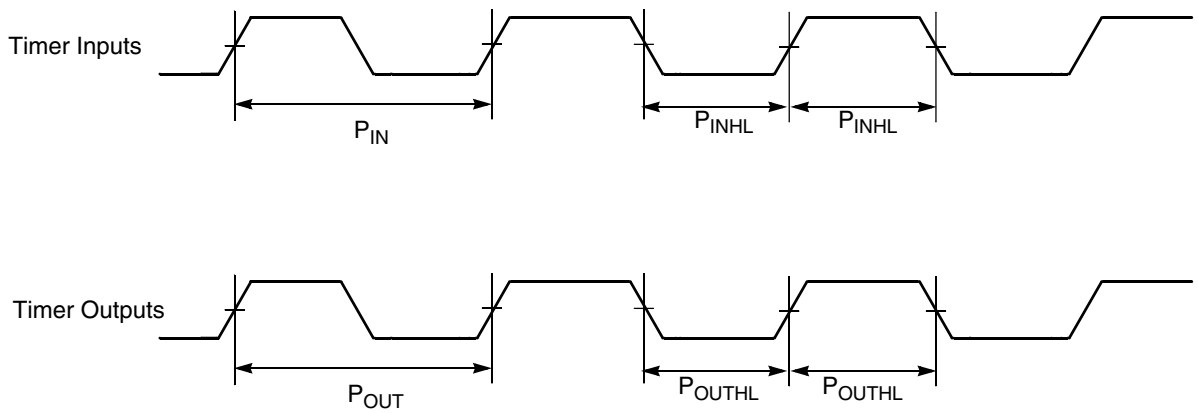


Figure 14. Timer timing

9.7 Communication interfaces

9.7.1 Queued Serial Peripheral Interface (SPI) timing

Parameters listed are guaranteed by design.

Table 34. SPI timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time	t_C	45	—	ns	Figure 15
Master		45	—	ns	Figure 16
Slave					Figure 17
					Figure 18

Table continues on the next page...

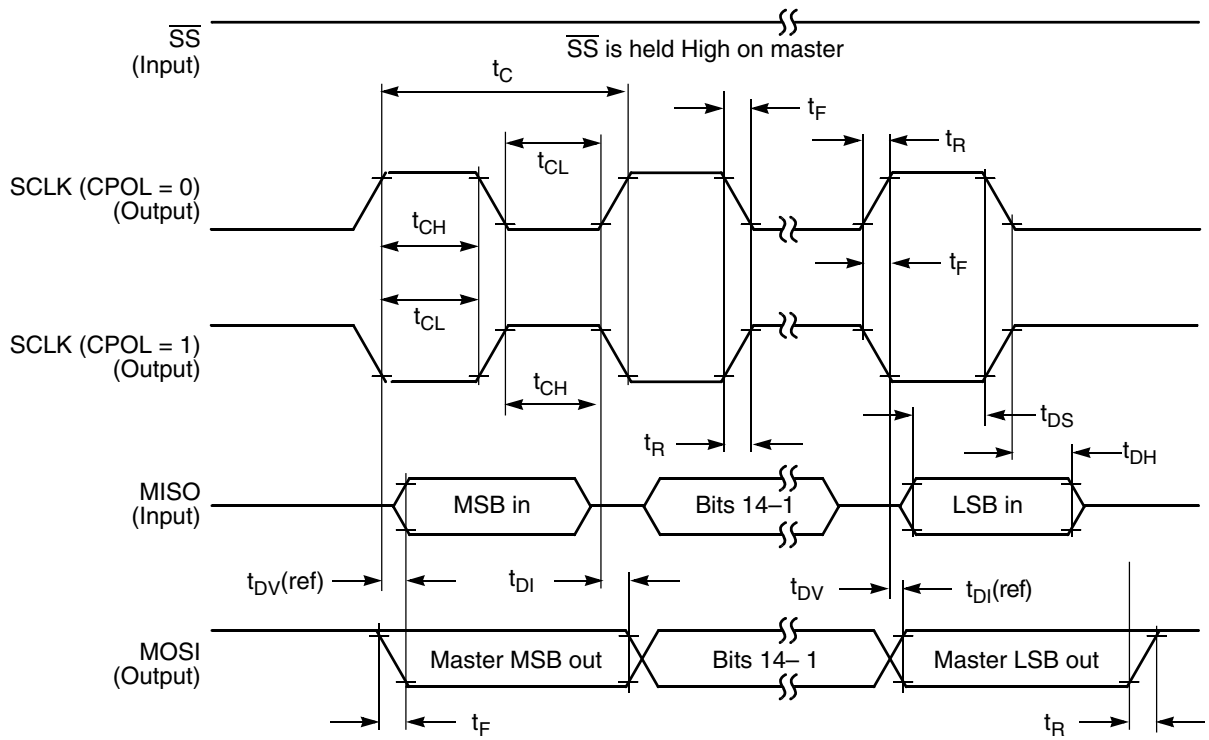


Figure 16. SPI master timing (CPHA = 1)

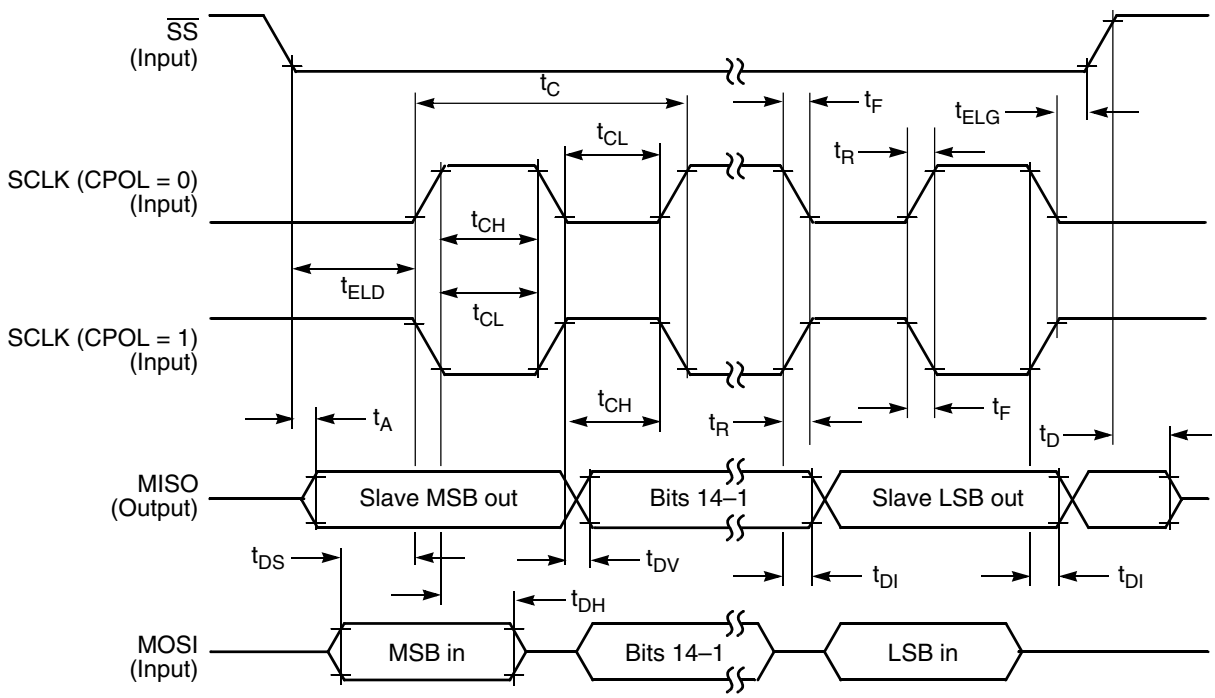


Figure 17. SPI slave timing (CPHA = 0)

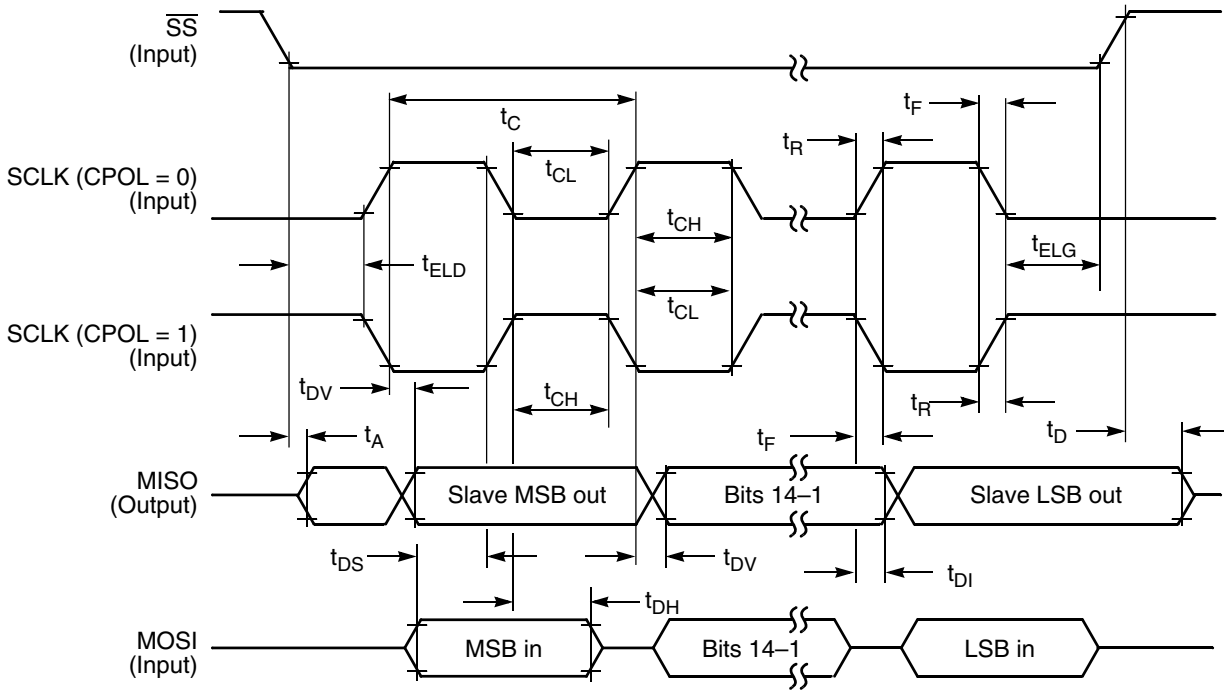


Figure 18. SPI slave timing (CPHA = 1)

9.7.2 Queued Serial Communication Interface (SCI) timing

Parameters listed are guaranteed by design.

Table 35. SCI timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud rate[1]	BR	—	(f_{MAX}/16)	Mbit/s	—
RXD pulse width	RXD_{PW}	0.965/BR	1.04/BR	ns	Figure 19
TXD pulse width	TXD_{PW}	0.965/BR	1.04/BR	ns	Figure 20
LIN Slave Mode					
Deviation of slave node clock from nominal clock rate before synchronization	$F_{TOL\_UNSYNCH}$	-14	14	%	—
Deviation of slave node clock relative to the master node clock after synchronization	F_{TOL_SYNCH}	-2	2	%	—
Minimum break character length	T_{BREAK}	13	—	Master node bit periods	—
		11	—	Slave node bit periods	—

1. f_{MAX} is the frequency of operation of the SCI clock in MHz, which can be selected as the bus clock (max.160 MHz depending on part number) or 2x bus clock (max. MHz) for the devices.

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

To determine the junction temperature of the device in the application when heat sinks are used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

10.2 Electrical design considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the device:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1 µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.
- Bypass the V_{DD} and V_{SS} with approximately 100 µF, plus the number of 0.1 µF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.

- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA}, and V_{SSA} pins.
- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA} are recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, then connect a small inductor or ferrite bead in serial with V_{DDA}. Traces of V_{SS} and V_{SSA} should be shorted together.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or I^2C, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The resistor value should be in the range of 4.7 kΩ–10 kΩ; the capacitor value should be in the range of 0.22 µF–4.7 µF.
- Configuring the $\overline{\text{RESET}}$ pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 kΩ external pullup on the TMS pin of the JTAG port to keep EOnCE in a restate during normal operation if JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at tri-state.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33 pF 10Ω RC filter.

11 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **freescale.com** and perform a keyword search for the drawing's document number:

Drawing for package	Document number to be used
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W

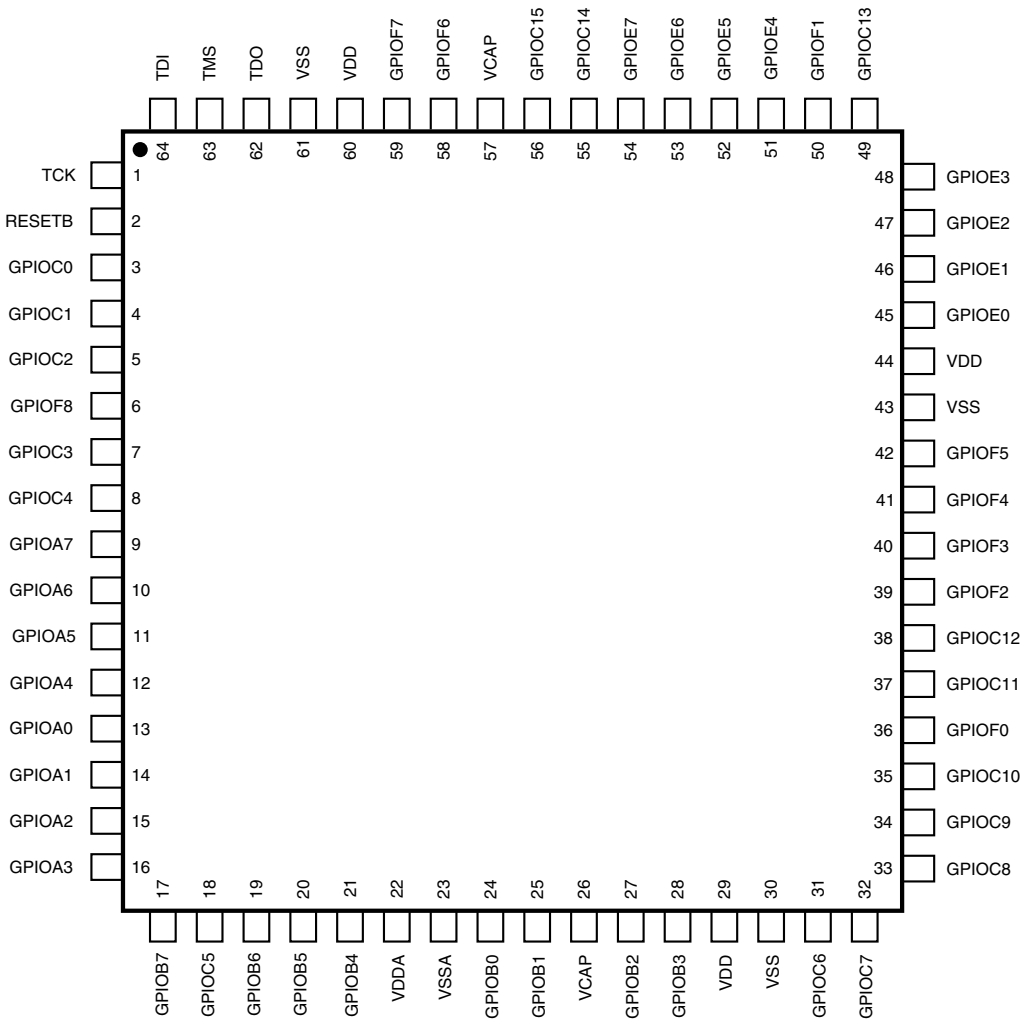


Figure 23. 64-pin LQFP

NOTE

The RESETB pin is a 3.3 V pin only.

13 Product documentation

The documents listed in Table 38 are required for a complete description and proper design with the device. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, or online at **freescale.com**.

Table 38. Device documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F8455x Reference Manual	Detailed functional description and programming model	MC56F8455XRM
MC56F8455x Data Sheet	Electrical and timing specifications, pin descriptions, and package information (this document)	MC56F8455X
MC56F84xxx Errata	Details any chip issues that might be present	MC56F84XXX_0N27E

14 Revision history

The following table summarizes changes to this document since the release of the previous version.

Table 39. Revision history

Rev.	Date	Substantial Changes

3	06/2014	Changes include:
		• Correction to "PWMs and timers" feature group on page 1
		• Updates and corrections to "56F844xx/5xx/7xx family" table.
		• In "Interrupt Controller" section, added info about Interrupt level 3.
		• In "Enhanced Flex Pulse Width Modulator (eFlexPWM)" section,
		  • Upated PWM frequencies based on device frequency, plus updated resolution of fractional clock digital dithering.
		  • Updated feature list.
		• Added new section "MC56F844xx signal and pin descriptions".
		• In "Signal groups" section, in "Functional Group Pin Allocations" table, made corrections to "Functional Group Pin Allocations" table.
		• In "Voltage and current operating requirements" section, added RESET voltage high to "Recommended Operating Conditions" table.
		• In "Voltage and current operating behaviors" section, in "DC Electrical Characteristics" table, updated Digital Input Current High for Pin Group 2.
		• For "Power mode transition operating behaviors" section,
		  • Changed the name to "Power mode operating behaviors".
		  • In "Reset, Stop, Wait, and Interrupt Timing" table, updated "RESET deassertion to First Address Fetch" parameters.
		  • Added new table "Power-On-Reset mode transition times".
		• In "Power consumption operating behaviors" section, updated mode currrent values in "Current Consumption" table.
		• In "JTAG Timing" section, changed "TCK frequency of operation" to SYS_CLK/16 from SYS_CLK/8.
		• In "System modules" section, in "Voltage regulator specifications" section, in "Regulator 1.2 V parameters" table, updated "Short Circuit Current" parameter.
		• In "Relaxation Oscillator Timing" section, updates in "Relaxation Oscillator Electrical Specifications" table.
		• In "Memories and memory interfaces" section,
		  • "Flash Memory Characteristics" section is now called "Flash electrical specifications" section.
		  • Added new section "Flash timing specifications — program and erase", where the "Flash Timing Parameters" table (now called "NVM program/erase timing specifications" table, and table was updated.
		  • Added new section "Flash high voltage current behaviors".
		• In "Analog" section, in "12-bit cyclic Analog-to-Digital Converter (ADC) parameters" section, updated "12-bit ADC electrical specifications" table.
		• In "Pinout" section, in "Signal Multiplexing and Pin Assignments" section,
		  • Added 3 notes.
		  • In pin mux table, changed SCK0 to SCLK0, SCK1 to SCLK1, updates to 64LQFP[62-64] and 48LQFP[46-48].
		  • In "64-pin LQFP" figure, made updates to pins 62-64, and added a note.
		  • In "48-pin LQFP" figure, made updates to pins 46-48, and added a note.
		• In "Product Documentation" section, in "Device Documentation" table, removed Serial Bootloader User Guide, because it is not used for these devices.