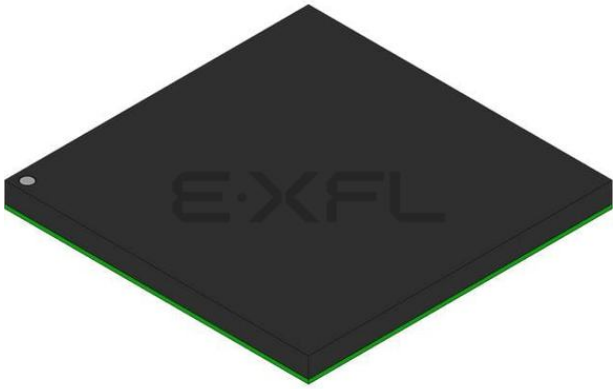

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What is "Embedded - Microcontrollers"?

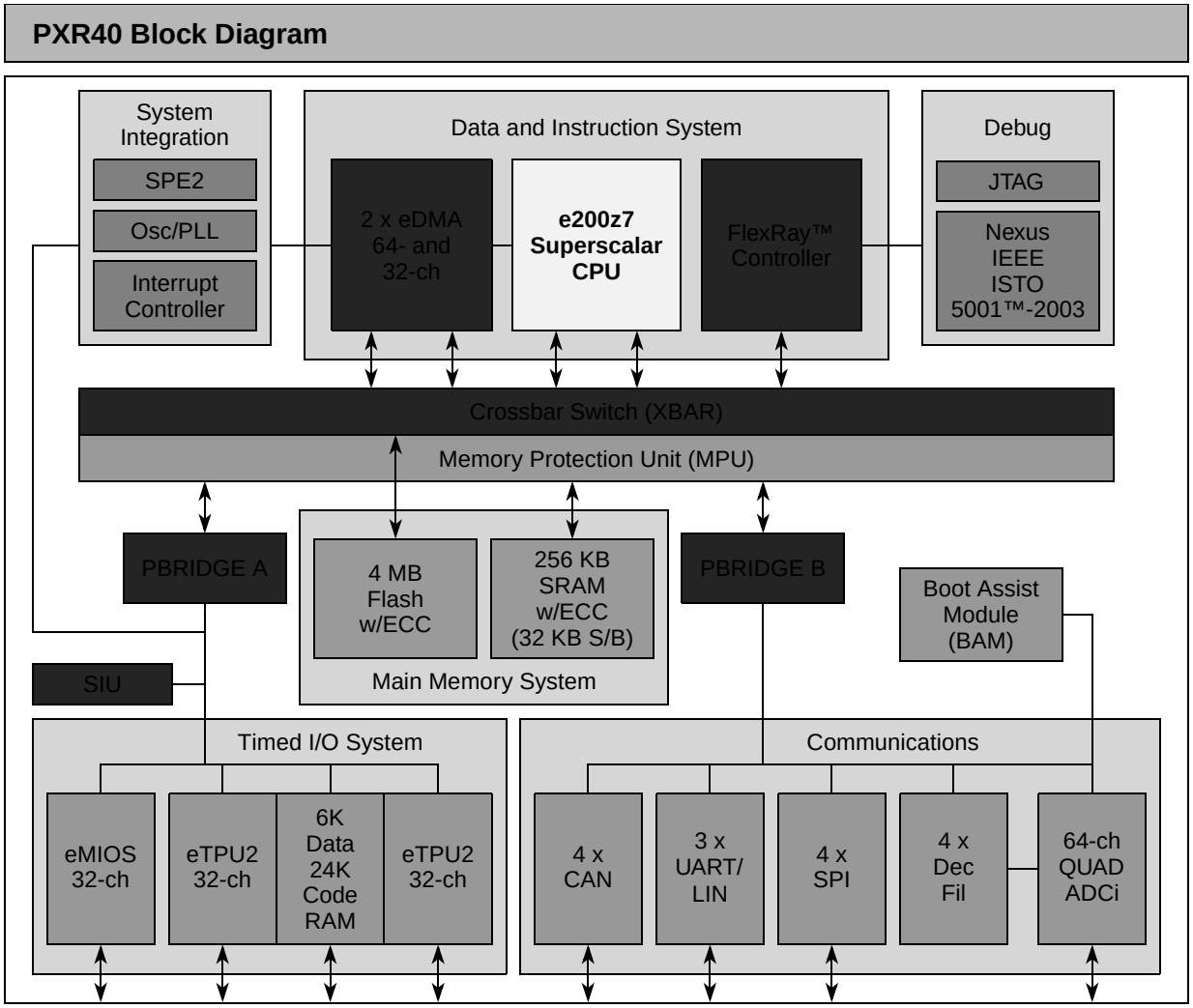
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Single-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	198
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpxr4040vvu264

2 PXR40 block diagram

Figure 1 shows a top-level block diagram of the PXR40 microcontrollers.



ADC – Analog-to-digital converter
ADCi – ADC interface
AIPS – Peripheral I/O bridge
AMux – Analog multiplexer
CAN – Controller area network
DECFIL – Decimation filter
EBI – External bus interface
ECSM – Error correction status module
eDMA2 – Enhanced direct memory access
eMIOS – Enhanced modular I/O system
eQADC – Enhanced queued A/D converter module
eTPU2 – Enhanced time processing unit 2
MMU – Memory management unit
MPU – Memory protection unit
PBRIDGE – Peripheral I/O bridge
S/B – Stand-by
SIU – System integration unit
SPE2 – Signal processing engine 2
SPI – Serial peripheral interface controller
SRAM – General-purpose static RAM
UART/LIN – Universal asynchronous receiver/transmitter/ local interconnect network
VLE – Variable length instruction encoding

Figure 1. Block diagram

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location (416)
143	ETPUA29_PCSC2_ GPIO143	P	ETPUA29	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	D3
		A1	PCSC2	DSPI C peripheral chip select	O					
		A2	—	—	—					
		G	GPIO143	GPIO	I/O					
144	ETPUA30_PCSC3_ GPIO144	P	ETPUA30	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	C1
		A1	PCSC3	DSPI C peripheral chip select	O					
		A2	—	—	—					
		G	GPIO144	GPIO	I/O					
145	ETPUA31_PCSC4_ GPIO145	P	ETPUA31	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	C2
		A1	PCSC4	DSPI C peripheral chip select	O					
		A2	—	—	—					
		G	GPIO145	GPIO	I/O					
eTPU_B										
146	TCRCLKB_IRQ6_ GPIO146	P	TCRCLKB	eTPU B TCR clock	I	MH	V_{DDEH6}	—/Up	—/Up	T23
		A1	IRQ6	External interrupt request	I					
		A2	—	—	—					
		G	GPIO146	GPIO	I/O					
147	ETPUB0_ETPUB16_ GPIO147	P	ETPUB0	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	T24
		A1	ETPUB16	eTPU B channel (output only)	O					
		A2	—	—	—					
		G	GPIO147	GPIO	I/O					
148	ETPUB1_ETPUB17_ GPIO148	P	ETPUB1	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	T25
		A1	ETPUB17	eTPU B channel (output only)	O					
		A2	—	—	—					
		G	GPIO148	GPIO	I/O					

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location (416)
167	ETPUB20_ GPIO167	P	ETPUB20	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	V26
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO167	GPIO	I/O					
168	ETPUB21_ GPIO168	P	ETPUB21	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	V25
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO168	GPIO	I/O					
169	ETPUB22_ GPIO169	P	ETPUB22	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	V24
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO169	GPIO	I/O					
170	ETPUB23_ GPIO170	P	ETPUB23	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	W26
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO170	GPIO	I/O					
171	ETPUB24_ GPIO171	P	ETPUB24	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	W25
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO171	GPIO	I/O					
172	ETPUB25_ GPIO172	P	ETPUB25	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	W24
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO172	GPIO	I/O					

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location (416)
173	ETPUB26_ GPIO173	P	ETPUB26	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	V23
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO173	GPIO	I/O					
174	ETPUB27_ GPIO174	P	ETPUB27	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	Y25
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO174	GPIO	I/O					
175	ETPUB28_ GPIO175	P	ETPUB28	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	Y24
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO175	GPIO	I/O					
176	ETPUB29_ GPIO176	P	ETPUB29	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	Y23
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO176	GPIO	I/O					
177	ETPUB30_ GPIO177	P	ETPUB30	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	AA24
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO177	GPIO	I/O					
178	ETPUB31_ GPIO178	P	ETPUB31	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	AB24
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO178	GPIO	I/O					

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location (416)
446	ETPUC5_ GPIO446[9]	P	—	—	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	E25
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO446	GPIO	I/O					
447	ETPUC6_ GPIO447[9]	P	—	—	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	E26
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO447	GPIO	I/O					
448	ETPUC7_ GPIO448[9]	P	—	—	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F23
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO448	GPIO	I/O					
449	ETPUC8_ GPIO449[9]	P	—	—	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F24
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO449	GPIO	I/O					
450	ETPUC9_IRQ0_ GPIO450[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F25
		A1	IRQ0	External interrupt request	I					
		A2	—	—	—					
		G	GPIO450	GPIO	I/O					
451	ETPUC10__IRQ1_ GPIO451[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F26
		A1	IRQ1	External interrupt request	I					
		A2	—	—	—					
		G	GPIO451	GPIO	I/O					

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location (416)
452	ETPUC11_IRQ2_ GPIO452[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	G23
		A1	IRQ2	External interrupt request	I					
		A2	—	—	—					
		G	GPIO452	GPIO	I/O					
453	ETPUC12_IRQ3_ GPIO453[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	G24
		A1	IRQ3	External interrupt request	I					
		A2	—	—	—					
		G	GPIO453	GPIO	I/O					
454	ETPUC13_3_IRQ4_ GPIO454[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	G25
		A1	IRQ4	External interrupt request	I					
		A2	—	—	—					
		G	GPIO454	GPIO	I/O					
455	ETPUC14_4_IRQ5_ GPIO455[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	G26
		A1	IRQ5	External interrupt request	I					
		A2	—	—	—					
		G	GPIO455	GPIO	I/O					
456	ETPUC15__ GPIO456[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	H23
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO456	GPIO	I/O					
457	ETPUC16_FR_A_TX_ GPIO457[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	H24
		A1	FR_A_TX	FlexRay A transfer	O					
		A2	—	—	—					
		G	GPIO457	GPIO	I/O					

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location (416)
469	ETPUC28_PCSD0_ GPIO469[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	L24
		A1	PCSD0	DSPI D peripheral chip select	I/O					
		A2	—	—	—					
		G	GPIO469	GPIO	I/O					
470	ETPUC29_SCKD_ GPIO470[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	L25
		A1	SCKD	DSPI D clock	I/O					
		A2	—	—	—					
		G	GPIO470	GPIO	I/O					
471	ETPUC30_SOUTD_ GPIO471[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	L26
		A1	SOUTD	DSPI D data output	O					
		A2	—	—	—					
		G	GPIO471	GPIO	I/O					
472	ETPUC31_SIND_ GPIO472[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	M23
		A1	SIND	DSPI D data input	I					
		A2	—	—	—					
		G	GPIO472	GPIO	I/O					
eMIOS										
179	EMIOS0_ETPUA0_ GPIO179	P	EMIOS0	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AE10
		A1	ETPUA0	eTPU A channel	O					
		A2	—	—	—					
		G	GPIO179	GPIO	I/O					
180	EMIOS1_ETPUA1_ GPIO180	P	EMIOS1	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AF10
		A1	ETPUA1	eTPU A channel	O					
		A2	—	—	—					
		G	GPIO180	GPIO	I/O					

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location (416)
187	EMIOS8_ETPUA8_ GPIO187	P	EMIOS8	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AC13
		A1	ETPUA8	eTPU A channel	O					
		A2	—	—	—					
		G	GPIO187	GPIO	I/O					
188	EMIOS9_ETPUA9_ GPIO188	P	EMIOS9	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AD13
		A1	ETPUA9	eTPU A channel	O					
		A2	—	—	—					
		G	GPIO188	GPIO	I/O					
189	EMIOS10_SCKD_ GPIO189	P	EMIOS10	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AE13
		A1	SCKD	DSPI D clock	O					
		A2	—	—	—					
		G	GPIO189	GPIO	I/O					
190	EMIOS11_SIND_ GPIO190	P	EMIOS11	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AF13
		A1	SIND	DSPI D data input	I					
		A2	—	—	—					
		G	GPIO190	GPIO	I/O					
191	EMIOS12_SOUTC_ GPIO191	P	EMIOS12	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AF14
		A1	SOUTC	DSPI C data output	O					
		A2	—	—	—					
		G	GPIO191	GPIO	I/O					
192	EMIOS13_SOUTD_ GPIO192	P	EMIOS13	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AE14
		A1	SOUTD	DSPI D data output	O					
		A2	—	—	—					
		G	GPIO192	GPIO	I/O					

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location (416)
193	EMIOS14_IRQ0_ GPIO193	P	EMIOS14	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AC14
		A1	IRQ0	External interrupt request	I					
		A2	CNTXD	FlexCAN D transmit	O					
		G	GPIO193	GPIO	I/O					
194	EMIOS15_IRQ1_ GPIO194	P	EMIOS15	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AD14
		A1	IRQ1	External interrupt request	I					
		A2	CNRXD	FlexCAN D receive	I					
		G	GPIO194	GPIO	I/O					
195	EMIOS16_ETPUB0_ GPIO195	P	EMIOS16	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AF15
		A1	ETPUB0	eTPU B channel	O					
		A2	FR_DBG[3]	FlexRay debug	O					
		G	GPIO195	GPIO	I/O					
196	EMIOS17_ETPUB1_ GPIO196	P	EMIOS17	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AE15
		A1	ETPUB1	eTPU B channel	O					
		A2	FR_DBG[2]	FlexRay debug	O					
		G	GPIO196	GPIO	I/O					
197	EMIOS18_ETPUB2_ GPIO197	P	EMIOS18	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AC15
		A1	ETPUB2	eTPU B channel	O					
		A2	FR_DBG[1]	FlexRay debug	O					
		G	GPIO197	GPIO	I/O					
198	EMIOS19_ETPUB3_ GPIO198	P	EMIOS19	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AD15
		A1	ETPUB3	eTPU B channel	O					
		A2	FR_DBG[0]	FlexRay debug	O					
		G	GPIO198	GPIO	I/O					

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location (416)
199	EMIOS20_ETPUB4_ GPIO199	P	EMIOS20	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AF16
		A1	ETPUB4	eTPU B channel	O					
		A2	—	—	—					
		G	GPIO199	GPIO	I/O					
200	EMIOS21_ETPUB5_ GPIO200	P	EMIOS21	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AE16
		A1	ETPUB5	eTPU B channel	O					
		A2	—	—	—					
		G	GPIO200	GPIO	I/O					
201	EMIOS22_ETPUB6_ GPIO201	P	EMIOS22	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AC16
		A1	ETPUB6	eTPU B channel	O					
		A2	—	—	—					
		G	GPIO201	GPIO	I/O					
202	EMIOS23_ETPUB7_ GPIO202	P	EMIOS23	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AD16
		A1	ETPUB7	eTPU B channel	O					
		A2	—	—	—					
		G	GPIO202	GPIO	I/O					
203	EMIOS24_PCSB0_ GPIO203	P	EMIOS24	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AF17
		A1	PCSB0	DSPI B peripheral chip select	I/O					
		A2	—	—	—					
		G	GPIO203	GPIO	I/O					
204	EMIOS25_PCSB1_ GPIO204	P	EMIOS25	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AE17
		A1	PCSB1	DSPI B peripheral chip select	O					
		A2	—	—	—					
		G	GPIO204	GPIO	I/O					

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location (416)
250	FR_A_TX_EN_ GPIO250	P	FR_A_TX_EN	FlexRay A transfer enable	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AF3
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO250	GPIO	I/O					
251	FR_B_TX_ GPIO251	P	FR_B_TX	FlexRay B transfer	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AD5
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO251	GPIO	I/O					
252	FR_B_RX_ GPIO252	P	FR_B_RX	FlexRay B receive	I	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AE4
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO252	GPIO	I/O					
253	FR_B_TX_EN_ GPIO253	P	FR_B_TX_EN	FlexRay B transfer enable	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AF4
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO253	GPIO	I/O					
FlexCAN										
83	CNTXA_TXDA_ GPIO83	P	CNTXA	FlexCAN A transmit	O	MH	V_{DDEH4}	—/Up	—/Up	AF19
		A1	TXDA	eSCI A transmit	O					
		A2	—	—	—					
		G	GPIO83	GPIO	I/O					
84	CNRXA_RXDA_ GPIO84	P	CNRXA	FlexCAN A receive	I	MH	V_{DDEH4}	—/Up	—/Up	AE19
		A1	RXDA	eSCI A receive	I					
		A2	—	—	—					
		G	GPIO84	GPIO	I/O					

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location (416)
240	PCSC2_GPIO240	P	PCSC2	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	—/Up	AE23
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO240	GPIO	I/O					
241	PCSC3_GPIO241	P	PCSC3	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	—/Up	AD23
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO241	GPIO	I/O					
242	PCSC4_GPIO242	P	PCSC4	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	—/Up	AF24
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO242	GPIO	I/O					
243	PCSC5_GPIO243	P	PCSC5	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	—/Up	AE24
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO243	GPIO	I/O					
Reset and Clocks										
—	RESET	P	RESET	External reset input	I	MH	V_{DDEH1}	RESET/Up	RESET/Up	R2
230	RSTOUT	P	RSTOUT	External reset output	O	MH	V_{DDEH1}	RSTOUT/Low	RSTOUT/ High	A3
212	BOOTCFG1_IRQ3_ GPIO212	P	BOOTCFG1	Boot configuration	I	MH	V_{DDEH1}	BOOTCFG/ Down	Input/Down	N2
		A1	IRQ3	External interrupt request	I					
		A2	—	—	—					
		G	GPIO212	GPIO	I/O					

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location (416)
220	MDO0_GPIO220 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO0[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	MDO0/Low	U3
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO220	GPIO	I/O					
221	MDO1_GPIO221 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO1[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	U4
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO221	GPIO	I/O					
222	MDO2_GPIO222 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO2[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	V1
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO222	GPIO	I/O					
223	MDO3_GPIO223 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO3[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	V2
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO223	GPIO	I/O					
75	MDO4_GPIO75 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO4[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	V3
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO75	GPIO	I/O					
76	MDO5_GPIO76 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO5[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	V4
		A1	—	—	—					
		A2	—	—	—					
		G	GPIO76	GPIO	I/O					

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location (416)
—	TEST	—	TEST	Test mode select (not for customer use)	I	F	V_{DDEH1}	TEST/Down	TEST/Down	B4
—	VDDSYN	—	VDDSYN	Clock synthesizer power input	I	VDDE	V_{DDSYN}	VDDSYN	VDDSYN	AD26
—	VSSSYN	—	VSSSYN	Clock synthesizer ground input	I	VSSE	V_{DDSYN}	VSSSYN	VSSSYN	AA26
—	VSTBY	—	VSTBY	SRAM standby power input	I	VHV	V_{DDEH1}	VSTBY	VSTBY	M4
—	REGSEL	—	REGSEL	Selects regulator mode (Linear/Switch mode)	I	AE	V_{DDREG}	REGSEL	REGSEL	W23
—	REGCTL	—	REGCTL	Regulator controller output to base/gate of power transistor	O	AE	V_{DDREG}	REGCTL	REGCTL	Y26
—	VSSFL	—	VSSFL	Tie to V_{SS}	I	VSS	V_{DDREG}	VSSFL	VSSFL	AB25
—	VDDREG	—	VDDREG	Source voltage for on-chip regulators and Low voltage detect circuits	I	VDDINT	V_{DDREG}	VDDREG	VDDREG	AA25

1 The GPIO number is the same as the corresponding pad configuration register (SIU_PCRn) number in pins that have GPIO functionality. For pins that do not have GPIO functionality, this number is the PCR number.

2 The primary signal name is used as the pin label on the BGA map for identification purposes. However, the primary signal function is not available on all devices and is indicated by a dash in the following table columns: Signal Functions, P/F/G, and I/O Type.

3 P/A/G stands for Primary/Alternate/GPIO. This column indicates which function on a pin is Primary, Alternate 1, Alternate 2, (Alternate *n*) and GPIO.

4 Each line in the Function column corresponds to a separate signal function on the pin. For all device I/O pins, the primary, alternate, or GPIO signal functions are designated in the PA field of the SIU_PCRn registers except where explicitly noted.

5 MH = High voltage, medium speed
F = Fast speed
FS = Fast speed with slew
AE = Analog with ESD protection circuitry (up/down = pull up and pull down circuits included in the pad)
VHV = Very high voltage

6 VDDE (fast I/O) and VDDEH (slow I/O) power supply inputs are grouped into segments. Each segment of VDDEH pins can connect to a separate 3.3–5.0 V (+5%/–10%) power supply input. Each segment of VDDE pins can connect to a separate 1.8–3.3 V (±10%) power supply.

7 The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. The terminology used in this column is: O – output, I – input, Up – weak pull up enabled, Down – weak pulldown enabled, Low – output driven low, High – output driven high, ABS — Auto Baud Select (during Reset or until JCOMP assertion). A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin. The signal name to the left or right of the slash indicates the pin is enabled.

8 The Function After Reset of a GPI function is general purpose input. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin.

5.2.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the TEPBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm. of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road

Table 14. DSPI LVDS pad specification (continued)

9	Diff Skew Itphla-tplhbI or Itplhb-tphlaI	T_{SKEW}	—	—	—	0.5	ns
Termination							
10	Trans. Line (differential Zo)	—	—	95	100	105	ohms
11	Temperature	—	—	–40	—	150	°C

5.8 Oscillator and FMPLL electrical characteristics

Table 15. FMPLL Electrical Specifications[1]

(V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H)

Spec	Characteristic	Symbol	Min	Max	Unit
1	PLL Reference Frequency Range[2] (Normal Mode) Crystal Reference (PLLCFG2 = 0b0) Crystal Reference (PLLCFG2 = 0b1) External Reference (PLLCFG2 = 0b0) External Reference (PLLCFG2 = 0b1)	 $f_{ref\_crystal}$ $f_{ref\_crystal}$ f_{ref_ext} f_{ref_ext}	 8 16 8 16	 20 40[3] 20 40	MHz
2	Loss of Reference Frequency[4]	f_{LOR}	100	1000	kHz
3	Self Clocked Mode Frequency[5]	f_{SCM}	4	16	MHz
4	PLL Lock Time[6]	t_{LPLL}	—	< 400	µs
5	Duty Cycle of Reference [7]	t_{DC}	40	60	%
6	Frequency un-LOCK Range	f_{UL}	–4.0	4.0	% f_{sys}
7	Frequency LOCK Range	f_{LCK}	–2.0	2.0	% f_{sys}
8	D_CLKOUT Period Jitter[8, 9] Measured at f_{SYS} Max Cycle-to-cycle Jitter	C_{Jitter}	–5	5	%f_{clkout}
9	Peak-to-Peak Frequency Modulation Range Limit [10,11] (f_{sys} Max must not be exceeded)	C_{mod}	0	4	%f_{sys}
10	FM Depth Tolerance[12]	C_{mod_err}	–0.25	0.25	%f_{sys}
11	VCO Frequency	f_{VCO}	192	600	MHz
12	Modulation Rate Limits[13]	f_{mod}	0.400	1	MHz
13	Predivider output frequency range[14]	f_{prediv}	4	10	MHz

1 All values given are initial design targets and subject to change.

2 Crystal and External reference frequency limits depend on device relying on PLL to lock prior to release of reset, default PREDIV/EPREDIV, MFD/EMFD default settings, and VCO frequency range. Absolute minimum loop frequency is 4 MHz.

3 Upper tolerance of less than 1% is allowed on 40MHz crystal.

4 “Loss of Reference Frequency” is the reference frequency detected internally, which transitions the PLL into self clocked mode.

5 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR}. This frequency is measured at D_CLKOUT. A default RFD value of (0x05) is used in SCM mode, and the programmed MFD and RFD values have no effect

5.9 eQADC electrical characteristics

Table 17. eQADC Conversion Specifications (Operating)

Spec	Characteristic	Symbol	Min	Max	Unit
1	ADC Clock (ADCLK) Frequency	f_{ADCLK}	2	16	MHz
2	Conversion Cycles Single Ended Conversion Cycles 12 bit resolution Single Ended Conversion Cycles 10 bit resolution Single Ended Conversion Cycles 8 bit resolution **Note:** Differential conversion (min) is one clock cycle less than the single-ended conversion values listed here.	CC	 2 + 14 2 + 12 2 + 10	 128 + 14 128 + 12 128 + 10	ADCLK cycles
3	Stop Mode Recovery Time[1]	T_{SR}	10	—	µs
4	Resolution[2]	—	1.25	—	mV
5	INL: 8 MHz ADC Clock[3]	INL8	–4[4]	4[4]	LSB[5]
6	INL: 16 MHz ADC Clock[3]	INL16	–8[4]	8[4]	LSB
7	DNL: 8 MHz ADC Clock[3]	DNL8	–3[4]	3[4]	LSB
8	DNL: 16 MHz ADC Clock[3]	DNL16	–3[4]	3[4]	LSB
9	Offset Error without Calibration	OFFNC	0[4]	100[4]	LSB
10	Offset Error with Calibration	OFFWC	–4[4]	4[4]	LSB
11	Full Scale Gain Error without Calibration	GAINNC	–120[4]	0[4]	LSB
12	Full Scale Gain Error with Calibration	GAINWC	–4[4,6]	4[4,6]	LSB
13	Non-Disruptive Input Injection Current [7, 8, 9, 10]	I_{INJ}	–3	3	mA
14	Incremental Error due to injection current[11, 12]	E_{INJ}	–4[4]	4[4]	Counts
15	TUE value at 8 MHz [13, 14] (with calibration)	TUE8	–4[4,6]	4[4,6]	Counts
16	TUE value at 16 MHz [13, 14] (with calibration)	TUE16	–8	8	Counts
17	Maximum differential voltage[15] (DANx+ - DANx-) or (DANx- - DANx+) PREGAIN set to 1X setting PREGAIN set to 2X setting PREGAIN set to 4X setting	 $DIFF_{max}$ $DIFF_{max2}$ $DIFF_{max4}$	 — — —	 $(V_{RH} – V_{RL})/2$ $(V_{RH} – V_{RL})/4$ $(V_{RH} - V_{RL})/8$	 V V V
18	Differential input Common mode voltage[15] (DANx- + DANx+)/2	$DIFF_{cmv}$	$(V_{RH} – V_{RL})/2$ – 5%	$(V_{RH} – V_{RL})/2$ + 5%	V

1 Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions. Delay from power up to full accuracy = 8 ms.

2 At $V_{RH} – V_{RL}$ = 5.12 V, one count = 1.25 mV without using pregain.

3 INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} – 50 LSB. The eQADC is guaranteed to be monotonic at 10 bit accuracy (12 bit resolution selected).

4 New design target. Actual specification will change following characterization. Margin for manufacturing has not been fully included.

5 At $V_{RH} – V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

6 The value is valid at 8 MHz, it is ±8 counts at 16 Mhz.

7 Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. Other channels are not affected by non-disruptive conditions.

5.10 C90 flash memory electrical characteristics

Table 22. Flash program and erase specifications

Spec	Characteristic	Symbol	Min	Typ[1]	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time[4]	$t_{dwprogram}$	—	38	—	500	µs
2	Page Program Time[4,5]	$t_{pprogram}$	—	45	160	500	µs
3	16 KB Block Pre-program and Erase Time	$t_{16kpperase}$	—	270	1000	5000	ms
4	64 KB Block Pre-program and Erase Time	$t_{64kpperase}$	—	800	1800	5000	ms
5	128 KB Block Pre-program and Erase Time	$t_{128kpperase}$	—	1500	2600	7500	ms
6	256 KB Block Pre-program and Erase Time	$t_{256kpperase}$	—	3000	5200	15000	ms

1 Typical program and erase times assume nominal supply values and operation at 25 ^{o}C.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 ^{o}C, typical supply voltage, 80 MHz minimum system frequency.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 Program times are actual hardware programming times and do not include software overhead.

5 Page size is 128 bits (4 words).

Table 23. Flash EEPROM module life

Spec	Characteristic	Symbol	Min	Typical[1]	Unit
1	Number of program/erase cycles per block for 16 KB and 64 KB blocks over the operating temperature range (T_J)	P/E	100,000	—	cycles
2	Number of program/erase cycles per block for 128 KB and 256 KB blocks over the operating temperature range (T_J)	P/E	1,000	100,000	cycles
3	Minimum Data Retention at 85 °C ambient temperature[2] Blocks with 0–1,000 P/E cycles Blocks with 1,001–10,000 P/E cycles Blocks with 10,001–100,000 P/E cycles	Retention	 20 10 5	 — — —	years

1 Typical endurance is evaluated at 25 °C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

2 Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

Table 24 shows the Platform Flash Configuration Register 1 (PFCPR1) settings versus frequency of operation. Refer to the device reference manual for definitions of these bit fields.

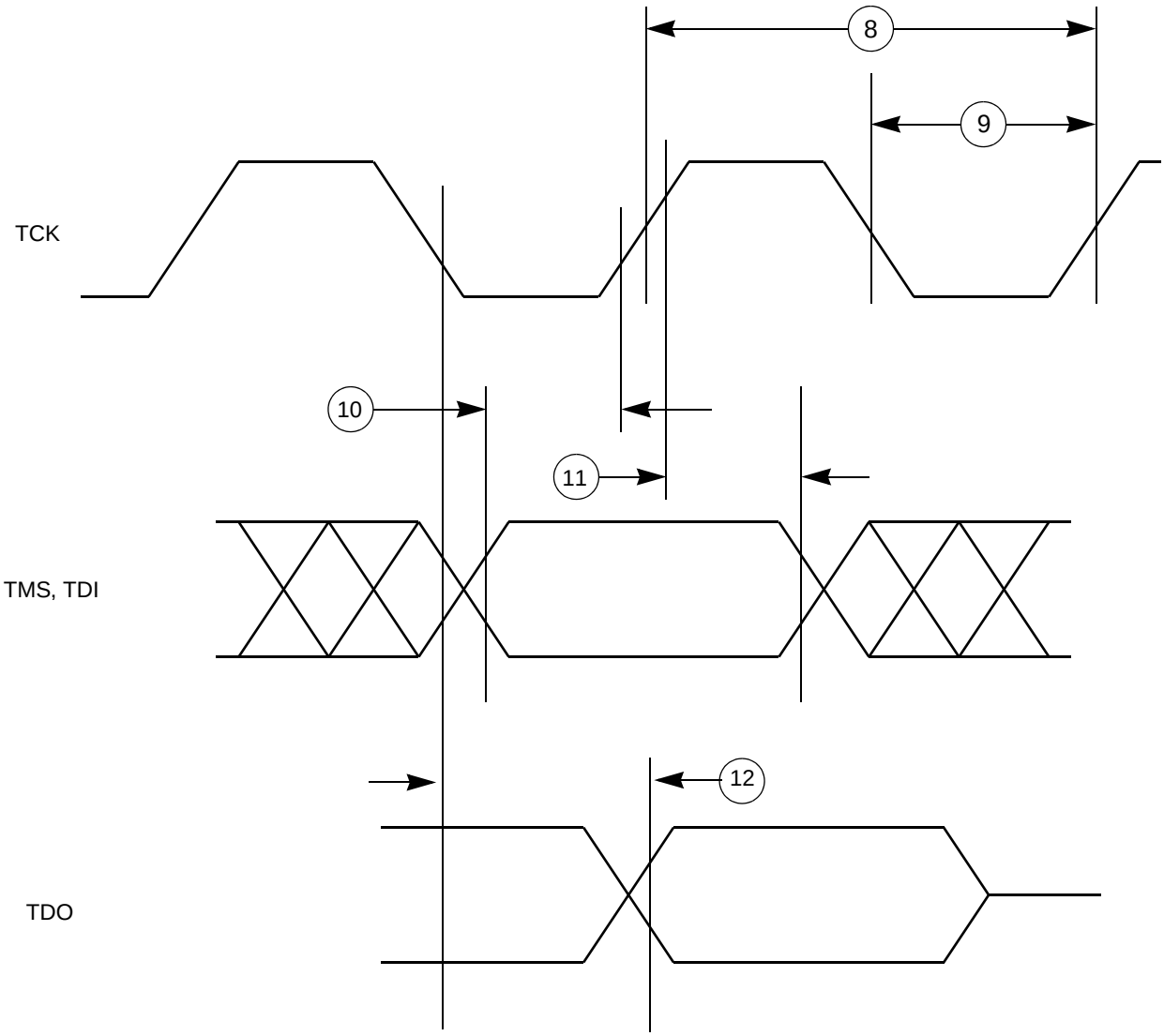


Figure 18. Nexus TCK, TDI, TMS, TDO timing

7 Package information

7.1 416-pin package

The package drawings of the 416-pin TEPBGA package are shown in Figure 36 and Figure 37.

Figure 36. 416 TEPBGA package (1 of 2)