**What is "Embedded - Microcontrollers"?**

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

**Applications of "Embedded - Microcontrollers"**

### Details

| | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, LINbus, SPI, TSI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT |
| Number of I/O | 54 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D - 16bit; D/A - 12bit |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl16z256vlh4r |

# Table of Contents

# 1 Ratings

## 1.1 Thermal handling ratings

**Table 1.  Thermal handling ratings**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | −55 | 150 | °C | 1 |
| $T_{SDR}$ | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.2 Moisture handling ratings

**Table 2.  Moisture handling ratings**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.3 ESD handling ratings

**Table 3.  ESD handling ratings**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{HBM}$ | Electrostatic discharge voltage, human body model | −2000 | +2000 | V | 1 |
| $V_{CDM}$ | Electrostatic discharge voltage, charged-device model | −500 | +500 | V | 2 |
| $I_{LAT}$ | Latch-up current at ambient temperature of 105 °C | −100 | +100 | mA | 3 |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

**Table 6.  V$_{DD}$ supply LVD and POR operating requirements (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| V$_{LVW1H}$ | • Level 1 falling (LVWV = 00) | 2.62 | 2.70 | 2.78 | V | |
| V$_{LVW2H}$ | • Level 2 falling (LVWV = 01) | 2.72 | 2.80 | 2.88 | V | |
| V$_{LVW3H}$ | • Level 3 falling (LVWV = 10) | 2.82 | 2.90 | 2.98 | V | |
| V$_{LVW4H}$ | • Level 4 falling (LVWV = 11) | 2.92 | 3.00 | 3.08 | V | |
| V$_{HYSH}$ | Low-voltage inhibit reset/recover hysteresis — high range | — | ±60 | — | mV | — |
| V$_{LVDL}$ | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | — |
| | Low-voltage warning thresholds — low range | | | | | 1 |
| V$_{LVW1L}$ | • Level 1 falling (LVWV = 00) | 1.74 | 1.80 | 1.86 | V | |
| V$_{LVW2L}$ | • Level 2 falling (LVWV = 01) | 1.84 | 1.90 | 1.96 | V | |
| V$_{LVW3L}$ | • Level 3 falling (LVWV = 10) | 1.94 | 2.00 | 2.06 | V | |
| V$_{LVW4L}$ | • Level 4 falling (LVWV = 11) | 2.04 | 2.10 | 2.16 | V | |
| V$_{HYSL}$ | Low-voltage inhibit reset/recover hysteresis — low range | — | ±40 | — | mV | — |
| V$_{BG}$ | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | — |
| t$_{LPO}$ | Internal low power oscillator period — factory trimmed | 900 | 1000 | 1100 | µs | — |

1. Rising thresholds are falling threshold + hysteresis voltage

## 2.2.3  Voltage and current operating behaviors

**Table 7.  Voltage and current operating behaviors**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| V$_{OH}$ | Output high voltage — Normal drive pad (except RESET_b)<br>• 2.7 V ≤ V$_{DD}$ ≤ 3.6 V, I$_{OH}$ = -5 mA<br>• 1.71 V ≤ V$_{DD}$ ≤ 2.7 V, I$_{OH}$ = -2.5 mA | V$_{DD}$ − 0.5<br>V$_{DD}$ − 0.5 | —<br>— | V<br>V | 1, 2 |
| V$_{OH}$ | Output high voltage — High drive pad (except RESET_b)<br>• 2.7 V ≤ V$_{DD}$ ≤ 3.6 V, I$_{OH}$ = -20 mA<br>• 1.71 V ≤ V$_{DD}$ ≤ 2.7 V, I$_{OH}$ = -10 mA | V$_{DD}$ − 0.5<br>V$_{DD}$ − 0.5 | —<br>— | V<br>V | 1, 2 |
| I$_{OHT}$ | Output high current total for all ports | — | 100 | mA | |
| V$_{OL}$ | Output low voltage — Normal drive pad<br>• 2.7 V ≤ V$_{DD}$ ≤ 3.6 V, I$_{OL}$ = 5 mA<br>• 1.71 V ≤ V$_{DD}$ ≤ 2.7 V, I$_{OL}$ = 2.5 mA | —<br>— | 0.5<br>0.5 | V<br>V | 1 |

*Table continues on the next page...*

## Table 9. Power consumption operating behaviors (continued)

| Symbol | Description | | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|
| $I_{DD\_LLS}$ | Low leakage stop mode current at 3.0 V | at 25 °C | 2.00 | 2.7 | µA | — |
| | | at 50 °C | 3.96 | 5.14 | µA | |
| | | at 70 °C | 7.77 | 10.71 | µA | |
| | | at 85 °C | 14.15 | 18.79 | µA | |
| | | at 105 °C | 33.20 | 43.67 | µA | |
| $I_{DD\_VLLS3}$ | Very low-leakage stop mode 3 current at 3.0 V | at 25 °C | 1.5 | 2.2 | µA | — |
| | | at 50 °C | 2.83 | 3.55 | µA | |
| | | at 70 °C | 5.53 | 7.26 | µA | |
| | | at 85 °C | 9.92 | 12.71 | µA | |
| | | at 105 °C | 22.90 | 29.23 | µA | |
| $I_{DD\_VLLS1}$ | Very low-leakage stop mode 1 current at 3.0V | at 25 °C | 0.71 | 1.2 | µA | — |
| | | at 50 °C | 1.27 | 1.9 | µA | |
| | | at 70 °C | 2.48 | 3.51 | µA | |
| | | at 85 °C | 4.65 | 6.29 | µA | |
| | | at 105 °C | 11.55 | 14.34 | µA | |
| $I_{DD\_VLLS0}$ | Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V | at 25 °C | 0.41 | 0.9 | µA | — |
| | | at 50 °C | 0.96 | 1.56 | µA | |
| | | at 70 °C | 2.17 | 3.1 | µA | |
| | | at 85 °C | 4.35 | 5.32 | µA | |
| | | at 105 °C | 11.24 | 14.00 | µA | |
| $I_{DD\_VLLS0}$ | Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V | at 25 °C | 0.23 | 0.69 | µA | 7 |
| | | at 50 °C | 0.77 | 1.35 | µA | |
| | | at 70 °C | 1.98 | 2.52 | µA | |
| | | at 85 °C | 4.16 | 5.14 | µA | |
| | | at 105 °C | 11.05 | 13.80 | µA | |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for PEE mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
3. MCG configured for FEI mode.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
6. MCG configured for BLPI mode.
7. No brownout.
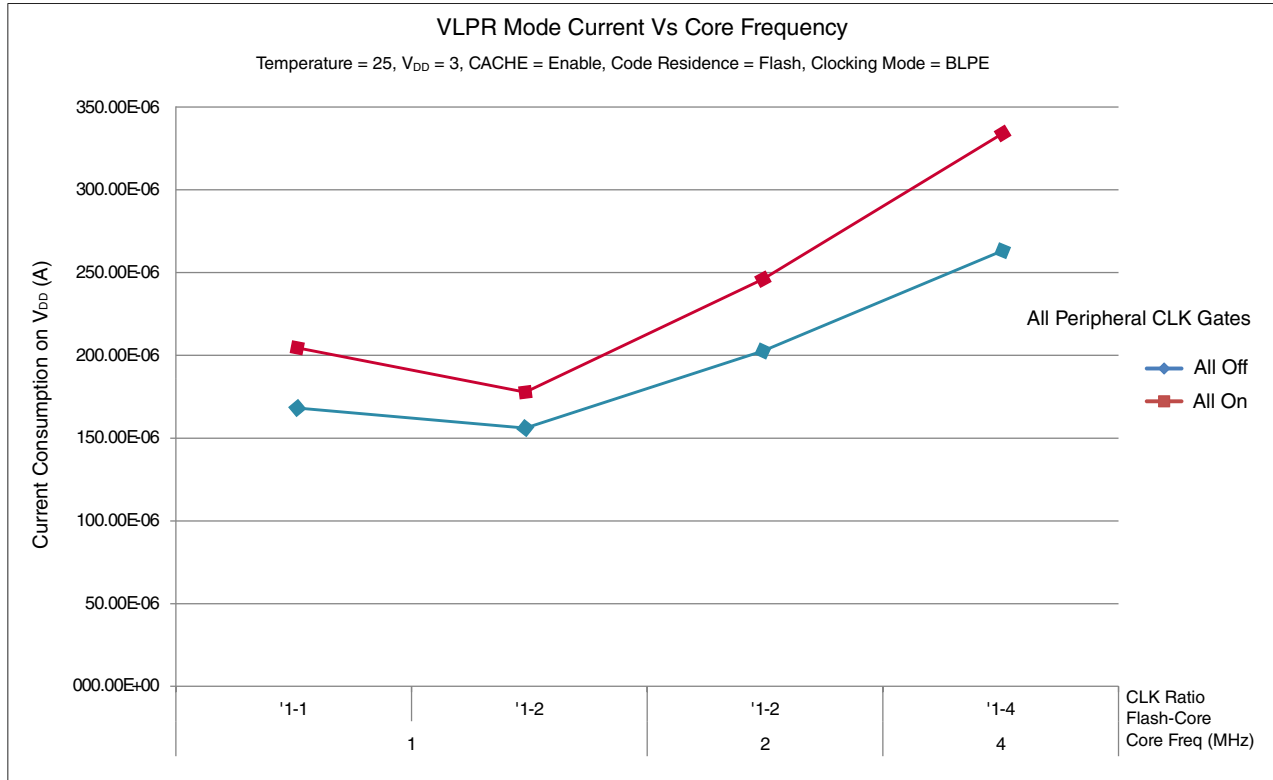
**Figure 4. VLPR mode current vs. core frequency**

### 2.2.6  EMC radiated emissions operating behaviors

**Table 11.  EMC radiated emissions operating behaviors**

| Symbol | Description | Frequency band (MHz) | Typ. | Unit | Notes |
|--------|-------------|----------------------|------|------|-------|
| $V_{RE1}$ | Radiated emissions voltage, band 1 | 0.15–50 | 12 | dBμV | 1,2 |
| $V_{RE2}$ | Radiated emissions voltage, band 2 | 50–150 | 8 | dBμV | |
| $V_{RE3}$ | Radiated emissions voltage, band 3 | 150–500 | 7 | dBμV | |
| $V_{RE4}$ | Radiated emissions voltage, band 4 | 500–1000 | 4 | dBμV | |
| $V_{RE\_IEC}$ | IEC level | 0.15–1000 | M | — | 2,3 |

1.  Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2.  $V_{DD}$ = 3.3 V, $T_A$ = 25 °C, $f_{OSC}$ = 8 MHz (crystal), $f_{SYS}$ = 48 MHz, $f_{BUS}$ = 24 MHz
3.  Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

**Table 19. Oscillator DC electrical specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | | — | 0 | — | kΩ | |
| $V_{pp}$[5] | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |

1. $V_{DD}$=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. $C_x$,$C_y$ can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, $R_F$ is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

### 3.3.2.2 Oscillator frequency specifications

**Table 20. Oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc\_lo}$ | Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| $f_{osc\_hi\_1}$ | Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01) | 3 | — | 8 | MHz | |
| $f_{osc\_hi\_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| $f_{ec\_extal}$ | Input clock frequency (external clock mode) | — | — | 48 | MHz | 1, 2 |
| $t_{dc\_extal}$ | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| $t_{cst}$ | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | 750 | — | ms | 3, 4 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | 250 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

# 3.4 Memories and memory interfaces

## 3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

### 3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 21. NVM program/erase timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|-------------|------|------|------|------|-------|
| $t_{hvpgm4}$ | Longword Program high-voltage time | — | 7.5 | 18 | µs | — |
| $t_{hversscr}$ | Sector Erase high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversblk128k}$ | Erase Block high-voltage time for 128 KB | — | 52 | 452 | ms | 1 |
| $t_{hversall}$ | Erase All high-voltage time | — | 52 | 452 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

### 3.4.1.2 Flash timing specifications — commands

**Table 22. Flash command timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|-------------|------|------|------|------|-------|
| $t_{rd1blk128k}$ | Read 1s Block execution time<br>• 128 KB program flash | — | — | 1.7 | ms | — |
| $t_{rd1sec1k}$ | Read 1s Section execution time (flash sector) | — | — | 60 | µs | 1 |
| $t_{pgmchk}$ | Program Check execution time | — | — | 45 | µs | 1 |
| $t_{rdrsrc}$ | Read Resource execution time | — | — | 30 | µs | 1 |
| $t_{pgm4}$ | Program Longword execution time | — | 65 | 145 | µs | — |
| $t_{ersblk128k}$ | Erase Flash Block execution time<br>• 128 KB program flash | — | 88 | 600 | ms | 2 |

*Table continues on the next page...*

**Table 25.  16-bit ADC operating conditions (continued)**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $C_{rate}$ | ADC conversion rate | 16-bit mode | | | | | 5 |
| | | No ADC hardware averaging | 37.037 | — | 461.467 | Ksps | |
| | | Continuous conversions enabled, subsequent conversion time | | | | | |

1. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25 °C, $f_{ADCK}$ = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The $R_{AS}/C_{AS}$ time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.
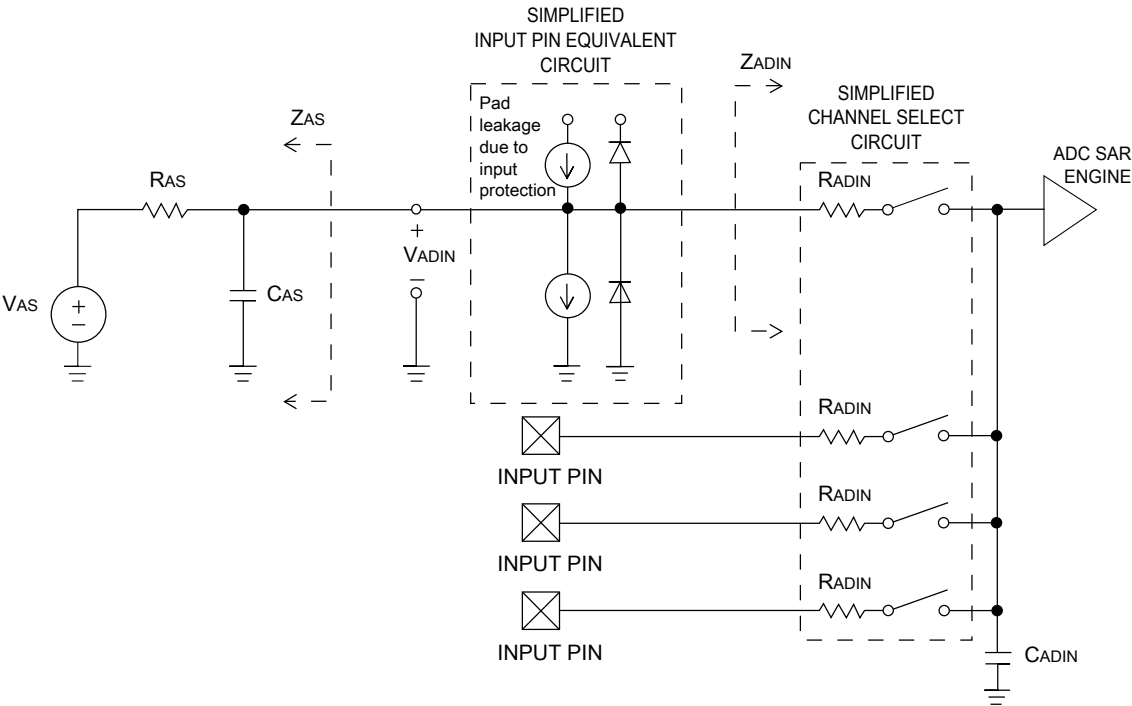


**Figure 7. ADC input impedance equivalency diagram**

## 3.6.1.2   16-bit ADC electrical characteristics

## Table 26.  16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

| Symbol | Description | Conditions[1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $I_{DDA\_ADC}$ | Supply current | | 0.215 | — | 1.7 | mA | 3 |
| $f_{ADACK}$ | ADC asynchronous clock source | • ADLPC = 1, ADHSC = 0<br>• ADLPC = 1, ADHSC = 1<br>• ADLPC = 0, ADHSC = 0<br>• ADLPC = 0, ADHSC = 1 | 1.2<br>2.4<br>3.0<br>4.4 | 2.4<br>4.0<br>5.2<br>6.2 | 3.9<br>6.1<br>7.3<br>9.5 | MHz<br>MHz<br>MHz<br>MHz | $t_{ADACK} = 1/f_{ADACK}$ |
| | Sample Time | See Reference Manual chapter for sample times | | | | | |
| TUE | Total unadjusted error | • 12-bit modes<br>• <12-bit modes | —<br>— | ±4<br>±1.4 | ±6.8<br>±2.1 | LSB[4] | 5 |
| DNL | Differential non-linearity | • 12-bit modes<br>• <12-bit modes | —<br>— | ±0.7<br>±0.2 | −1.1 to +1.9<br>−0.3 to 0.5 | LSB[4] | 5 |
| INL | Integral non-linearity | • 12-bit modes<br>• <12-bit modes | —<br>— | ±1.0<br>±0.5 | −2.7 to +1.9<br>−0.7 to +0.5 | LSB[4] | 5 |
| $E_{FS}$ | Full-scale error | • 12-bit modes<br>• <12-bit modes | —<br>— | −4<br>−1.4 | −5.4<br>−1.8 | LSB[4] | $V_{ADIN} = V_{DDA}$[5] |
| $E_Q$ | Quantization error | • 16-bit modes<br>• ≤13-bit modes | —<br>— | −1 to 0<br>— | —<br>±0.5 | LSB[4] | |
| ENOB | Effective number of bits | 16-bit differential mode<br>• Avg = 32<br>• Avg = 4<br><br>16-bit single-ended mode<br>• Avg = 32<br>• Avg = 4 | 12.8<br>11.9<br><br>12.2<br>11.4 | 14.5<br>13.8<br><br>13.9<br>13.1 | —<br>—<br><br>—<br>— | bits<br>bits<br><br>bits<br>bits | 6 |
| SINAD | Signal-to-noise plus distortion | See ENOB | 6.02 × ENOB + 1.76 | | | dB | |
| THD | Total harmonic distortion | 16-bit differential mode<br>• Avg = 32<br><br>16-bit single-ended mode<br>• Avg = 32 | —<br><br>— | -94<br><br>-85 | —<br><br>— | dB<br><br>dB | 7 |
| SFDR | Spurious free dynamic range | 16-bit differential mode | 82 | 95 | — | dB | 7 |

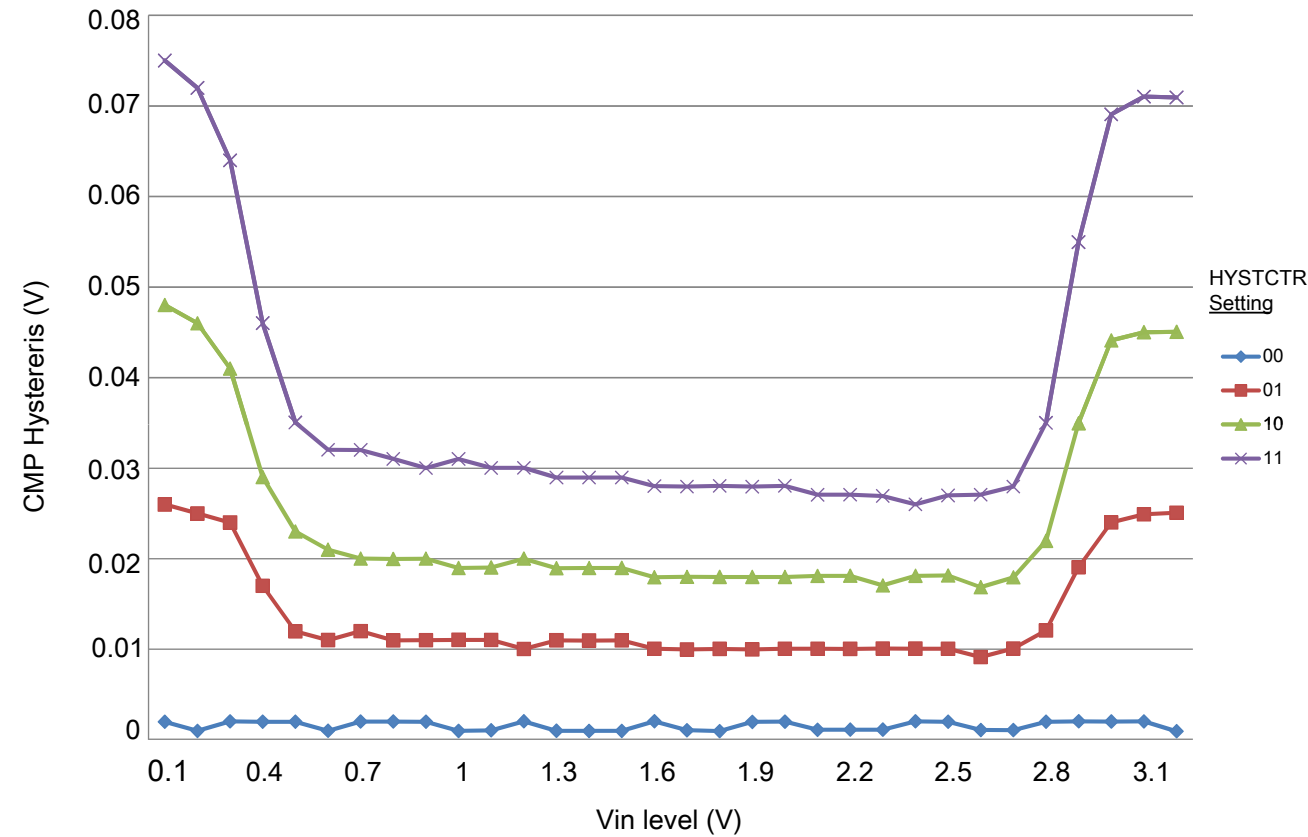*Table continues on the next page...*

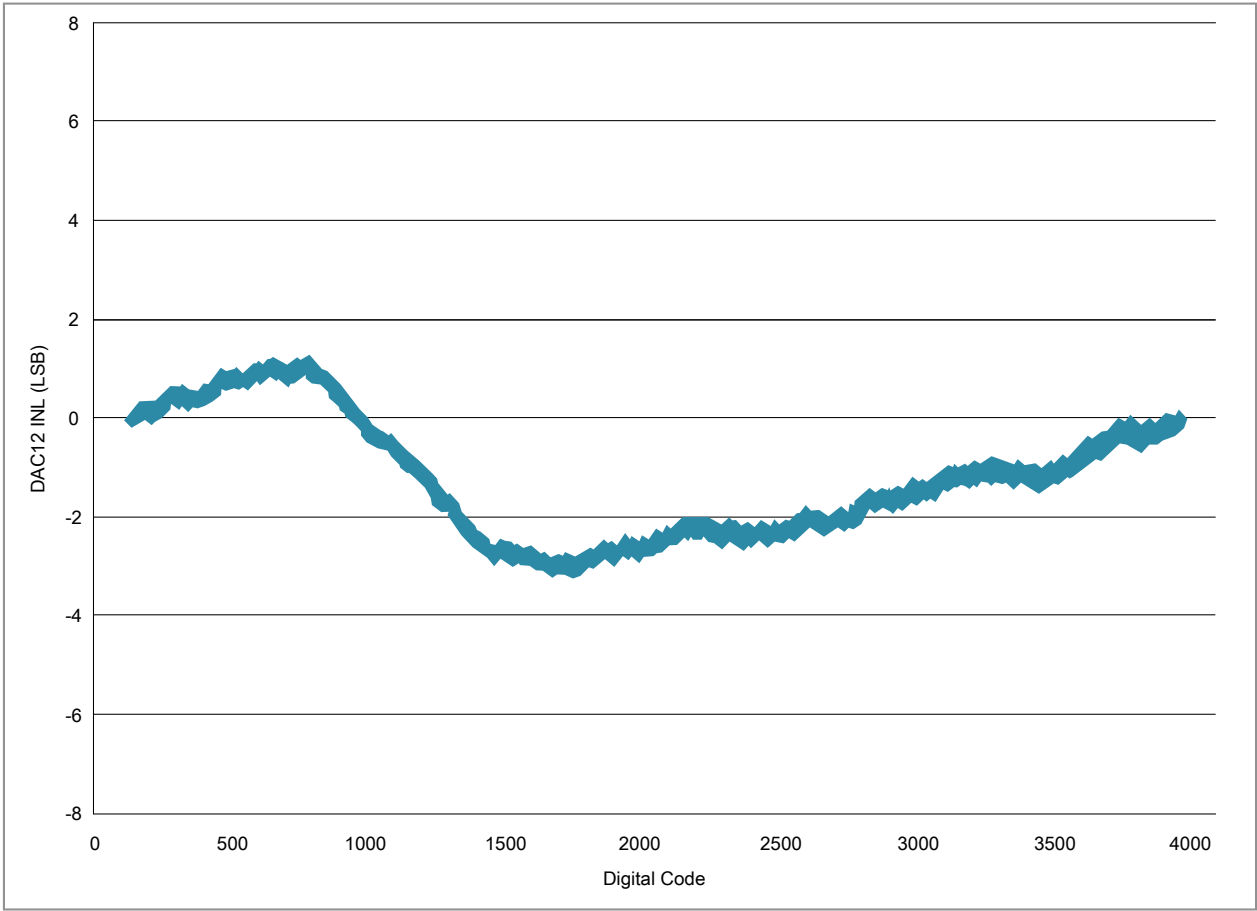**Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)**

**Figure 12. Typical INL error vs. digital code**

### 3.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% $V_{DD}$ and 80% $V_{DD}$ thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

**Table 30. SPI master mode timing on slew rate disabled pads**

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | $f_{periph}/2048$ | $f_{periph}/2$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | $2 \times t_{periph}$ | $2048 \times t_{periph}$ | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1/2 | — | $t_{SPSCK}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1/2 | — | $t_{SPSCK}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph}$ - 30 | $1024 \times t_{periph}$ | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 18 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 0 | — | ns | — |
| 8 | $t_v$ | Data valid (after SPSCK edge) | — | 15 | ns | — |
| 9 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 10 | $t_{RI}$ | Rise time input | — | $t_{periph}$ - 25 | ns | — |
|  | $t_{FI}$ | Fall time input |  |  |  |  |
| 11 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
|  | $t_{FO}$ | Fall time output |  |  |  |  |

1. For SPI0 $f_{periph}$ is the bus clock ($f_{BUS}$). For SPI1 $f_{periph}$ is the system clock ($f_{SYS}$).
2. $t_{periph} = 1/f_{periph}$

**Table 31. SPI master mode timing on slew rate enabled pads**

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | $f_{periph}/2048$ | $f_{periph}/2$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | $2 \times t_{periph}$ | $2048 \times t_{periph}$ | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1/2 | — | $t_{SPSCK}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1/2 | — | $t_{SPSCK}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph}$ - 30 | $1024 \times t_{periph}$ | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 96 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 0 | — | ns | — |

*Table continues on the next page...*
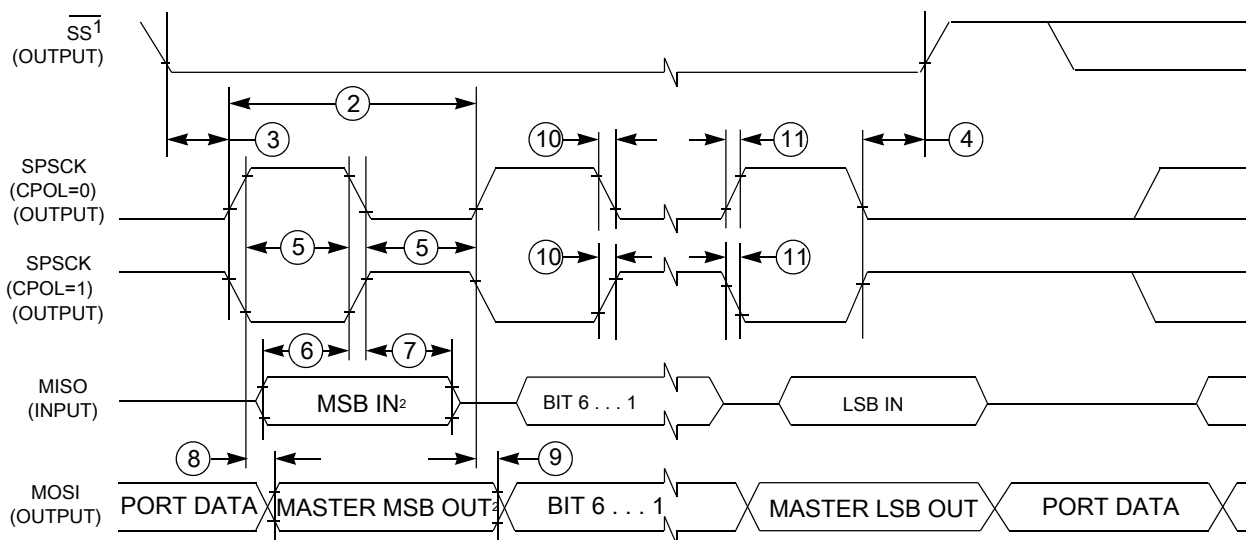
1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 15. SPI master mode timing (CPHA = 1)**

**Table 32.   SPI slave mode timing on slew rate disabled pads**

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | 0 | $f_{periph}/4$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | $4 \times t_{periph}$ | — | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1 | — | $t_{periph}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1 | — | $t_{periph}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph}$ - 30 | — | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 2.5 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 3.5 | — | ns | — |
| 8 | $t_a$ | Slave access time | — | $t_{periph}$ | ns | 3 |
| 9 | $t_{dis}$ | Slave MISO disable time | — | $t_{periph}$ | ns | 4 |
| 10 | $t_v$ | Data valid (after SPSCK edge) | — | 31 | ns | — |
| 11 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 12 | $t_{RI}$ | Rise time input | — | $t_{periph}$ - 25 | ns | — |
|  | $t_{FI}$ | Fall time input |  |  |  |  |
| 13 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
|  | $t_{FO}$ | Fall time output |  |  |  |  |

1. For SPI0 $f_{periph}$ is the bus clock ($f_{BUS}$). For SPI1 $f_{periph}$ is the system clock ($f_{SYS}$).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

### Table 36.   I2S/SAI slave mode timing

| Num. | Characteristic | Min. | Max. | Unit |
|------|----------------|------|------|------|
| | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 80 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 10 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 2 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | 33 | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 10 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 2 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid[1] | — | 28 | ns |

1.   Applies to first bit in each frame and only if the TCR4[FSE] bit is clear
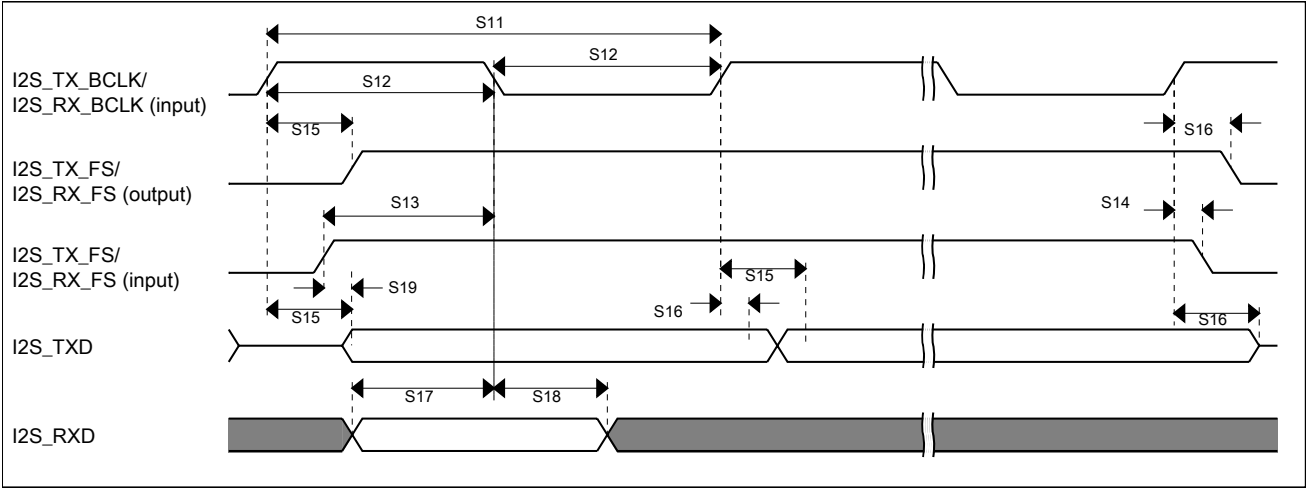


**Figure 20. I2S/SAI timing — slave modes**

## 3.8.4.2   VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

**Table 39. TSI electrical specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| TSI_RUNV | Variable power consumption in run mode (depends on oscillator's current selection) | 1.0 | — | 128 | µA |
| TSI_EN | Power consumption in enable mode | — | 100 | — | µA |
| TSI_DIS | Power consumption in disable mode | — | 1.2 | — | µA |
| TSI_TEN | TSI analog enable time | — | 66 | — | µs |
| TSI_CREF | TSI reference capacitor | — | 1.0 | — | pF |
| TSI_DVOLT | Voltage variation of VP & VM around nominal values | 0.19 | — | 1.03 | V |

# 4 Dimensions

## 4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **freescale.com** and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|---|---|
| 64-pin LQFP | 98ASS23234W |
| 64-pin MAPBGA | 98ASA00420D |

# 5 Pinout

## 5.1 KL16 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 64 BGA | 64 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | 1 | PTE0 | DISABLED | | PTE0 | SPI1_MISO | UART1_TX | RTC_CLKOUT | CMP0_OUT | I2C1_SDA | |
| B1 | 2 | PTE1 | DISABLED | | PTE1 | SPI1_MOSI | UART1_RX | | SPI1_MISO | I2C1_SCL | |

**Pinout**

| 64 BGA | 64 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| — | 3 | VDD | VDD | VDD | | | | | | | |
| C4 | 4 | VSS | VSS | VSS | | | | | | | |
| E1 | 5 | PTE16 | ADC0_DP1/ ADC0_SE1 | ADC0_DP1/ ADC0_SE1 | PTE16 | SPI0_PCS0 | UART2_TX | TPM_CLKIN0 | | | |
| D1 | 6 | PTE17 | ADC0_DM1/ ADC0_SE5a | ADC0_DM1/ ADC0_SE5a | PTE17 | SPI0_SCK | UART2_RX | TPM_CLKIN1 | | LPTMR0_ ALT3 | |
| E2 | 7 | PTE18 | ADC0_DP2/ ADC0_SE2 | ADC0_DP2/ ADC0_SE2 | PTE18 | SPI0_MOSI | | I2C0_SDA | SPI0_MISO | | |
| D2 | 8 | PTE19 | ADC0_DM2/ ADC0_SE6a | ADC0_DM2/ ADC0_SE6a | PTE19 | SPI0_MISO | | I2C0_SCL | SPI0_MOSI | | |
| G1 | 9 | PTE20 | ADC0_DP0/ ADC0_SE0 | ADC0_DP0/ ADC0_SE0 | PTE20 | | TPM1_CH0 | UART0_TX | | | |
| F1 | 10 | PTE21 | ADC0_DM0/ ADC0_SE4a | ADC0_DM0/ ADC0_SE4a | PTE21 | | TPM1_CH1 | UART0_RX | | | |
| G2 | 11 | PTE22 | ADC0_DP3/ ADC0_SE3 | ADC0_DP3/ ADC0_SE3 | PTE22 | | TPM2_CH0 | UART2_TX | | | |
| F2 | 12 | PTE23 | ADC0_DM3/ ADC0_SE7a | ADC0_DM3/ ADC0_SE7a | PTE23 | | TPM2_CH1 | UART2_RX | | | |
| F4 | 13 | VDDA | VDDA | VDDA | | | | | | | |
| G4 | 14 | VREFH | VREFH | VREFH | | | | | | | |
| G3 | 15 | VREFL | VREFL | VREFL | | | | | | | |
| F3 | 16 | VSSA | VSSA | VSSA | | | | | | | |
| H1 | 17 | PTE29 | CMP0_IN5/ ADC0_SE4b | CMP0_IN5/ ADC0_SE4b | PTE29 | | TPM0_CH2 | TPM_CLKIN0 | | | |
| H2 | 18 | PTE30 | DAC0_OUT/ ADC0_SE23/ CMP0_IN4 | DAC0_OUT/ ADC0_SE23/ CMP0_IN4 | PTE30 | | TPM0_CH3 | TPM_CLKIN1 | | | |
| H3 | 19 | PTE31 | DISABLED | | PTE31 | | TPM0_CH4 | | | | |
| H4 | 20 | PTE24 | DISABLED | | PTE24 | | TPM0_CH0 | | I2C0_SCL | | |
| H5 | 21 | PTE25 | DISABLED | | PTE25 | | TPM0_CH1 | | I2C0_SDA | | |
| D3 | 22 | PTA0 | SWD_CLK | TSI0_CH1 | PTA0 | | TPM0_CH5 | | | | SWD_CLK |
| D4 | 23 | PTA1 | DISABLED | TSI0_CH2 | PTA1 | UART0_RX | TPM2_CH0 | | | | |
| E5 | 24 | PTA2 | DISABLED | TSI0_CH3 | PTA2 | UART0_TX | TPM2_CH1 | | | | |
| D5 | 25 | PTA3 | SWD_DIO | TSI0_CH4 | PTA3 | I2C1_SCL | TPM0_CH0 | | | | SWD_DIO |
| G5 | 26 | PTA4 | NMI_b | TSI0_CH5 | PTA4 | I2C1_SDA | TPM0_CH1 | | | | NMI_b |
| F5 | 27 | PTA5 | DISABLED | | PTA5 | | TPM0_CH2 | | | I2S0_TX_ BCLK | |
| H6 | 28 | PTA12 | DISABLED | | PTA12 | | TPM1_CH0 | | | I2S0_TXD0 | |
| G6 | 29 | PTA13 | DISABLED | | PTA13 | | TPM1_CH1 | | | I2S0_TX_FS | |
| G7 | 30 | VDD | VDD | VDD | | | | | | | |
| H7 | 31 | VSS | VSS | VSS | | | | | | | |
| H8 | 32 | PTA18 | EXTAL0 | EXTAL0 | PTA18 | | UART1_RX | TPM_CLKIN0 | | | |

## 8.4   Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 8.4.1   Example

This is an example of an operating rating:

| Symbol | Description | Min. | Max. | Unit |
|--------|-------------|------|------|------|
| $V_{DD}$ | 1.0 V core supply voltage | −0.3 | 1.2 | V |

## 8.5   Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
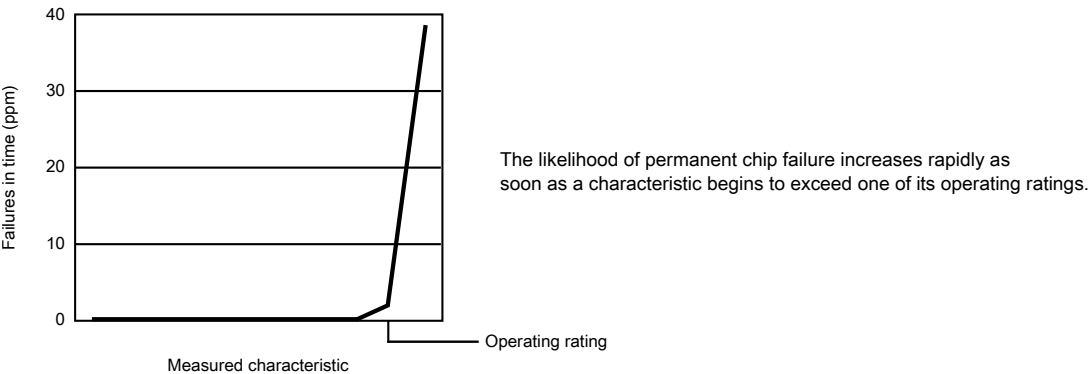
## 8.6 Relationship between ratings and operating requirements

| Operating rating (min.) | Operating requirement (min.) | Operating requirement (max.) | Operating rating (max.) |

| Fatal range | Degraded operating range | Normal operating range | Degraded operating range | Fatal range |
|---|---|---|---|---|
| Expected permanent failure | - No permanent failure<br>- Possible decreased life<br>- Possible incorrect operation | - No permanent failure<br>- Correct operation | - No permanent failure<br>- Possible decreased life<br>- Possible incorrect operation | Expected permanent failure |

−∞                                                                                                  ∞

**Operating (power on)**

| Handling rating (min.) | Handling rating (max.) |

| Fatal range | Handling range | Fatal range |
|---|---|---|
| Expected permanent failure | No permanent failure | Expected permanent failure |

−∞                                                                                                  ∞

**Handling (power off)**

## 8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:
- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.
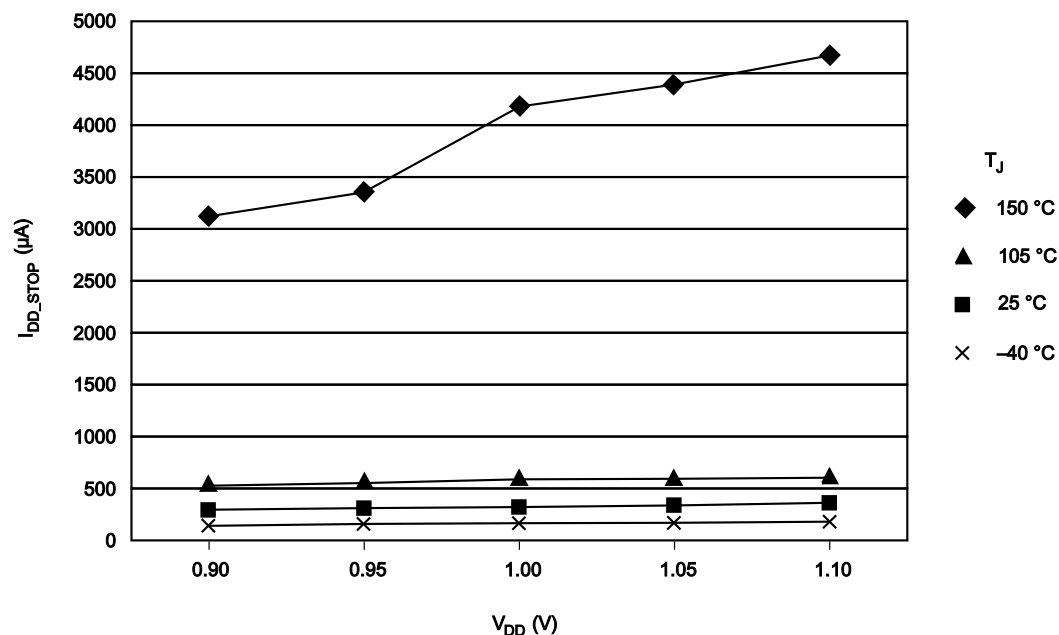
### 8.8.1  Example 1

This is an example of an operating behavior that includes a typical value:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------|-------------|------|------|------|------|
| $I_{WP}$ | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | µA |

### 8.8.2  Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



## 8.9  Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

**How to Reach Us:**

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freescale.com

**Web Support:**
freescale.com/support

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