Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, QSPI, SCI, SPI
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	136
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5606sf2clu6

Table 1. MPC5606S family device comparison (continued)

Feature	MPC5602S	MPC5604S	MPC5606S
Real-Time Counter and Autonomous Periodic Interrupt	Yes	Yes	Yes
Periodic Interrupt Timer (PIT)	4 ch, 32-bit		
Software Watchdog Timer (SWT)	Yes		
System Timer Module (STM)	4 ch, 32-bit		
Timed I/O[2]	8 ch, 16-bit IC/OC		
	16 ch, 16-bit OPWM/IC/OC[3]		
ADC[4]	16 channels, 10-bit		
CAN (64 mailboxes)	1 × FlexCAN	2 × FlexCAN	2 × FlexCAN
CAN sampler	Yes		
SCI	2 × LINFlex		
SPI	2 × DSPI	2 × DSPI	3[5] × DSPI
QuadSPI serial flash interface	No	No	Yes
I^2C	2	2	4
GPIO	105	105	105 (144-pin package) 133 (176-pin package)
Debug	Nexus 1	Nexus 1	Nexus 2+[6]
Package	144 LQFP	144 LQFP	144 LQFP[7] 176 LQFP 208 MAPBGA[8]

1 Configuration is software-programmable.
2 IC-Input Capture, OC-Output Compare, OPWM-Output Pulse Width Modulation.
3 This functionality is split over two eMIOS blocks.
4 Support for external multiplexer enabling up to 23 channels.
5 QuadSPI serial Flash controller can be optionally used as a third DSPI.
6 Nexus2+ available on 176 LQFP as alternate pin function and on 208 MAPBGA.
7 Not all features are available simultaneously in 144 LQFP package option.
8 The 208-pin package is not a production package; it is available in limited quantities for tool development only.

1.4 MPC5606S series blocks

1.4.1 Block diagram

Figure 1 shows a high-level block diagram of the MPC5606S series.

- Two-wire bi-directional serial bus for on-board communications
- Compatibility with I^2C bus standard
- Multimaster operation
- Software-programmable for one of 256 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

1.5.6 Interrupt Controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high-priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software-configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource cannot preempt each other.

Multiple processors can assert interrupt requests to each other through software-settable interrupt requests. These same software-settable interrupt requests also can be used to break the work involved in servicing an interrupt request into a high-priority portion and a low-priority portion. The high-priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software-settable interrupt request to finish the servicing in a lower priority ISR. Therefore these software-settable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS. The INTC provides the following features:

- Unique 9-bit vector for each of the possible 128 separate interrupt sources
- Eight software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority
  - Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources
- External NMI directly accessing the main core critical interrupt mechanism
- 32 external interrupts

1.5.7 QuadSPI serial flash controller

The QuadSPI module enables use of external serial flash memories supporting single, dual, and quad modes of operation. It features the following:

- Memory mapping of external serial flash memory
- Automatic serial flash read command generation by CPU, DMA, or DCU read access on AHB bus
- Supports single, dual, and quad serial flash read commands
- Flexible buffering scheme to maximize read bandwidth of serial flash

- Separate internal power domain applied to full SRAM block, 8 KB SRAM block during Standby modes to retain contents during low-power mode.

1.5.11 On-chip graphics SRAM

The MPC5606S microcontroller has 160 KB on-chip graphics SRAM with the following features:

- Usable as general purpose SRAM
- Typical SRAM access time: 0 wait-state for reads and 32-bit writes
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory

1.5.12 Memory Protection Unit (MPU)

The MPU features the following:

- 12 region descriptors for per-master protection
- Start and end address defined with 32-byte granularity
- Overlapping regions supported
- Protection attributes can optionally include process ID
- Protection offered for three concurrent read ports
- Read and write attributes for all masters
- Execute and supervisor/user mode attributes for processor masters

1.5.13 Boot Assist Module (BAM)

The BAM is a block of read-only memory that is programmed once by Freescale. The BAM program is executed every time the MCU is started up or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (a program is downloaded into RAM via FlexCAN or LINFlex and then executed)
- Booting from external memory

Additionally the BAM:

- Enables and manages the transition of the MCU from reset to user code execution
- Configures device for serial bootload
- Enables multiple bootcode starting locations out of reset through implementation of search for valid Reset Configuration Halfword

1.5.14 Enhanced Modular Input/Output System (eMIOS)

MPC5606S microcontrollers have two eMIOS modules—one with 16 channels and one with eight—with input/output channels supporting a range of 16-bit input capture, output compare, and Pulse Width Modulation functions.

The modules are configurable and can implement 8-channel, 16-bit input capture/output compare or 16-channel, 16-bit output pulse width modulation/input compare/output compare. As many as five additional channels are configurable as modulus counters.

eMIOS other features include:

- Selectable clock source from main FMPLL, auxiliary FMPLL, external 4–16 MHz oscillator or 16 MHz internal RC oscillator
- Timed I/O channels with 16-bit counter resolution
- Buffered updates
- Support for shifted PWM outputs to minimize occurrence of concurrent edges

- MPC5606S includes a 32 KHz low-power external oscillator for slow execution, reduced power consumption, and Real Time Clock
- Dedicated internal 128 kHz RC oscillator for low-power mode operation and self wakeup
  - ±10% accuracy across voltage and temperature (after factory trimming)
  - Trimming registers to support improved accuracy with in-application calibration
- Dedicated 16 MHz internal RC oscillator
  - Used as default clock source out of reset
  - Provides a clock for rapid startup from low-power modes
  - Provides a backup clock in the event of PLL or external oscillator clock failure
  - Offers an independent clock source for the watchdog timer
  - ±5% accuracy across voltage and temperature (after factory trimming)
  - Trimming registers to support frequency adjustment with in-application calibration

1.5.20 Periodic Interrupt Timer module (PIT)

The PIT features the following:

- Four general-purpose interrupt timers
- As many as two dedicated interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by system clock frequency
- 32-bit counter for Real Time Interrupt, clocked from main external oscillator

1.5.21 Real Time Counter (RTC)

The RTC supports wakeup from low-power modes or Real Time Clock generation

- Configurable resolution for different timeout periods
  - 1 s resolution for >1 hour period
  - 1 ms resolution for 2 second period
- Selectable clock sources from external 32 KHz crystal, external 4–16 MHz crystal, internal 128 kHz RC oscillator, or divided internal 16 MHz RC oscillator

1.5.22 System Timer Module (STM)

The STM is a 32-bit timer designed to support commonly required system and application software timing functions. The STM includes a 32-bit up counter and four 32-bit compare channels with a separate interrupt source for each channel. The counter is driven by the system clock divided by an 8-bit prescale value (1 to 256).

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.5.23 Software Watchdog Timer (SWT)

The Watchdog features the following:

- Watchdog can be activated by software or enabled out of reset
- Supports normal or windowed mode
- Watchdog timer value writable once after reset

  - Static debug
  - Watchpoint messaging
  - Ownership trace messaging
  - Program trace messaging
  - Real time read/write of any internally memory-mapped resources through JTAG pins
  - Overrun control, which selects whether to stall before Nexus overruns or else keep executing and allow overwrite of information
  - Watchpoint triggering, watchpoint triggers program tracing
- Configured via the IEEE 1149.1 (JTAG) port
- Nexus Auxiliary port supported on the 176 LQFP and 208-pin BGA package FOR DEVELOPMENT ONLY
  - Narrow Auxiliary Nexus port supporting support trace, with two MDO pins
  - Wide Auxiliary Nexus port supporting higher bandwidth trace, with four MDO pins

2 Pinout and signal descriptions

2.1 144 LQFP package pinouts

This section shows the pinouts for the 144-pin LQFP packages.

CAUTION

Any pins labeled “NC” must not be connected to any external circuit.

Table 8. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number		
									144 LQFP	176 LQFP	208 MAPBGA
PC[10]	PCR[40]	Option 0 Option 1 Option 2 Option 3	GPIO[40] — SOUND —	ANS[10]	SIUL — SGL —	I/O	J	None, None	60	76	T9
PC[11]	PCR[41]	Option 0 Option 1 Option 2 Option 3	GPIO[41] — MA0 PCS2_1	ANS[11]	SIUL — ADC DSPI_1	I/O	J	None, None	59	75	R9
PC[12]	PCR[42]	Option 0 Option 1 Option 2 Option 3	GPIO[42] — MA1 PCS1_1	ANS[12]	SIUL — ADC DSPI_1	I/O	J	None, None	58	74	P9
PC[13]	PCR[43]	Option 0 Option 1 Option 2 Option 3	GPIO[43] — MA2 PCS0_1	ANS[13]	SIUL — ADC DSPI_1	I/O	J	None, None	57	73	N9
PC[14]	PCR[44]	Option 0 Option 1 Option 2 Option 3	GPIO[44] — — —	ANS[14] EXTAL32	SIUL — — —	I/O	J	None, None	56	72	T8
PC[15]	PCR[45]	Option 0 Option 1 Option 2 Option 3	GPIO[45] — — —	ANS[15] XTAL32	SIUL — — —	I/O	J	None, None	55	71	R8
PD[0]	PCR[46]	Option 0 Option 1 Option 2 Option 3	GPIO[46] M0C0M SSD0_0 eMIOSB[23]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	73	89	R16
PD[1]	PCR[47]	Option 0 Option 1 Option 2 Option 3	GPIO[47] M0C0P SSD0_1 eMIOSB[22]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	74	90	P16

Table 8. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number		
									144 LQFP	176 LQFP	208 MAPBGA
PD[2]	PCR[48]	Option 0 Option 1 Option 2 Option 3	GPIO[48] M0C1M SSD0_2 eMIOSB[21]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	75	91	P15
PD[3]	PCR[49]	Option 0 Option 1 Option 2 Option 3	GPIO[49] M0C1P SSD0_3 eMIOSB[20]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	76	92	N16
PD[4]	PCR[50]	Option 0 Option 1 Option 2 Option 3	GPIO[50] M1C0M SSD1_0 eMIOSB[19]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	79	95	N15
PD[5]	PCR[51]	Option 0 Option 1 Option 2 Option 3	GPIO[51] M1C0P SSD1_1 eMIOSB[18]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	80	96	M15
PD[6]	PCR[52]	Option 0 Option 1 Option 2 Option 3	GPIO[52] M1C1M SSD1_2 eMIOSB[17]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	81	97	M16
PD[7]	PCR[53]	Option 0 Option 1 Option 2 Option 3	GPIO[53] M1C1P SSD1_3 eMIOSB[16]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	82	98	K16
PD[8]	PCR[54]	Option 0 Option 1 Option 2 Option 3	GPIO[54] M2C0M SSD2_0 —	—	SIUL SMC SSD —	I/O	SMD	None, None	83	99	J16
PD[9]	PCR[55]	Option 0 Option 1 Option 2 Option 3	GPIO[55] M2C0P SSD2_1 —	—	SIUL SMC SSD —	I/O	SMD	None, None	84	100	K15

Table 8. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number		
									144 LQFP	176 LQFP	208 MAPBGA
PG[8]	PCR[94]	Option 0 Option 1 Option 2 Option 3	GPIO[94] DCU_VSYNC — —	BP0	SIUL DCU — —	I/O	M2	Input, None	17	17	J3
PG[9]	PCR[95]	Option 0 Option 1 Option 2 Option 3	GPIO[95] DCU_HSYNC — —	BP1	SIUL DCU — —	I/O	M1	Input, None	18	18	K3
PG[10]	PCR[96]	Option 0 Option 1 Option 2 Option 3	GPIO[96] DCU_DE — —	BP2	SIUL DCU — —	I/O	M2	None, None	19	19	J4
PG[11]	PCR[97]	Option 0 Option 1 Option 2 Option 3	GPIO[97] DCU_PCLK — —	BP3	SIUL DCU — —	I/O	M1	None, None	20	20	K4
PG[12]	PCR[98]	Option 0 Option 1 Option 2 Option 3	GPIO[98] eMIOSA[23] SOUND eMIOSA[8]	FP30	SIUL PWM/Timer SGL PWM/Timer	I/O	S	None, None	126	156	D10
PG[13]	—	—	Reserved	—	—	—	—	—	—	—	—
PG[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PG[15]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[0][7]	PCR[99]	Option 0 Option 1 Option 2 Option 3	GPIO[99] TCK — —	—	SIUL JTAG — —	I/O	S	Input, Pullup	36	43	R1
PH[1][7]	PCR[100]	Option 0 Option 1 Option 2 Option 3	GPIO[100] TDI — —	—	SIUL JTAG — —	I/O	S	Input, Pullup	33	36	P2

Table 8. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number		
									144 LQFP	176 LQFP	208 MAPBGA
PJ[1]	PCR[106]	Option 0 Option 1 Option 2 Option 3	GPIO[106] PDI_HSYNC — —	—	SIUL PDI — —	I/O	S	None, None	—	120	A3
PJ[2]	PCR[107]	Option 0 Option 1 Option 2 Option 3	GPIO[107] PDI_VSYNC — —	—	SIUL PDI — —	I/O	S	None, None	—	121	B3
PJ[3]	PCR[108]	Option 0 Option 1 Option 2 Option 3	GPIO[108] PDI_PCLK — —	—	SIUL PDI — —	I/O	M1	None, None	—	122	A4
PJ[4]	PCR[109]	Option 0 Option 1 Option 2 Option 3	GPIO[109] PDI[0] CANRX_0 —	—	SIUL PDI FlexCAN_0 —	I/O	S	None, None	—	57	B4
PJ[5]	PCR[110]	Option 0 Option 1 Option 2 Option 3	GPIO[110] PDI[1] CANTX_0 —	—	SIUL PDI FlexCAN_0 —	I/O	M1	None, None	—	58	A5
PJ[6]	PCR[111]	Option 0 Option 1 Option 2 Option 3	GPIO[111] PDI[2] CANRX_1 eMIOSA[22]	—	SIUL PDI FlexCAN_1 PWM/Timer	I/O	S	None, None	—	59	B5
PJ[7]	PCR[112]	Option 0 Option 1 Option 2 Option 3	GPIO[112] PDI[3] CANTX_1 eMIOSA[21]	—	SIUL PDI FlexCAN_1 PWM/Timer	I/O	M1	None, None	—	60	A6
PJ[8]	PCR[113]	Option 0 Option 1 Option 2 Option 3	GPIO[113] PDI[4] — —	—	SIUL PDI — —	I/O	S	None, None	—	125	B6

Table 15. Recommended operating conditions (3.3 V) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{LCD}	SR	C	Voltage on VLCD (LCD supply) pin with respect to V_{SS}	—	0	V_{DDE_A} + 0.3	V
TV_{DD}	SR	C	V_{DD} slope to ensure correct power up	—	5×10^{-6}	0.25	V/µs
T_A	SR	C	Ambient temperature under bias	—	–40	105	°C
T_J	SR	C	Junction temperature under bias		–40	150	

1 100 nF capacitance needs to be provided between V_{DDA}/V_{SSA} pair.

2 At least 10 µF capacitance must be connected between V_{DDR} and V_{SSR}. This is required because of sharp surge due to external ballast.

3 V_{DD} refers collectively to I/O voltage supplies, i.e., V_{DDE_A}, V_{DDE_B}, V_{DDE_C}, V_{DDE_E}, V_{DDMA}, V_{DDMB} and V_{DDMC}.

4 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair

5 Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/O's DC electrical specification may not be guaranteed.
When voltage drops below V_{LVDHVL} device is reset.

6 V_{SS} refers collectively to I/O voltage supply grounds, i.e., V_{SSE_A}, V_{SSE_B}, V_{SSE_C}, V_{SSE_E}, V_{SSMA}, V_{SSMB} and V_{SSMC}) unless otherwise noted.

Table 16. Recommended operating conditions (5.0 V)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{DDA}[1]	SR	C	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SS})	—	4.5	5.5	V
		C		Voltage drop[2]	3.0	5.5	
		C		Relative to V_{DDE_C}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SSA}	SR	C	Voltage on VSSA (ADC reference) pin with respect V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{SSPLL}	SR	C	Voltage on VSSPLL pin with respect to V_{SS12}	—	0	0	V
V_{DDR}[3]	SR	C	Voltage on VDDR pin (regulator supply) with respect to ground (V_{SSR})	—	4.5	5.5	V
		C		Voltage drop[2]	3.0	5.5	
		C		Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SSR}	SR	C	Voltage on VSSR (regulator ground) pin with respect to V_{SS12}	—	0	0	V
V_{SS12}	CC	C	Voltage on VSS12 pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD}[4,5]	SR	C	Voltage on VDD pins (VDDE_A, VDDE_B, VDDE_C, VDDE_E, VDDMA, VDDMB, VDDMC) with respect to ground (V_{SS})	Voltage drop[2]	4.5	5.5	V
V_{SS}[6]	SR	C	I/O supply ground	—	0	0	V
V_{DDE_A}	SR	C	Voltage on VDDE_A (I/O supply) pin with respect to ground (V_{SSE_A})	—	4.5	5.5	V

- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ±10% range
- LVDLVCOR monitors power domain No. 1
- LVDLVBKP monitors power domain No. 0

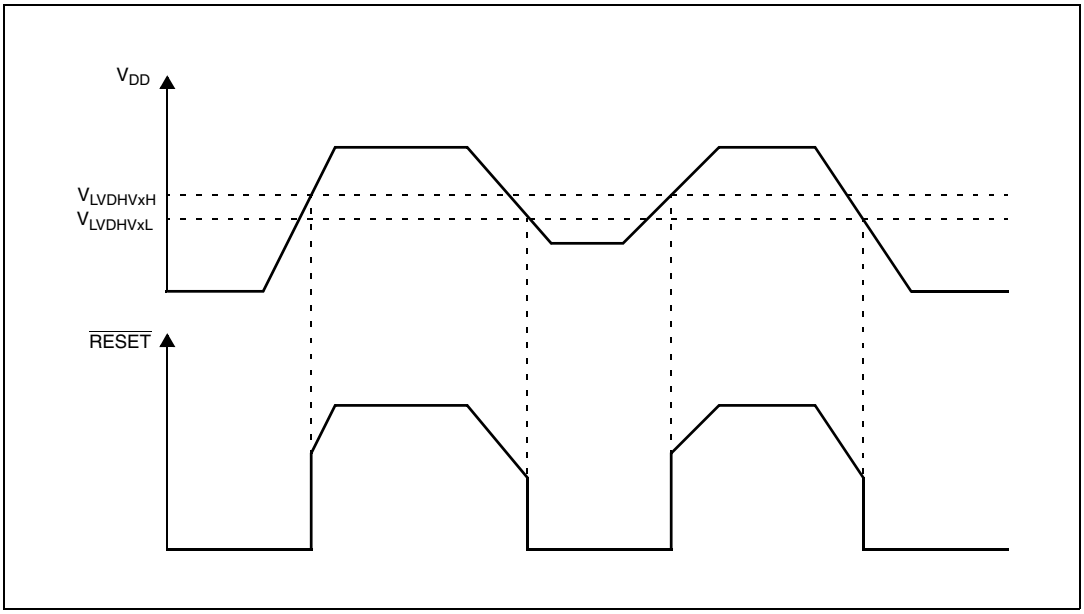


Figure 9. Low voltage monitor vs. reset

Table 26. Low voltage monitor electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{PORH}	CC	P	Power-on reset threshold	—	1.5	—	2.6	V
$V_{LVDHV3H}$	CC	P	LVDHV3 low voltage detector high threshold	—	—	—	2.9	V
$V_{LVDHV5H}$	CC	P	LVDHV5 low voltage detector high threshold	—	—	—	4.4	V
$V_{LVDHV3L}$	CC	P	LVDHV3 low voltage detector low threshold	—	2.6	—	—	V
$V_{LVDHV5L}$	CC	P	LVDHV5 low voltage detector low threshold	—	3.8	—	—	V
$V_{LVDLVCORH}$[2]	CC	P	LVDLVCOR low voltage detector high threshold	T_A = 25 °C, after trimming	—	—	1.15	V
$V_{LVDLVCORL}$	CC	P	LVDLVCOR low voltage detector low threshold		1.08	—	—	V

[1] V_{DD} = 3.3 V ±10% / 5.0 V ±10%, T_A = –40 to 105 °C, unless otherwise specified.

[2] $L_{VDLVBKP}$ has same post-trim thresholds as $_{LVDLVCOR}$.

3.7.3 Low voltage domain power consumption

Table 27 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

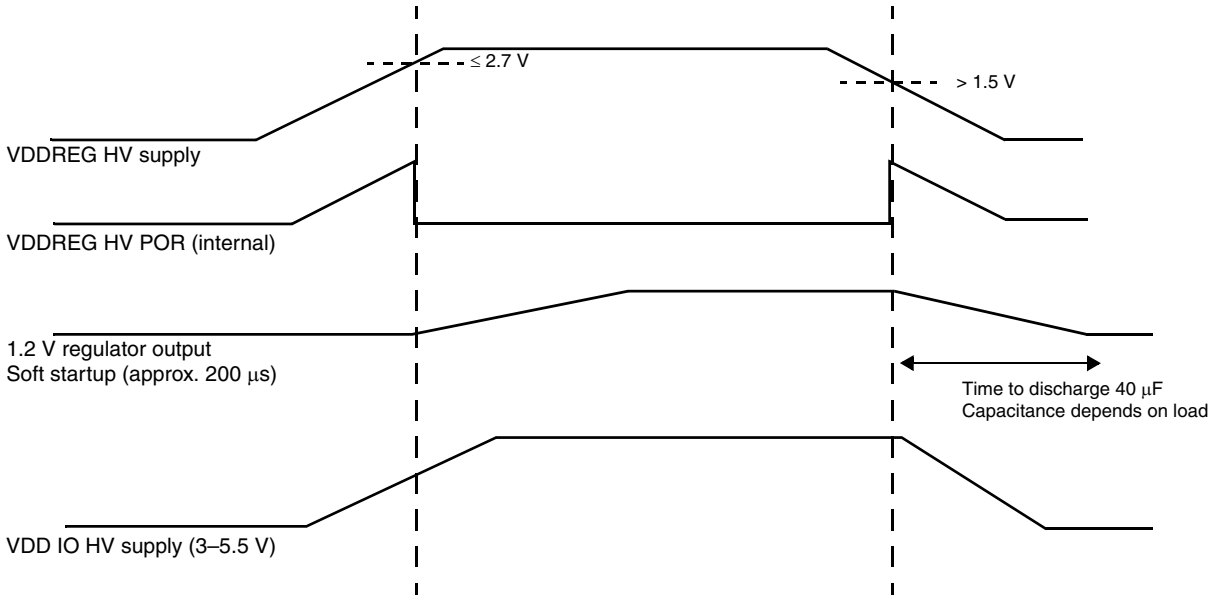


Figure 11. Recommended order for powering down the power supplies

CAUTION

The VDD IO HV supply must be disabled after the VDDREG HV supply voltage drops below 1.5 V. This is to ensure that the 1.2 V regulator shuts down before the 3.3 V regulator shuts down.

3.7.5 Power-up inrush current profile

Figure 12 shows the power up inrush current profile of the ballast transistor under the worst possible startup condition (fastest PVT and fastest power ramp time).

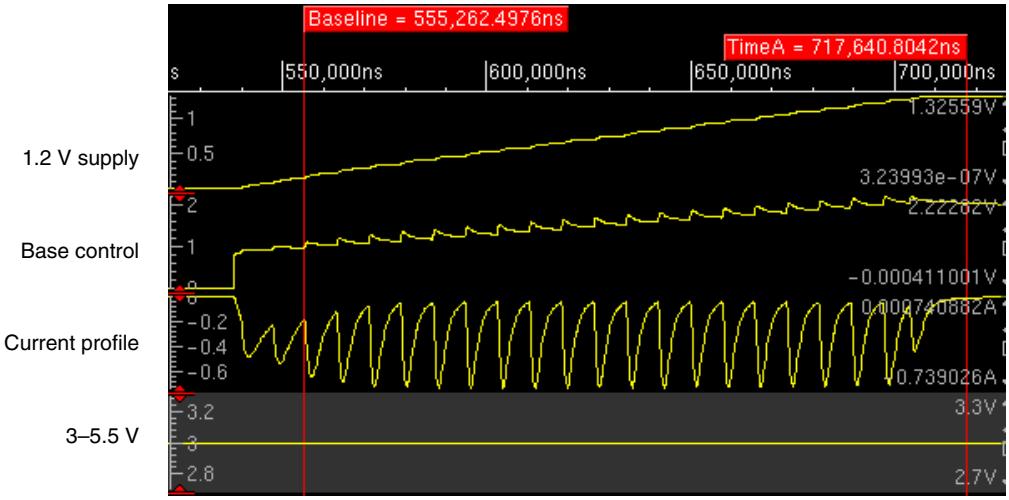


Figure 12. Power-up inrush current profile

Table 34. FAST configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
T_{tr}	CC	T	Output transition time output pin[3] FAST configuration	C_L = 25 pF, V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	4	ns
		T		C_L = 50 pF, V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	6	
		T		C_L = 100 pF, V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	12	
		T		C_L = 25 pF, V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	4	
		T		C_L = 50 pF, V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	7	
		T		C_L = 100 pF, V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	12	
ΔI_{tr50}	CC	D	Current slew at C_L = 50 pF FAST configuration	V_{DD} = 5.0 V ±10%, PAD3V5V = 0 (recommended configuration)	—	—	55	mA/ns
		D		V_{DD} = 3.3 V ±10%, PAD3V5V = 1 (recommended configuration)	—	—	40	
		D		V_{DD} = 5.0 V ±10%, PAD3V5V = 1	—	—	100	

1 V_{DD} = 3.3 V ±10% / 5.0 V ±10%, T_A = –40 to 105 °C, unless otherwise specified

2 This is a transient configuration during power-up. All pads but $\overline{\text{RESET}}$ and NEXUS output (MDOx, EVTO, MCK) are configured in input or in high impedance state.

3 C_L includes device and package capacitance (C_{PKG} < 5 pF).

Table 35. SMD pad electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IL}	CC	P	Low level input voltage	—	–0.4	—	0.35×V_{DDM}	V
V_{IH}	CC	P	High level input voltage	—	0.65×V_{DDM}	—	V_{DDM}+0.4	
V_{HYST}	CC	C	Schmitt trigger hysteresis	—	0.1×V_{DDM}	—	—	
V_{OL}	CC	P	Low level output voltage	I_{OL} = 20 mA[1]	—	—	0.32	
				I_{OL} = 30 mA[2]	—	—	0.48	
V_{OH}	CC	P	High level output voltage	I_{OH} = –20 mA[1]	V_{DDM}–0.32	—	—	
				I_{OH} = –30 mA[2]	V_{DDM}–0.48	—	—	

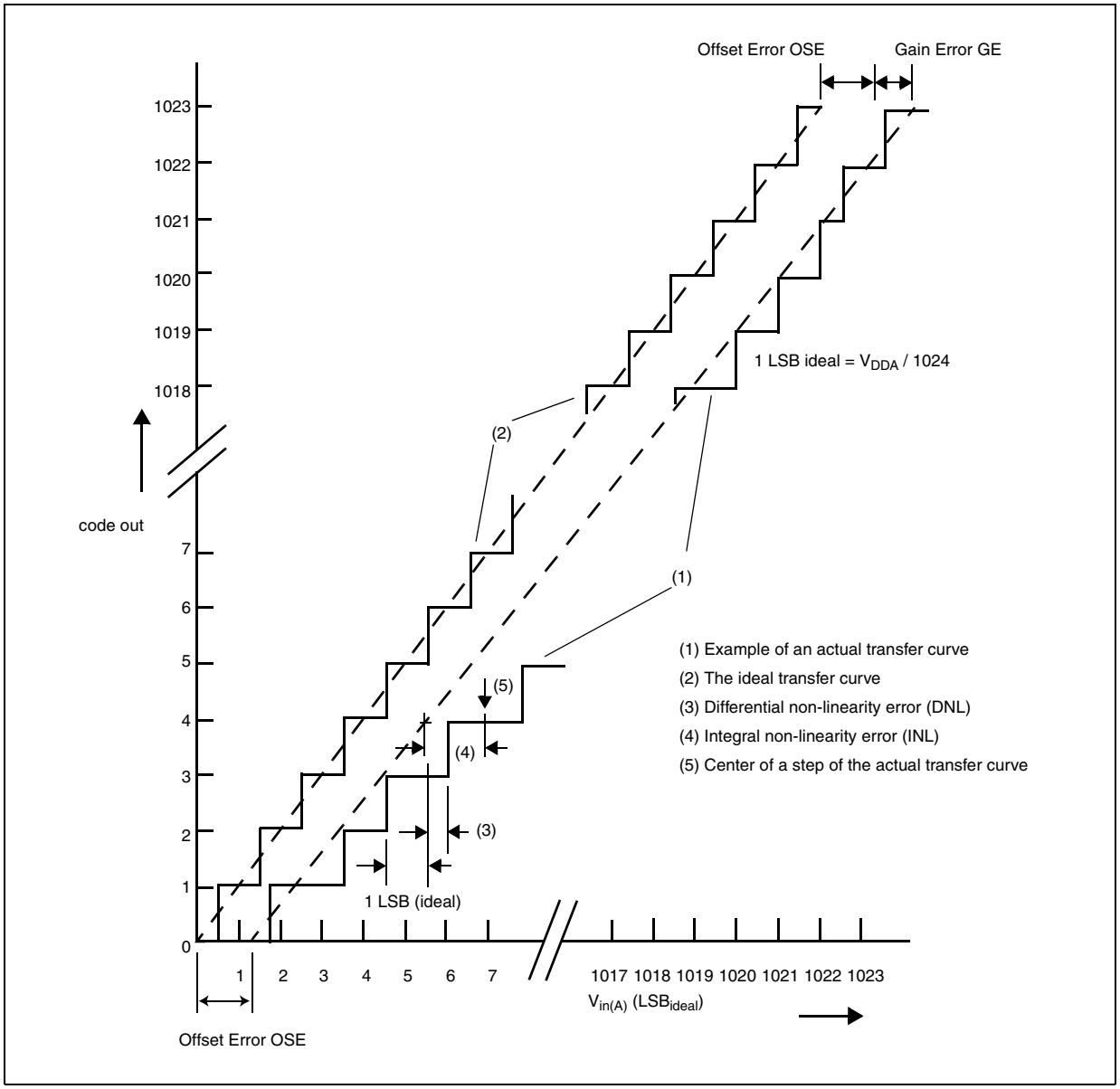


Figure 21. ADC Characteristics and Error Definitions

3.17.1 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

1 V_{DDA} = 3.3 V ±10% / 5.0 V ±10%, T_A = –40 to 105 °C, unless otherwise specified.

2 Analog and digital V_{SS} **must** be common (to be tied together externally).

3 V_{AINx} may exceed V_{SSA} and V_{DDA} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.

4 At 32 MHz the minimum sampling time must be at least 180 ns.

5 During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.

6 The maximum sample rate is 1 million samples per second, provided the source impedance and current limiter(> 1 kΩ) are calculated adequately.
— Filter capacitor at analog source output must meet the criteria Cf (filter capacitor) > 2048 × Cs (sampling capacitor is 3 pF).

7 This parameter does not include the sample time t_{ADC_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.

3.18 LCD driver electrical characteristics

Table 51. LCD driver specifications

Symbol		C	Parameter	Value[1]			Unit
				Min	Typ	Max	
VLCD	SR	C	Voltage on VLCD (LCD supply) pin with respect to VSS	0	—	VDDE + 0.3	V
$Z_{BP/FP}$	CC	T	LCD output impedance (BP[n-1:0],FP[m-1:0]) for output levels VLCD, VSS[2]	—	—	5.0	kΩ
$I_{BP/FP}$	CC	T	LCD output current (BP[n-1:0],FP[m-1:0]) for outputs charge/discharge voltage levels VLCD2/3, VLCD1/2, VLCD1/3)[2,3]	—	25	—	μA

1 V_{DD} = 5.0 V ± 10%, T_A = –40–105 °C, unless otherwise specified

2 Outputs measured one at a time, low impedance voltage source connected to the VLCD pin.

3 With PWR=10, BSTEN=0, and BSTAO=0

3.19 Pad AC specifications

Table 52. Pad AC specifications (5.0 V, PAD3V5V = 0)[1]

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	1.5	—	30	6	—	50	—	—	4	0.04	—	2	25
		1.5	—	30	9	—	100	—	—	2	0.04	—	2	50
		1.5	—	30	12	—	125	—	—	2	0.04	—	2	100
		1.5	—	30	16	—	150	—	—	2	0.04	—	2	200

Table 53. Pad AC specifications (3.3 V, PAD3V5V = 1)[1] (continued)

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
3	Fast	1	—	6	1	—	4	—	—	72	3	—	40	25
		1	—	6	1.5	—	7	—	—	55	3	—	40	50
		1	—	6	3	—	12	—	—	40	3	—	40	100
		1	—	6	5	—	18	—	—	25	3	—	40	200
4	Pull Up/Down (3.6 V max)	—	—	—	—	—	7500	—	—	—	—	—	—	50
Parameter Classification		D			C			C			C			n/a

[1] Propagation delay from $V_{DD}/2$ of internal signal to Pchannel/Nchannel on condition

[2] Slope at rising/falling edge

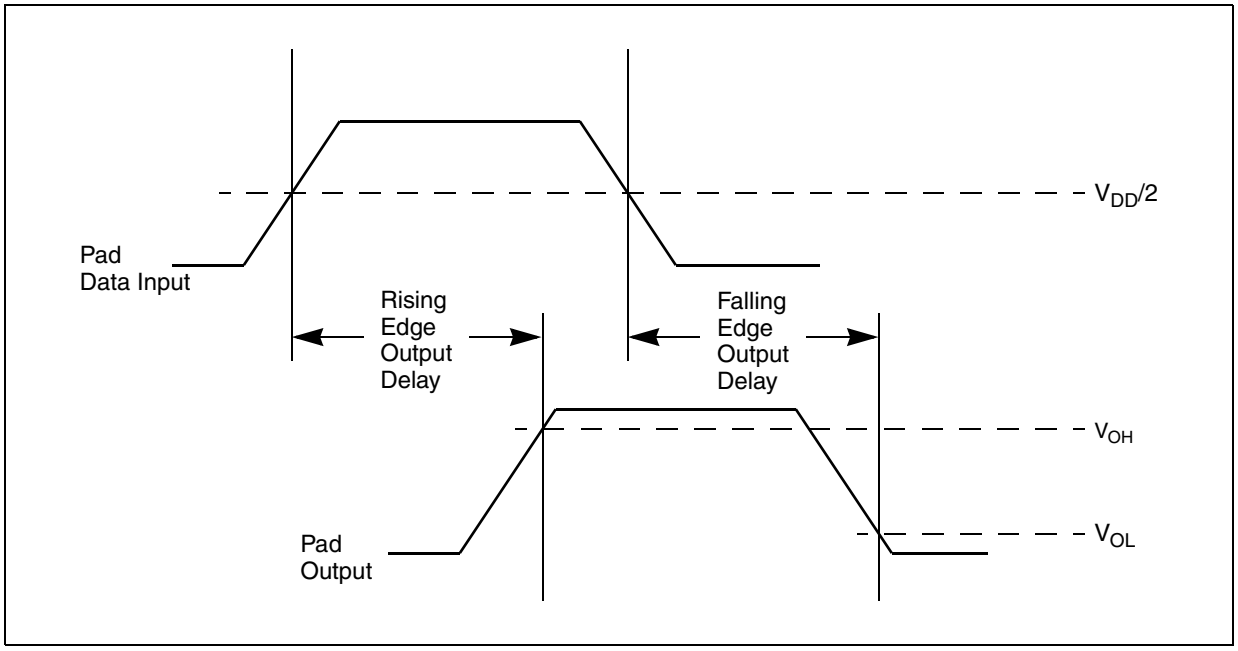


Figure 26. Pad output delay

The clock profile in Figure 49 is measured at 30% to 70% levels of VDDE.

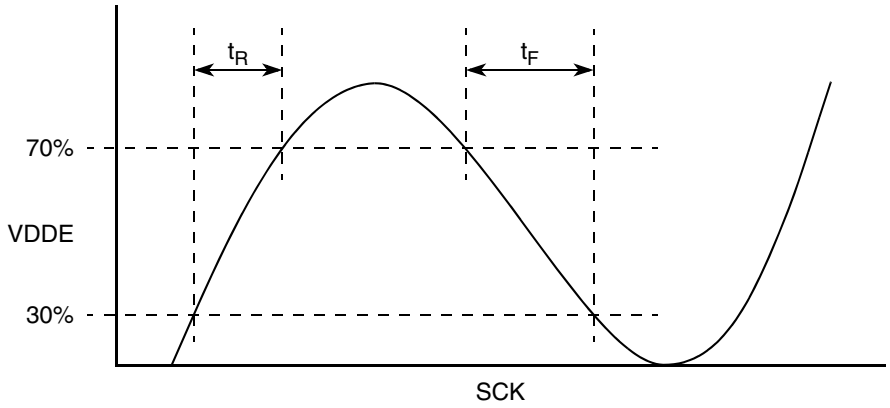
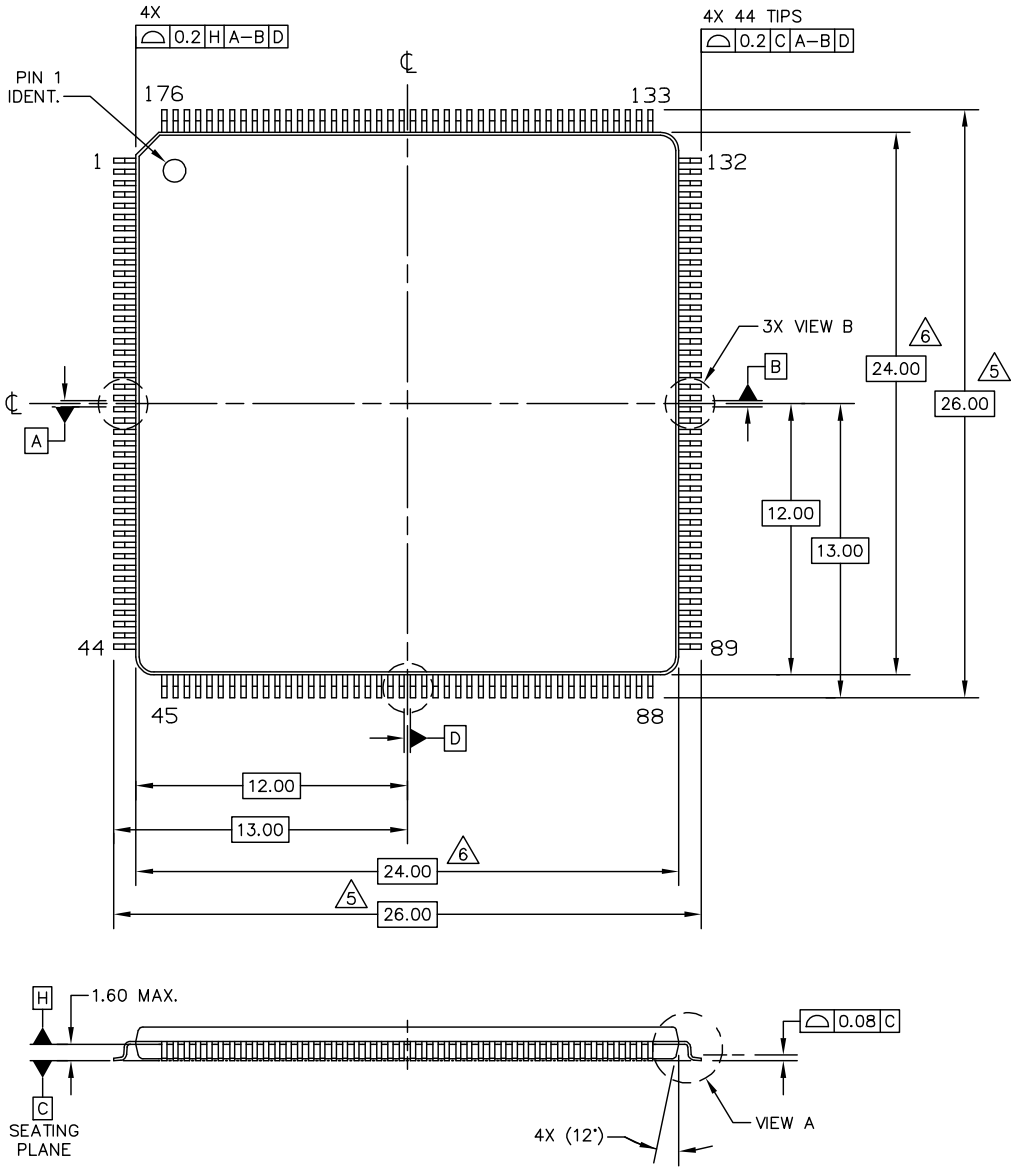


Figure 49. QuadSPI clock profile

4.2 176 LQFP



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 176 LD TQFP, 24 X 24 PKG, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23479W	REV: B
	CASE NUMBER: 1101–01	02 JUN 2005
	STANDARD: JEDEC MS–026 BGA	

Figure 53. LQFP176 mechanical drawing (Part 1 of 3)

Table 66. Document revision history

Revision	Date	Substantive changes
5	1 Sep 2010	Editorial changes and improvements. Replaced “validation” with “characterization” throughout. Added an entry for Rev. 3 to this table. In the block diagram, in the SXOSC block, changed “32 kHz” to “32 KHz”. Revised the feature section and added the “Feature details” subsection. Renamed the analog pins (were AN..., are ANS...) throughout. Changed several pin names that contained _A, _B, _C, ... to contain _0, _1, _2, ... throughout. Changed the PCS and oscillator pin names throughout. Revised the feature section and added the “Feature details” subsection. Deleted the out-of-date “Block summary” section. In the 144-pin pinout: • For pin 122, changed PCS_B1 to PCS1_1. • For pin 123, changed PCS_B0 to PCS0_1. In the “144 LQFP package pinout” section, added pinouts for the chips with 512 KB and 256 KB flash memory. In the 176-pin pinout: • For pin 152, changed PCS_B1 to PCS1_1. • For pin 153, changed PCS_B0 to PCS0_1. Revised the “Pad configuration during reset phases”, “Voltage supply pins”, “Pad types”, “System pins”, and “Nexus pins” sections. Changed several module names and abbreviations to be consistent with the official module names and abbreviations. In the “Voltage supply pin descriptions” table, revised the entry for V_{DD12}. In the “Debug pin descriptions” table, changed pad type M to pad type M1. In the “Pad types” section, changed “registers in the device reference manual” to “registers in the SIUL chapter of the device reference manual”. Changed the name of the port-pin summary section (was “Functional ports A, B, C, D, E, F, G, H, I, J, K”, is “Port pin summary”). In the “Signal details” section: • Renamed the analog pins (were AN..., are ANS...). • Added “ANS[0:15] connect to ATD channels [32:47]” to the ANS signal description. • Added “The available 8 multiplexed channels connect to ATD channels [64:71]” to the MA signal description. • Deleted “when high; otherwise low to allow a subframe display for pixels” from the DCU_DE description. • Changed the description for DCU_TAG, PDI_PCLK, TXD_A, and SSD signals. • Added QuadSPI signals. • Deleted “For valid Pixel Data this is high, otherwise low” from the PDI_DE description. • Changed several pin names that contained _A, _B, _C, ... to contain _0, _1, _2, ... In the “Port pin summary” table: • Changed the pad type for PC[0]—PC[9] (was S, is J). • Moved the AN[0]—AN[15] entries from the “Function” column to the “Special function” column. • Moved the OSC32K_EXTAL and OSC32K_XTAL entries from the “Function” column to the “Special function” column. • Added alternate function names and clarifying footnotes to the PF[11]—PF[14] entries. • Added new information on pad types (including splitting up the existing M pads into two categories, M1 and M2). • Added a footnote to the “Special function” column title.

Table 66. Document revision history

Revision	Date	Substantive changes
6	14 Jan 2011	Editorial changes and improvements. Swapped XTAL and EXTAL pins for the 208-pin BGA package and throughout. In the “Pinout and signal descriptions” section, changed WARNING labels to CAUTION labels. Updated the “Absolute maximum ratings” and “Recommended operating conditions” tables. Added footnote reference to V_{ss12} in “Recommended operating conditions (3.3 V)” table. Updated the “Connecting power supply pins” section. Removed footnote regarding characterization in the “Thermal characteristics” table. Updated the V_{DD12}/V_{DDPLL} operating voltages in the “Electromagnetic interference” table. Added typical values and updated the “Voltage regulator electrical characteristics,” “Low-power voltage regulator electrical characteristics,” and “Ultra-low-power voltage regulator electrical characteristics” tables. Updated classifications and values in the “Low voltage monitor electrical characteristics” table. Made major modifications and updates to the “DC electrical characteristics” table. Made major modifications and updates to the “I/O input DC electrical characteristics” table. Made major modifications and updates to the “I/O pull-up/pull-down DC electrical characteristics” table. Changed “SMC” pads to “SMD” pads throughout. Made updates to the “SMD pad electrical characteristics” table. Added run current during RESET to the “Reset electrical characteristics” table. Updated the FMPLL jitter (peak to peak) specification in the “FMPLL electrical characteristics” table. Updated f_{FIRC} and t_{FIRCSU} in the “Fast internal RC oscillator (16 MHz) electrical characteristics” table. Updated f_{SIRC} and t_{SIRCSU} in the “Slow internal RC oscillator (128 kHz) electrical characteristics” table. Removed “symmetric” pad type from the “Pad AC specifications (5.0 V, PAD3V5V = 0)” table. Removed “symmetric” pad type from the “Pad AC specifications (3.3 V, PAD3V5V = 1)” table. Updated V_{DD12} post-trimming minimum value in the “Low-power voltage regulator electrical characteristics” table. Updated V_{DD12} post-trimming minimum value in the “Ultra-low-power voltage regulator electrical characteristics” table. Updated $V_{LVDLVCORH}$ maximum value in the “Low voltage monitor electrical characteristics” table. Updated $V_{LVDLVCORL}$ minimum value in the “Low voltage monitor electrical characteristics” table. Updated value of V_{DD12}/V_{DDPLL} operating voltages in the “Input DC electrical characteristics” table. Corrected erroneous value of I_{LKG} (105°C case) in the “Input DC electrical characteristics” table.