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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, QSPI, SCI, SPI
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	108
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5606sf2vlq6

1 Overview

1.1 Document overview

This document describes the device features and highlights important electrical and physical characteristics. For functional characteristics, see the *MPC5606S Microcontroller Reference Manual*.

1.2 Description

The MPC5606S family of chips is designed to enable the development of automotive instrument cluster applications by providing a single-chip solution capable of hosting real-time applications and driving a TFT display directly using an on-chip color TFT display controller.

MPC5606S chips incorporate a cost-efficient host processor core compliant with the Power Architecture® embedded category. The processor is 100% user-mode compatible with the Power Architecture and capitalizes on the available development infrastructure of current Power Architecture devices with full support from available software drivers, operating systems and configuration code to assist with users' implementations.

Offering high performance processing at speeds up to 64 MHz, the MPC5606S family is optimized for low power consumption and supports a range of on-chip SRAM and internal flash memory sizes. The version with 1 MB of flash memory (MPC5606S) features 160 KB of on-chip graphics SRAM.

See Table 1 for specific memory and feature sets of the product family members.

1.3 Device comparison

Table 1. MPC5606S family device comparison

Feature	MPC5602S	MPC5604S	MPC5606S
CPU	e200z0h		
Execution speed	Static – 64 MHz		
Flash memory (ECC)	256 KB	512 KB	1 MB
EEPROM Emulation Block (ECC)	4 × 16 KB		
RAM (ECC)	24 KB	48 KB	48 KB
Graphics RAM	No	No	160 KB
MPU	12 entry		
eDMA	16 channels		
Display Control Unit (DCU)	No	No	Yes
Parallel Data Interface	No	No	Yes
Stepper Motor Controller (SMC)	6 motors		
Stepper Stall Detect (SSD)	Yes		
Sound Generation Logic (SGL)	Yes		
LCD driver	40 × 4, 38 × 6[1]		
32 KHz slow external crystal oscillator	Yes		

[5] A high level summary of some key durations that need to be considered when recovering from low-power modes. This does not account for all durations at wakeup. Other delays will be necessary to consider, including but not limited to the external supply startup time.
IRC wakeup time must not be added to the overall wakeup time as it starts in parallel with the VREG.
All other wakeup times must be added to determine the total startup time.

[6] This is the startup of the regulator that happens after the 5 V has reached beyond its POR range. If the external supply ramp rate is slow, measure from when VREG has crossed beyond the POR threshold; otherwise, this value will depend on the ramp rate of the external supply (VDDR).

Additional notes on low-power operation:

- Fast wakeup using the on-chip 16 MHz internal RC oscillator allows rapid execution from RAM on exit from low-power modes
- The 16 MHz internal RC oscillator supports low-speed code execution and clocking of peripherals when it is selected as the system clock and can also be used as the PLL input clock source to provide fast startup, without external oscillator delay
- MPC5606S devices include an internal voltage regulator that includes the following features:
  - Regulates input to generate all internal supplies
  - Manages power gating
  - Low-power regulators support operation when in Stop and Standby modes to minimize power consumption
  - Startup on-chip regulators in <50 µs for rapid exit of Stop and Standby modes
  - Low-voltage detection on main supply and 1.2 V regulated supplies

1.5.2 e200z0h core processor

The e200z0h processor is similar to other processors in the e200zx series, but supports only the VLE instruction set and does not include the signal processing extension for DSP applications or a floating point unit.

The e200z0h has all the features of the e200z0 plus:

- Branch acceleration using Branch Target Buffer (BTB)
- Supports independent instruction and data accesses to different memory subsystems, such as SRAM and flash memory via independent Instruction and Data BIUs

The e200z0h processor uses a four stage in-order pipeline for instruction execution.

1. The Instruction Fetch (stage 1)
2. Instruction Decode/Register file Read/Effective Address Calculation (stage 2)
3. Execute/Memory Access (stage 3)
4. Register Writeback (stage 4)

These stages operate in an overlapped fashion, allowing single clock instruction execution for most instructions.

The integer execution unit consists of:

- 32-bit Arithmetic Unit (AU)
- Logic Unit (LU)
- 32-bit Barrel shifter (Shifter)
- Mask-Insertion Unit (MIU)
- Condition Register manipulation Unit (CRU)
- Count-Leading-Zeros unit (CLZ)
- 8 × 32 hardware multiplier array
- Result feed-forward hardware
- Hardware divider

- Separate internal power domain applied to full SRAM block, 8 KB SRAM block during Standby modes to retain contents during low-power mode.

1.5.11 On-chip graphics SRAM

The MPC5606S microcontroller has 160 KB on-chip graphics SRAM with the following features:

- Usable as general purpose SRAM
- Typical SRAM access time: 0 wait-state for reads and 32-bit writes
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory

1.5.12 Memory Protection Unit (MPU)

The MPU features the following:

- 12 region descriptors for per-master protection
- Start and end address defined with 32-byte granularity
- Overlapping regions supported
- Protection attributes can optionally include process ID
- Protection offered for three concurrent read ports
- Read and write attributes for all masters
- Execute and supervisor/user mode attributes for processor masters

1.5.13 Boot Assist Module (BAM)

The BAM is a block of read-only memory that is programmed once by Freescale. The BAM program is executed every time the MCU is started up or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (a program is downloaded into RAM via FlexCAN or LINFlex and then executed)
- Booting from external memory

Additionally the BAM:

- Enables and manages the transition of the MCU from reset to user code execution
- Configures device for serial bootload
- Enables multiple bootcode starting locations out of reset through implementation of search for valid Reset Configuration Halfword

1.5.14 Enhanced Modular Input/Output System (eMIOS)

MPC5606S microcontrollers have two eMIOS modules—one with 16 channels and one with eight—with input/output channels supporting a range of 16-bit input capture, output compare, and Pulse Width Modulation functions.

The modules are configurable and can implement 8-channel, 16-bit input capture/output compare or 16-channel, 16-bit output pulse width modulation/input compare/output compare. As many as five additional channels are configurable as modulus counters.

eMIOS other features include:

- Selectable clock source from main FMPLL, auxiliary FMPLL, external 4–16 MHz oscillator or 16 MHz internal RC oscillator
- Timed I/O channels with 16-bit counter resolution
- Buffered updates
- Support for shifted PWM outputs to minimize occurrence of concurrent edges

Table 8. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number		
									144 LQFP	176 LQFP	208 MAPBGA
PB[0]	PCR[16]	Option 0 Option 1 Option 2 Option 3	GPIO[16] CANTX_0 PDI1 —	—	SIUL FlexCAN_0 PDI —	I/O	M1	None, None	106	130	T15
PB[1]	PCR[17]	Option 0 Option 1 Option 2 Option3	GPIO[17] CANRX_0 PDI0 —	—	SIUL FlexCAN_0 PDI —	I/O	S	None, None	105	129	T14
PB[2]	PCR[18]	Option 0 Option 1 Option 2 Option3	GPIO[18] TXD_0 — —	—	SIUL LINFlex_0 — —	I/O	S	None, None	112	140	R14
PB[3]	PCR[19]	Option 0 Option 1 Option 2 Option3	GPIO[19] RXD_0 — —	—	SIUL LINFlex_0 — —	I/O	S	None, None	111	139	R13
PB[4]	PCR[20]	Option 0 Option 1 Option 2 Option 3	GPIO[20] SCK_1 MA0 —	—	SIUL DSPI_1 ADC —	I/O	M1	None, None	48	62	P8
PB[5]	PCR[21]	Option 0 Option 1 Option 2 Option 3	GPIO[21] SOUT_1 MA1 FABM	—	SIUL DSPI_1 ADC Control	I/O	M1	Input, Pulldown	49	63	N8
PB[6]	PCR[22]	Option 0 Option 1 Option 2 Option 3	GPIO[22] SIN_1 MA2 ABS[0]	—	SIUL DSPI_1 ADC Control	I/O	S	Input, Pullup	50	66	R7
PB[7]	PCR[23]	Option 0 Option 1 Option 2 Option 3	GPIO[23] SIN_0 eMIOSB[22] —	—	SIUL DSPI_0 PWM/Timer —	I/O	S	None, None	46	56	P7

Table 8. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number		
									144 LQFP	176 LQFP	208 MAPBGA
PB[8]	PCR[24]	Option 0 Option 1 Option 2 Option 3	GPIO[24] SOUT_0 eMIOSB[21] —	—	SIUL DSPI_0 PWM/Timer —	I/O	M1	None, None	45	55	N7
PB[9]	PCR[25]	Option 0 Option 1 Option 2 Option 3	GPIO[25] SCK_0 eMIOSB[20] —	—	SIUL DSPI_0 PWM/Timer —	I/O	M1	None, None	44	54	T6
PB[10]	PCR[26]	Option 0 Option 1 Option 2 Option 3	GPIO[26] CANRX_1 PDI2 eMIOSA[23]	—	SIUL FlexCAN_1 PDI PWM/Timer	I/O	S	None, None	107	131	P13
PB[11]	PCR[27]	Option 0 Option 1 Option 2 Option 3	GPIO[27] CANTX_1 PDI3 eMIOSA[16]	—	SIUL FlexCAN_1 PDI PWM/Timer	I/O	M1	None, None	108	132	N12
PB[12]	PCR[28]	Option 0 Option 1 Option 2 Option 3	GPIO[28] RXD_1 eMIOSB[19] PCS2_0	—	SIUL LINFlex_1 PWM/Timer DSPI_0	I/O	S	None, None	40	48	R6
PB[13]	PCR[29]	Option 0 Option 1 Option 2 Option 3	GPIO[29] TXD_1 eMIOSB[18] PCS1_0	—	SIUL LINFlex_1 PWM/Timer DSPI_0	I/O	S	None, None	41	49	P6
PB[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PB[15]	—	—	Reserved	—	—	—	—	—	—	—	—
PC[0]	PCR[30]	Option 0 Option 1 Option 2 Option 3	GPIO[30] — — —	ANS[0]	SIUL — — —	I/O	J	None, None	72	88	T13
PC[1]	PCR[31]	Option 0 Option 1 Option 2 Option 3	GPIO[31] — — —	ANS[1]	SIUL — — —	I/O	J	None, None	71	87	T12

Table 9. Pad type descriptions

Abbreviation[1]	Description
F	Fast (with GPIO and digital alternate function)
J	Slow pads with analog muxing (built for ADC channels)
M1	Medium (with GPIO and digital alternate function)
M2	Programmable medium/slow pad (programmed via the slew rate control in the PCR): Slew rate disabled: Slow driver configuration (AC/DC parameters same as for a slow pad) Slew rate enabled: Medium driver configuration (AC/DC parameters same as for a medium pad)
S	Slow (with GPIO and digital alternate function)
SMD	Stepper motor driver (with slew rate control)
X	Oscillator

1 The pad descriptions refer to the different Pad Configuration Register (PCR) types. Chapter 37, System Integration Unit Lite (SIUL), for the features available for each pad type.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using Equation 4:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 4}$$

where:

T_T = thermocouple temperature on top of the package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
805 East Middlefield Rd.
Mountain View, CA 94043 USA
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

3.6 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

3.6.1 EMC requirements on board

The following practices help minimize noise in applications.

- Place a 100 nF capacitor between each of the V_{DD12}/V_{SS12} supply pairs and also between the V_{DDPLL}/V_{SSPLL} pair. The voltage regulator also requires stability capacitors for these supply pairs.
- Place a 10 µF capacitor on VDDR.
- Isolate VDDR with ballast emitter to avoid voltage droop during STANDBY mode exit.
- Enable pad slew rate only as necessary to eliminate I/O noise:
  - Enabling slew rate for SMD pads will reduce noise on motors.
  - Disabling slew rate for non-SMD pads will reduce noise on non-SMD I/Os.
- Enable PLL modulation (± 2%) for system clock.
- Place decoupling capacitors for all HV supplies close to the pins.

3.6.2 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

- Software recommendations — The software flowchart must include the management of runaway conditions such as:
  - — Corrupted program counter
  - — Unexpected reset
  - — Critical data corruption (control registers...)
- Prequalification trials — Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

3.6.3 Electromagnetic interference (EMI)

Table 18. EMI testing specifications[1]

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	SR	T	Scan range	150 kHz – 30 MHz: RBW 9 kHz, step size 5 kHz 30 MHz – 1 GHz: RBW 120 kHz, step size 80 kHz	0.15	—	1000	MHz
—	SR	T	Operating frequency	Crystal frequency 8 MHz	—	64	—	MHz
—	SR	T	V_{DD12}, V_{DDPLL} operating voltages	—	—	1.28	—	V
—	SR	T	VDD, VDDA operating voltages	—	—	5	—	V
—	SR	T	Maximum amplitude	No PLL frequency modulation	—	33	—	dBµV
				±2% PLL frequency modulation	—	30	—	
—	SR	T	Operating temperature	—	—	25	—	°C

[1] EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03.

3.6.4 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

3.6.4.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 19. ESD absolute maximum ratings[1] [2]

Symbol		C	Ratings	Conditions	Class	Max value	Unit
$V_{ESD(HBM)}$	CC	T	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	CC	T	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	CC	T	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
						750 (corners)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3.6.4.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 20. Latch-up results

Symbol		C	Parameter	Conditions	Class
LU	CC	T	Static latch-up class	T_A = 105 °C conforming to JESD 78	II level A

3.7 Power management electrical characteristics

3.7.1 Voltage regulator electrical characteristics

The internal high power or main regulator (HPREG) requires an external NPN ballast transistor (see Table 21 and Table 22) to be connected as shown in Figure 7 as well as an external capacitance (C_{REG}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 15 nH.

For the MPC5606S microcontroller, 100 nF should be placed between each of the V_{DD12}/V_{SS12} supply pairs and also between the V_{DDPLL}/V_{SSPLL} pair. These decoupling capacitors are in addition to the required stability capacitance. Additionally, 10 µF should be placed between the V_{DDR} pin and the adjacent V_{SS} pin.

V_{DDR} = 3.0 V to 3.6 V / 4.5 V to 5.5 V, T_A = –40 to 105 °C, unless otherwise specified.

Table 27. DC electrical characteristics

Symbol		C	Parameter	Conditions[1]	T_A	Value			Unit
						Min	Typ	Max	
I_{DDRUN}[2]	CC	P	RUN mode current	—		—	130	180	mA
I_{DDHALT}	CC	P	HALT mode current	—		—	4	25	mA
I_{DDSTOP}	CC	P	STOP mode current	16 MHz fast internal RC oscillator off, HPVREG off	25°C	—	250	1800	µA
					105°C	—	5	20	mA
				16 MHz fast internal RC oscillator off, HPVREG on	25°C	—	2.5	6.5	mA
					105°C	—	7	25	mA
$I_{DDSTDBY}$	CC	C	STANDBY mode current	See Table 28					
$I_{DDSTDBY1}$[3]	CC	P	STANDBY1 mode current		25°C	—	20	100	µA
					105°C	—	180	—	µA
				T_J = 150°C	—	—	350	1500	µA
$I_{DDSTDBY2}$[4]	CC	P	STANDBY2 mode current		25°C	—	30	100	µA
					105°C	—	350	—	µA
				T_J = 150°C	—	—	600	2500	µA

1 V_{DD} = 3.3 V ±10% / 5.0 V ±10%, T_A = –40 to 105 °C

2 Value is for maximum peripherals turned on. May vary significantly based on different configurations, active peripherals, operating frequency, etc.

3 ULPreg on, HP/LPVreg off, 8 KB RAM on, device configured for minimum consumption, all possible modules switched off.

4 ULPreg on, HP/LPVreg off, 32 KB RAM on, device configured for minimum consumption, all possible modules switched off.

Table 28. IDDSTDBY specification[1]

Temperature (T_A,°C)	FIRC off, 8 KB RAM on		FIRC on, 8 KB RAM on		32 kHz SXOSC on, 8 KB RAM on		32 kHz SXOSC on, all RAM on	
	3.3 V	5.5 V	3.3 V	5.5 V	3.3 V	5.5 V	3.3 V	5.5 V
–40	16 µA	25 µA	326 µA	340 µA	16 µA	26 µA	22 µA	32 µA
0	18 µA	29 µA	334 µA	347 µA	19 µA	29 µA	26 µA	37 µA
25	23 µA	33 µA	342 µA	355 µA	24 µA	34 µA	34 µA	45 µA
55	41 µA	51 µA	363 µA	377 µA	42 µA	53 µA	69 µA	80 µA
85	93 µA	104 µA	421 µA	435 µA	100 µA	110 µA	182 µA	195 µA
105	173 µA	185 µA	502 µA	517 µA	181 µA	194 µA	344 µA	358 µA
125[2]	320 µA	334 µA	648 µA	667 µA	321 µA	335 µA	620 µA	638 µA
150[2]	681 µA	698 µA	1005 µA	1028 µA	654 µA	677 µA	1270 µA	1300 µA

1 All current values are typical values.

2 Values provided for reference only. The permitted temperature range of the chip is specified separately.

3.7.4 Recommended power-up and power-down order

Figure 10 shows the recommended order for powering up the power supplies on this device.

The 1.2 V regulator output starts after the device's internal POR (VDDREG HV) is deasserted at approximately 2.7 V on VDDREG.

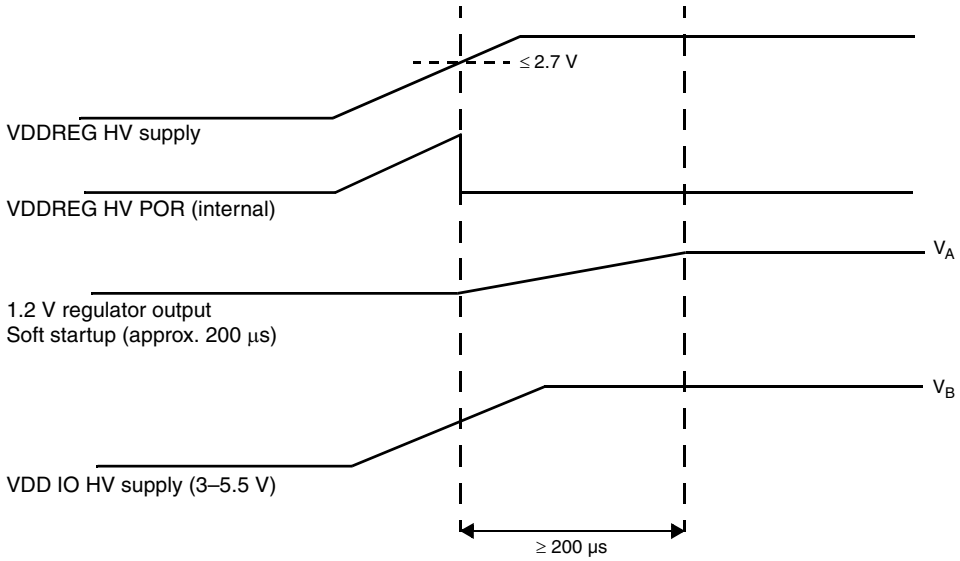

Figure 10. Recommended order for powering up the power supplies

CAUTION

The voltages V_A and V_B in Figure 10 must always obey the relation $V_B \geq V_A - 0.7$ V. Otherwise, currents from the 1.2 V supply to the 3.3 V supply may result.

Figure 11 shows the recommended order for powering down the power supplies on this device.

It is acceptable for the VDD IO HV supply to ramp down faster than the 1.2 V regulator output, even if the latter takes time to discharge the high 40 µF capacitance. (The capacitor will ultimately discharge.)

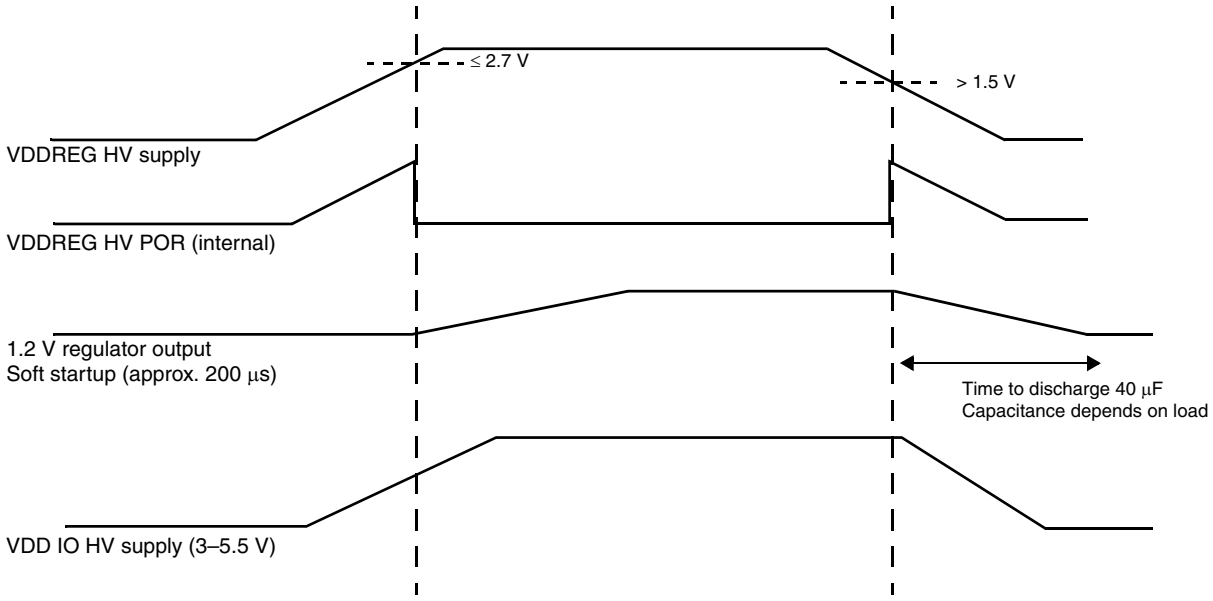

Figure 11. Recommended order for powering down the power supplies

CAUTION

The VDD IO HV supply must be disabled after the VDDREG HV supply voltage drops below 1.5 V. This is to ensure that the 1.2 V regulator shuts down before the 3.3 V regulator shuts down.

3.7.5 Power-up inrush current profile

Figure 12 shows the power up inrush current profile of the ballast transistor under the worst possible startup condition (fastest PVT and fastest power ramp time).

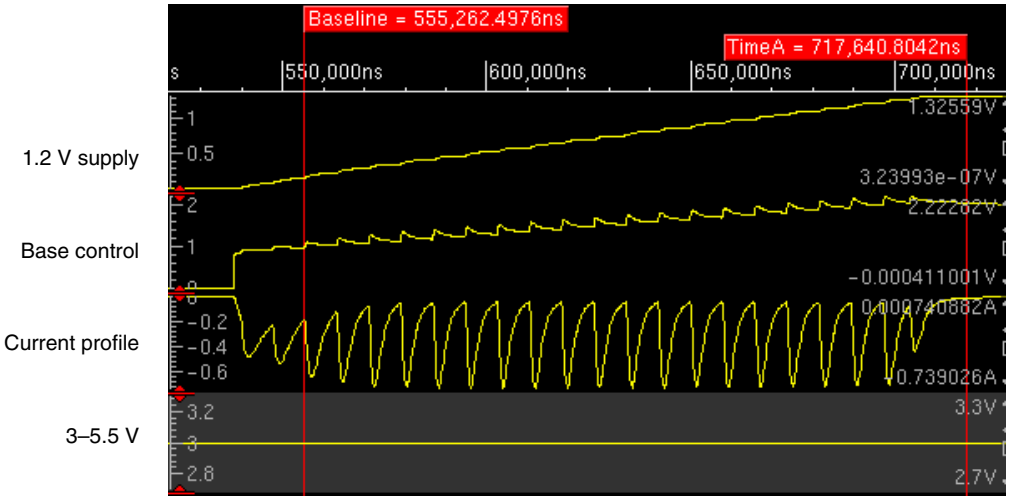

Figure 12. Power-up inrush current profile

Table 35. SMD pad electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{PU}	CC	P	Internal pull-up device current	$V_{in}=V_{IL}$	–130	—	—	µA
				$V_{in}=V_{IH}$	—	—	–10	
I_{PD}	CC	P	Internal pull-down device current	$V_{in}=V_{IL}$	10	—	—	
				$V_{in}=V_{IH}$	—	—	130	
I_{IN}	CC	P	Input leakage current	—	–1	—	1	
R_{DSONH}	CC	C	SMD pad driver active high impedance	$I_{OH} \leq -30$ mA[2]	—	—	16	Ω
R_{DSONL}	CC	C	SMD pad driver active low impedance	$I_{OL} \leq 30$ mA[2]	—	—	16	Ω
V_{OMATCH}	CC	C	Output driver matching V_{OH} / V_{OL}	I_{OH} / $I_{OL} \leq 30$ mA[2]	—	—	90	mV

1 VDD = 5.0 V ±10%, Tj = –40 to 150 °C.

2 VDD = 5.0 V ±10%, Tj = –40 to 130 °C.

3.8.4 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 36.

Table 37 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Table 36. I/O supply segment

Package	Supply segment				
	A[1]	B[2]	C[3,4]	D[5]	E[6]
144 LQFP	pins 1–21 pins 113–144	pins 22– 52	pins 53–72	pins 73–102	pins 103–112
176 LQFP	pins 1–21 pins 143–176	pins 22–68	pins 69–88	pins 89–118	pins 119–142

1 LCD pad segment containing pad supplies V_{DDE_A}

2 Miscellaneous pad segment containing pad supplies V_{DDE_B}

3 ADC pad segment containing pad supplies V_{DDE_C}

4 V_{DDE_C} should be the same as V_{DDA} with a 100 mV variation, i.e., $V_{DDE\_C} = V_{DDA} \pm 100$ mV.

5 Stepper Motor pad segment containing I/O supplies V_{DDMA}, V_{DDMB}, V_{DDMC}

6 Miscellaneous pad segment containing pad supplies V_{DDE_E}

Table 39. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS Schmitt Trigger	—	$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low level CMOS Schmitt Trigger	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	D	Input hysteresis CMOS Schmitt Trigger	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ±10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		D		Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ±10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C		Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ±10%, PAD3V5V = 1 (recommended)	—	—	0.5	
T_{tr}	CC	T	Output transition time output pin[3] MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	10	ns
		T		C_L = 50 pF, V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	20	
		T		C_L = 100 pF, V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	40	
		T		C_L = 25 pF, V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	12	
		T		C_L = 50 pF, V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	25	
		T		C_L = 100 pF, V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	1000	—	—	ns
I_{WPU}	CC	P	Weak pull-up current absolute value	—	10	—	150	µA
		D	RUN Current during RESET	Before Flash is ready	—	10	—	mA
				After Flash is ready	—	20	—	mA

1 V_{DD} = 3.3 V ±10% / 5.0 V ±10%, T_A = –40 to 105 °C, unless otherwise specified

2 This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to reset generation module (RGM) section of the device reference manual).

3 C_L includes device and package capacitance (C_{PKG} < 5 pF).

1 The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.

2 The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

Table 41. Resonator description

	CSTCR4M00G53-R0	CSTCR4M00G55-R0
Vibration	Fundamental	
Fr (kHz)	3929.50	3898.00
Fa (kHz)	4163.25	4123.00
Fa–Fr (dF) (kHz)	233.75	225.00
Ra (kΩ)	372.41	465.03
R1 (Ω)	12.78	11.38
L1 (mH)	0.84443	0.88244
C1 (pF)	1.94268	1.88917
Co (pF)	15.85730	15.90537
Qm	1630.93	1899.77
CL1 (nominal) (pF)	15	39
CL2 (nominal) (pF)	15	39

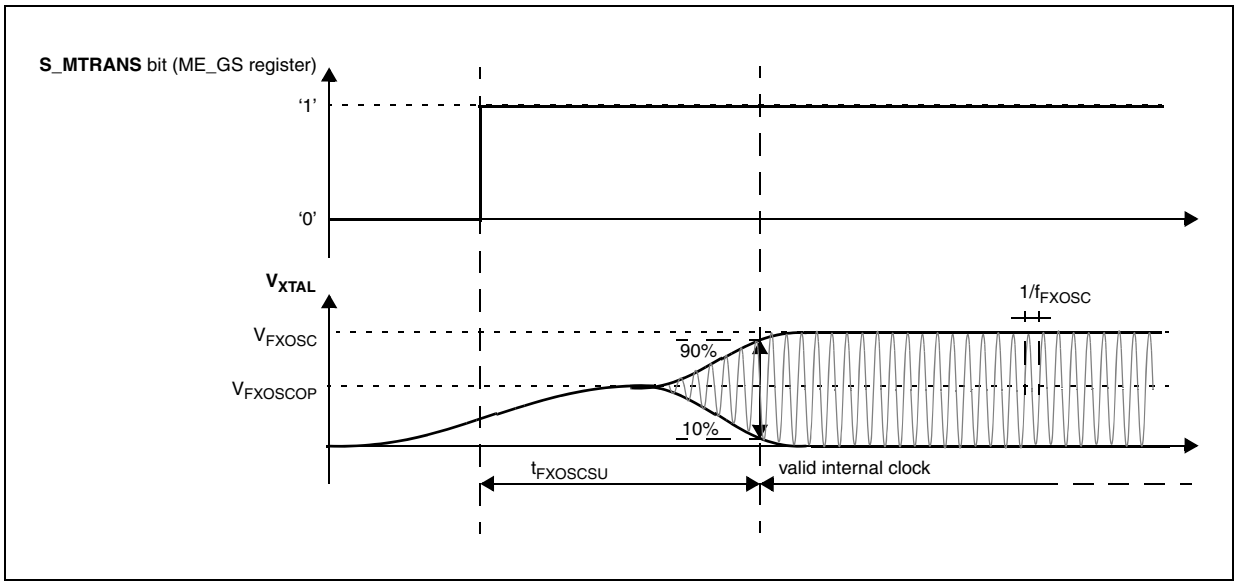

Figure 18. Fast external crystal oscillator (4–16 MHz) electrical characteristics

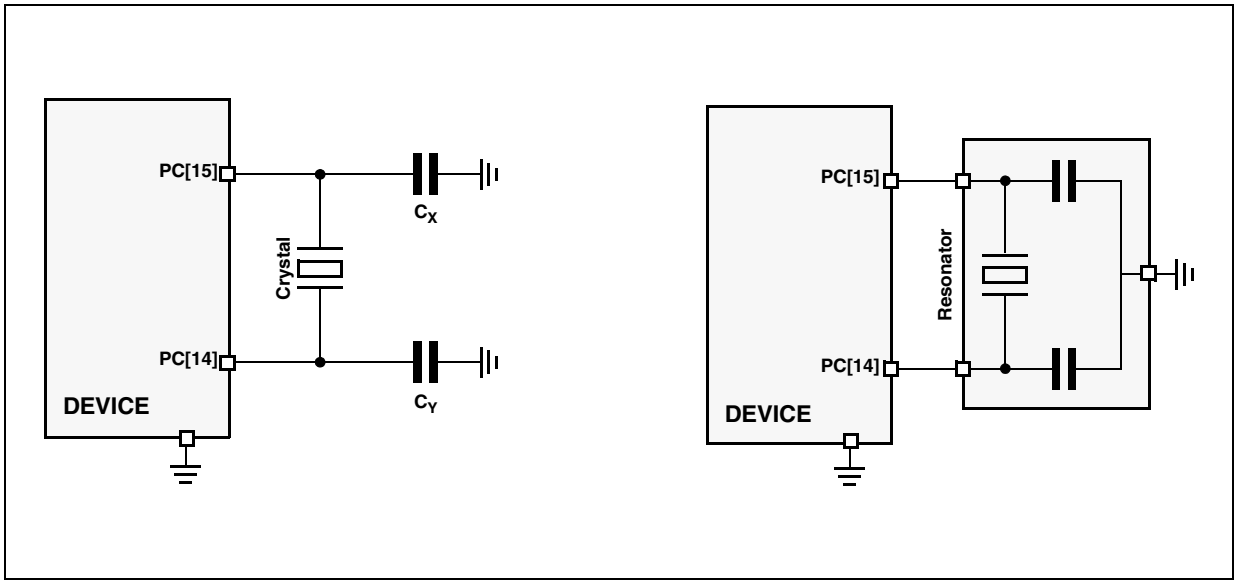

Figure 19. Crystal oscillator and resonator connection scheme

NOTE

PC[14]/PC[15] must not be directly used to drive external circuits.

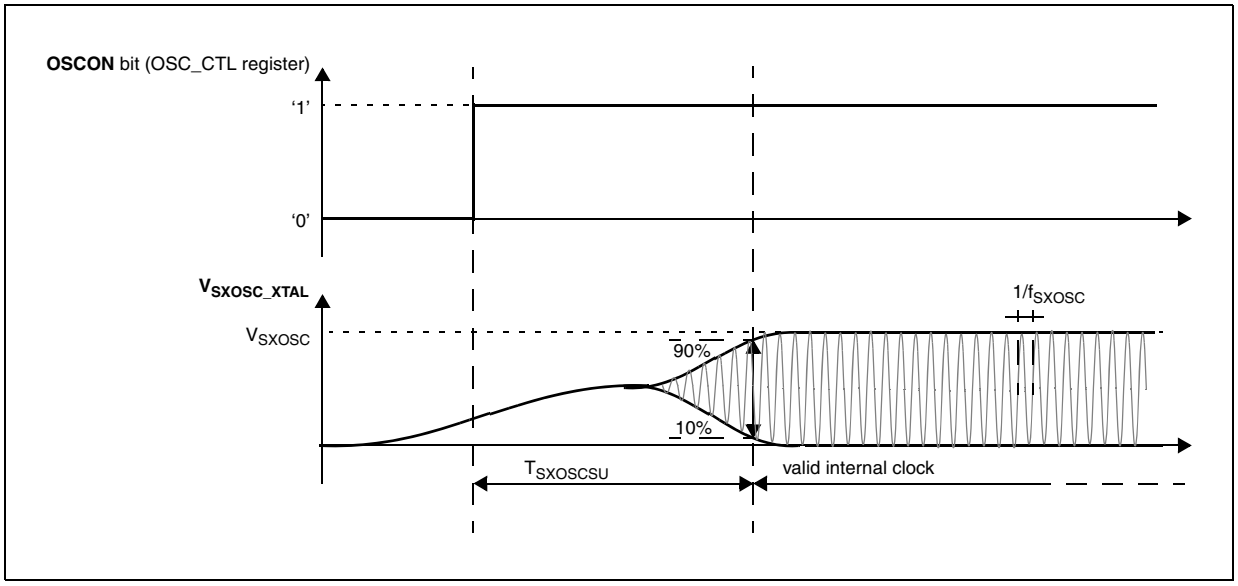

Figure 20. Slow external crystal oscillator (32 KHz) timing

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (f_c \times C_S)$, where f_c represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the Equation 7:

Eqn. 7

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 7 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

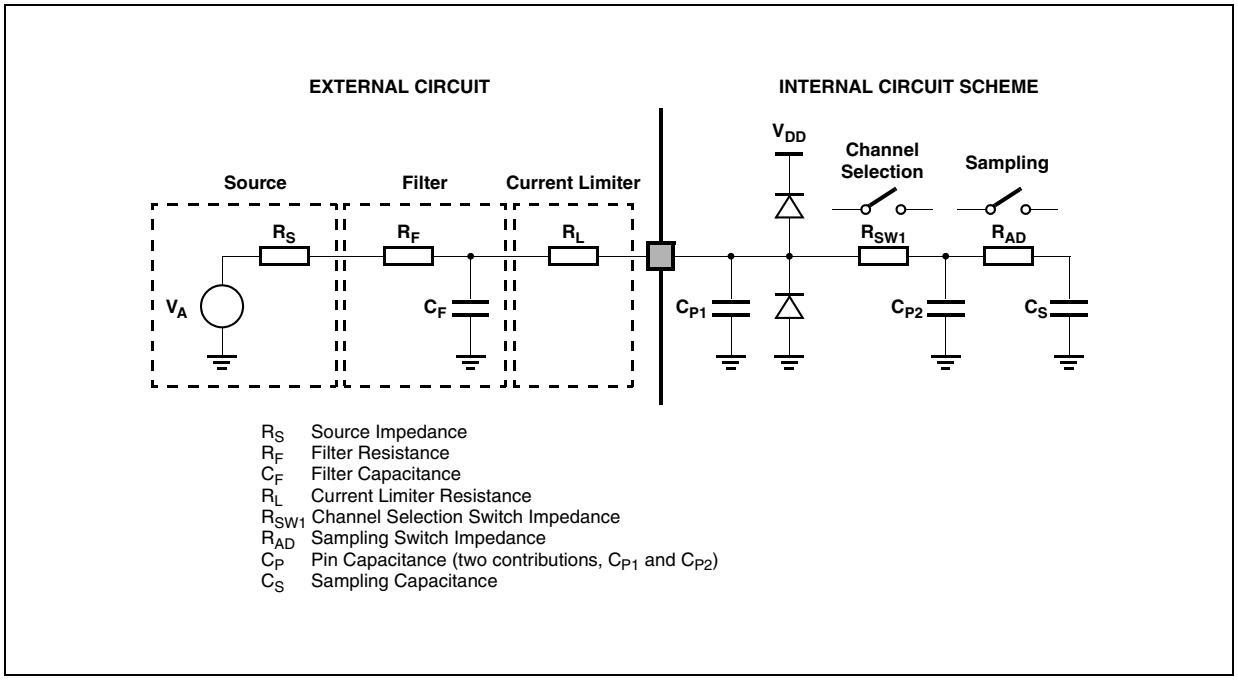

Figure 22. Input equivalent circuit (precise channels)

Table 50. ADC conversion characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SSA}	SR	D	Voltage on VSSA (ADC reference) pin with respect to ground (V_{SS})[2]	—	–0.1	—	0.1	V
V_{DDA}	SR	D	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SS})	—	V_{DD} – 0.1	—	V_{DD} + 0.1	V
V_{AINx}	SR	D	Analog input voltage[3]	—	V_{SSA} – 0.1	—	V_{DDA} + 0.1	V
f_{ADC}	SR	D	ADC analog frequency[4]	—	6	—	32	MHz
t_{ADC_PU}	SR	D	ADC power up delay	—	—	—	1.5	µs
t_{ADC_S}	CC	T	Sample time[5,6]	f_{ADC} = 32 MHz, ADC_conf_sample_input = 17	0.5	—	—	µs
		T		f_{ADC} = 6 MHz, ADC_conf_sample_input = 127	—	—	21	
t_{ADC_C}	CC	T	Conversion time[7]	f_{ADC} = 32 MHz, ADC_conf_comp = 2	0.625	—	—	µs
C_S	CC	D	ADC input sampling capacitance	—	—	—	3	pF
C_{P1}	CC	D	ADC input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC input pin capacitance 3	—	—	—	1	pF
R_{SW1}	CC	D	Internal resistance of analog source	—	—	—	1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—	—	—	1	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—	—	—	0.1	kΩ
I_{INJ}	SR	T	Input current Injection	Current injection on one ADC input, different from the converted one	–5	—	5	mA
INL	CC	P	Integral Non Linearity	No overload	2.5	—	2.5	LSB
DNL	CC	P	Differential Non Linearity	No overload	–1.0	—	1.0	LSB
OFS	CC	T	Offset error	After offset cancellation	—	0.5	—	LSB
GNE	CC	T	Gain error	—	—	0.6	—	LSB
TUEx	CC	P	Total unadjusted error for extended channel	Without current injection	–3	—	3	LSB
		T		With current injection	–4	—	4	

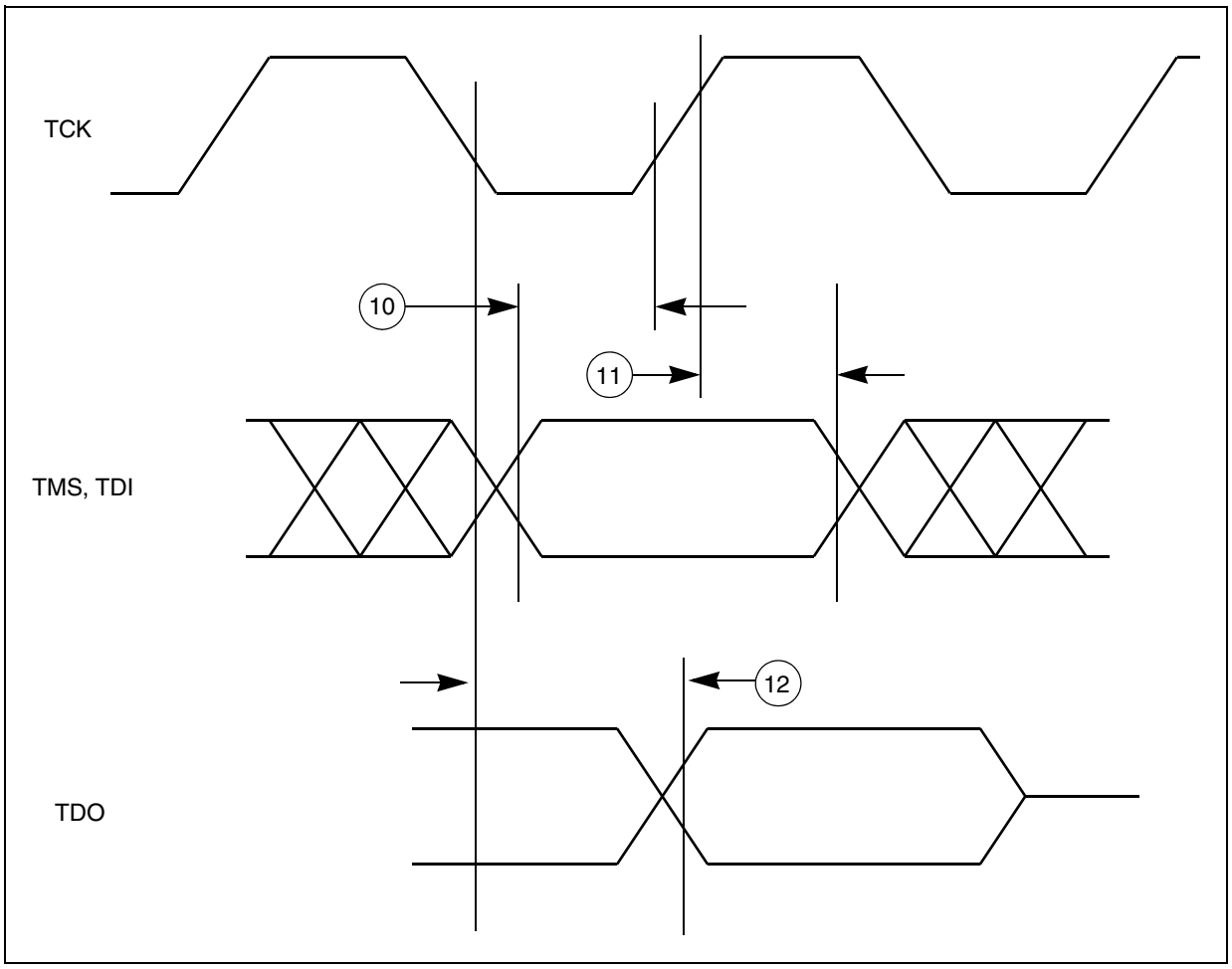

Figure 32. Nexus TDI, TMS, TDO timing

3.20.3 Interface to TFT LCD panels

Figure 33 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with positive polarity. The sequence of events for active matrix interface timing is:

1. DCU_CLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, DCU_CLK runs continuously.
2. DCU_HSYNC causes the panel to start a new line. It always encompasses at least one PCLK pulse.
3. DCU_VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
4. DCU_DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

3.20.3.2 Interface to TFT LCD panels

Table 58. TFT LCD interface timing parameters[1,2,3,4]

Symbol		C	Parameter	Value			Unit
				Min	Typ	Max	
t_{CKP}	CC	D	PDI clock period	15.25	—	—	ns
Δ_{CK}	CC	D	PDI clock duty cycle	40	—	60	%
t_{DSU}	CC	D	PDI data setup time	9.5	—	—	ns
t_{DHD}	CC	D	PDI data access hold time	4.5	—	—	ns
t_{CSU}	CC	D	PDI control signal setup time	9.5	—	—	ns
t_{CHD}	CC	D	PDI control signal hold time	4.5	—	—	ns
	CC	D	TFT interface data valid after pixel clock	—	—	6	ns
	CC	D	TFT interface VSYNC valid after pixel clock	—	—	5.5	ns
	CC	D	TFT interface DE valid after pixel clock	—	—	5.6	ns
	CC	D	TFT interface hold time for data and control bits	2	—	—	ns
	CC	D	Relative skew between the data bits	—	—	3.7	ns

1 The characteristics in this table are based on the assumption that data is output at positive edge and displays latch data on negative edge.

2 Intra bit skew is less than 2 ns.

3 Load C_L = 50 pF for panel frequency up to 20 MHz.

4 Load C_L = 25 pF for panel frequency from 20 to 32 MHz.

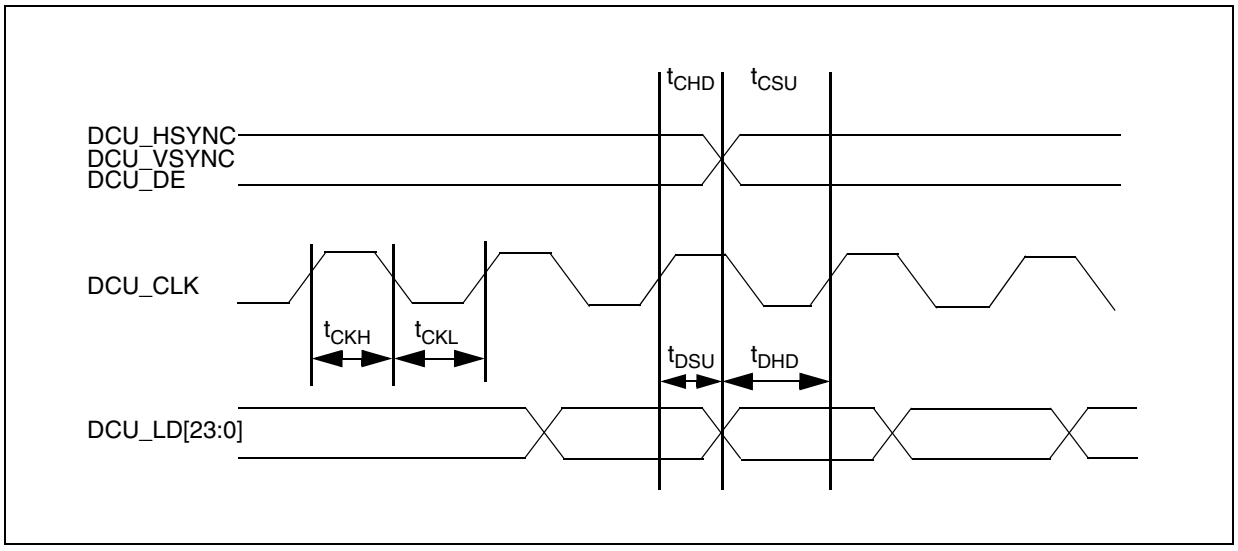

Figure 36. TFT LCD interface timing parameters