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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, QSPI, SCI, SPI
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	108
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5606sf2vlq6r

1.5.3 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows four concurrent transactions to occur from any master port to any slave port, but one of those transfers must be an instruction fetch from internal flash. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters having equal priority are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- Four master ports:
  - e200z0h core instruction port
  - e200z0h core complex load/store data port
  - eDMA controller
  - Display control unit
- Four slave ports:
  - One flash port dedicated to the CPU
  - Platform SRAM
  - QuadSPI serial flash controller
  - One slave port combining:
    - Flash port dedicated to the Display Control Unit and eDMA module
    - Graphics SRAM
    - Peripheral bridge
- 32-bit internal address bus, 32-bit internal data bus

1.5.4 Enhanced Direct Memory Access (eDMA)

The eDMA module is a controller capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine, that performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size. The eDMA module provides the following features:

- 16 channels support independent 8-, 16-, or 32-bit single value or block transfers.
- Supports variable-sized queues and circular queues.
- Source and destination address registers are independently configured to post-increment or remain constant.
- Each transfer is initiated by a peripheral, CPU, periodic timer interrupt, or eDMA channel request.
- Each DMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer.
- DMA transfers possible between system memories, QuadSPI, DSPIs, I^2C, ADC, eMIOS, and General Purpose I/Os (GPIOs).
- Programmable DMA Channel Mux allows assignment of any DMA source to any available DMA channel with as many as 64 potential request sources.

1.5.5 Inter-IC communications module (I^2C)

The I^2C module features the following:

- As many as four I^2C modules supported

- Eight clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for deglitching
- FIFOs for buffering as many as four transfers on the transmit and receive side
- General purpose I/O functionality on pins when not used for SPI
- Queueing operation possible through use of eDMA

1.5.17 FlexCAN

The MPC5606S MCU contains two controller area network (FlexCAN) modules. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth.

The FlexCan modules offer the following:

- Compliant with CAN protocol specification, Version 2.0B active
- 64 mailboxes, each configurable as transmit or receive
  - Mailboxes configurable while module remains synchronized to CAN bus
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - Individual programmable filters for each mailbox
  - Eight mailboxes configurable as a 6-entry receive FIFO
  - Eight programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid PLL jitter
- Listen-only mode capabilities
- CAN Sampler
  - Can catch the first message sent on the CAN network while the MPC5606S is stopped; this guarantees a clean startup of the system without missing messages on the CAN network
  - CAN sampler is connected to one of the CAN RX pins

1.5.18 Serial communication interface module (LINFlex)

The MPC5606S devices include as many as two LINFlex modules and support for LIN Master mode, LIN Slave mode, and UART mode. The modules are LIN state machine-compliant to the LIN 1.3 and 2.0 and 2.1 specifications and handle LIN frame transmission and reception without CPU intervention.

Other features include:

- Autonomous LIN frame handling
- Message buffer to store identifier and as many as 8 data bytes
- Supports message length as long as 64 bytes
- Detection and flagging of LIN errors
- Sync field, Delimiter, ID parity, Bit, Framing, Checksum, and Timeout errors
- Classic or extended checksum calculation

The PDI features the following:

- Supported color modes:
  - 8-bit mono
  - 8-bit color multiplexed
  - RGB565
  - 16-bit/18-bit RAW color
- Supported synchronization modes:
  - Embedded ITU-R BT.656-4 (RGB565 mode 2)
  - HSYNC, VSYNC
  - Data enable
- Direct interface with DCU background plane FIFO
- Synchronization generation for the DCU

1.5.26 Liquid Crystal Display (LCD) driver

The LCD driver module has two configurations allowing a maximum of 160 or 228 LCD segments:

- As many as 40 frontplane drivers and four backplane drivers
- As many as 38 frontplane drivers and six backplane drivers

Each segment is controlled and can be masked by a corresponding bit in the LCD RAM.

Four to six multiplex modes (1/1, 1/2, 1/3, 1/4, 1/5, 1/6 duty), and three bias (1/1, 1/2, 1/3) methods are available. All frontplane and backplane pins can be multiplexed with other port functions.

The LCD driver module features the following:

- Programmable frame clock generator from different clock sources:
  - System clock
  - Internal RC oscillator
- Programmable bias voltage level selector
- On-chip generation of all output voltage levels
  - LCD voltage reference taken from main 5 V supply
- LCD RAM – contains the data to be displayed on the LCD
  - Data can be read from or written to the display RAM at any time
- End-of-frame interrupt:
  - Optimize data refresh without visual artifacts
  - Selectable number of frames between each interrupt
- Contrast adjustment using programmable internal voltage reference
- Remapping capability of four or six backplanes with frontplanes
  - Increases pin selection flexibility
- In low-power modes, LCD operation can be suspended under software control; the LCD can also operate in low-power modes, clocked by the internal 128 kHz IRC or external 32 KHz crystal oscillator
- Selectable output current boost during transitions

1.5.27 Stepper Motor Controller (SMC)

The SMC module is a PWM motor controller suitable to drive instruments in a cluster configuration or any other loads requiring a PWM signal. The motor controller has twelve PWM channels associated with two pins each (24 pins in total).

The SMC module includes the following features:

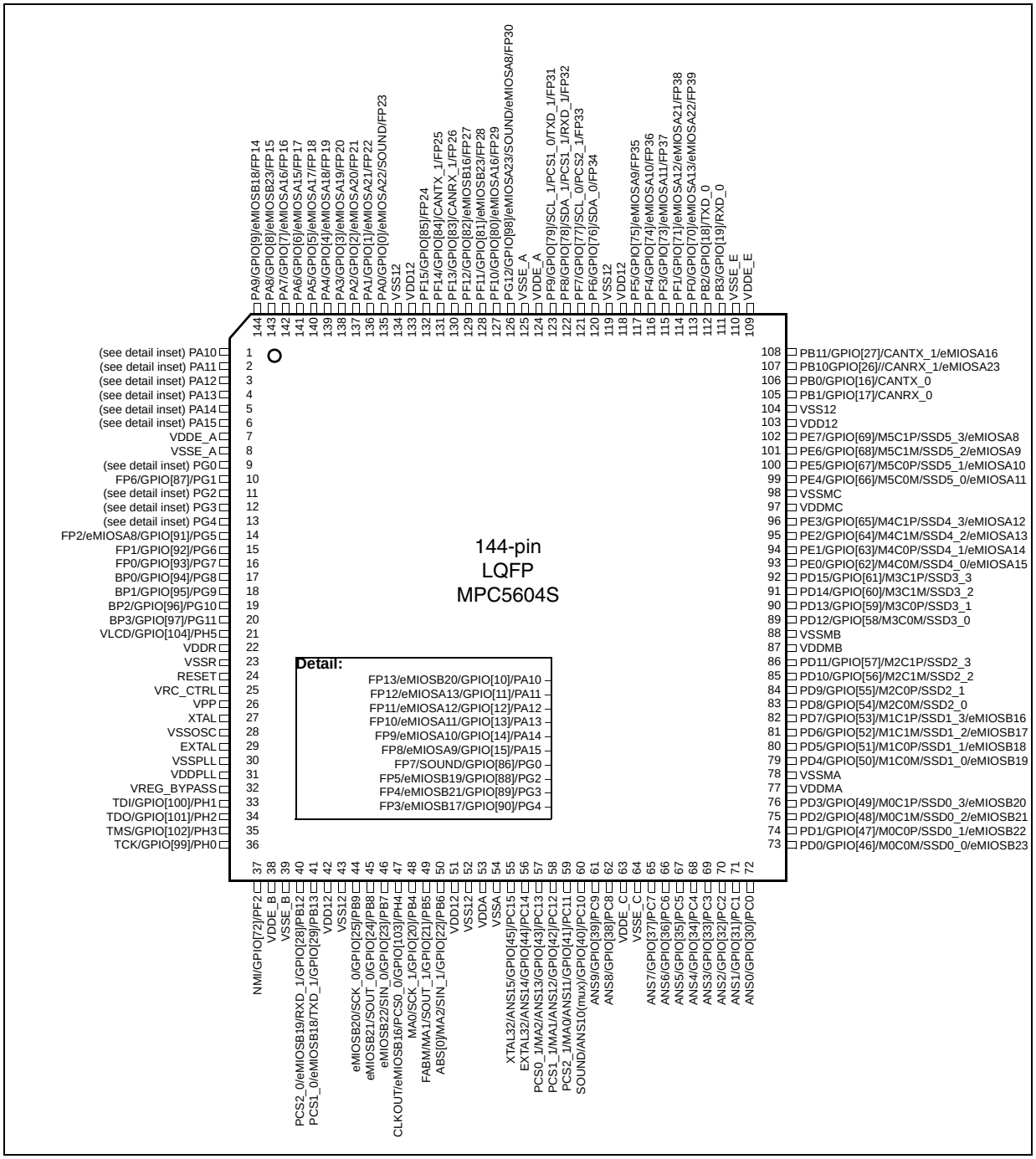


Figure 3. 144-pin LQFPpinout for MPC5604S

2.9.1 Signal details

Table 10. Signal details

Signal	Peripheral	Description
ABS[0]	BAM	Alternate Boot Select. Gives an option to boot by downloading code via CAN or LIN.
ANS[0:15]	ADC	Inputs used to bring into the device sensor-based signals for A/D conversion. ANS[0:15] connect to ATD channels [32:47].
MA[0:2]	ADC	These three control bits are output to enable the selection for an external Analog Mux for expansion channels. The available 8 multiplexed channels connect to ATD channels [64:71].
FABM		Force Alternate Boot mode. Forces the device to boot from the external bus (Can or LIN). If not asserted, the device boots up from the lowest flash sector containing a valid boot signature.
DCU_DE	DCU	Indicates that valid pixels are present.
DCU_HSYNC	DCU	Horizontal sync pulse for TFT-LCD display.
DCU_PCLK	DCU	Output pixel clock for TFT-LCD display.
DCU_R[0:7], DCU_G[0:7], DCU_B[0:7]	DCU	Red, green and blue color 8-bit pixel values for TFT-LCD displays.
DCU_TAG	DCU	Indicates when a tagged pixel is present in safety mode.
DCU_VSYNC	DCU	Vertical sync pulse for TFT-LCD display.
PCS[0..2]_0, PCS[0..2]_1	DSPI	Peripheral chip selects when device is in Master mode; not used in slave modes.
SCK_0, SCK_1	DSPI	SPI clock signal—bidirectional.
SIN_0, SIN_1	DSPI	SPI data input signal.
SOUT_0, SOUT_1	DSPI	SPI data output signal.
PCS0_2	QuadSPI	Peripheral chip select for serial flash mode or chip select 0 for SPI master mode.
IO2/PCS1_2	QuadSPI	Chip select 1 for SPI master mode and bidirectional IO2 for serial flash mode.
IO3/PCS2_2	QuadSPI	Chip select 2 for SPI master mode and bidirectional IO3 for serial flash mode.
IO0/SIN_2	QuadSPI	Data input signal for SPI master and slave modes and bidirectional IO0 for serial flash mode.
IO1/SOUT_2	QuadSPI	Data output signal for SPI master and slave modes and bidirectional IO1 for serial flash mode.
SCK_2	QuadSPI	Clock output signal for SPI master and serial flash modes and clock input signal for SPI slave mode.
eMIOSA[8:23], eMIOSB[16:23]	eMIOS	Enhanced Modular Input Output System. 16+8 channel eMIOS for timed input or output functions.

Table 14. Absolute maximum ratings (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{DDE_B}[1]	SR	C	Voltage on VDDE_B (I/O supply) pin with respect to ground (V_{SSE_B})	—	–0.3	6.0	V
V_{DDE_C}[1]	SR	C	Voltage on VDDE_C (I/O supply) pin with respect to ground (V_{SSE_C})	—	–0.3	6.0	V
V_{DDE_E}[1]	SR	C	Voltage on VDDE_E (I/O supply) pin with respect to ground (V_{SSE_E})	—	–0.3	6.0	V
V_{DDMA}[1]	SR	C	Voltage on VDDMA (stepper motor supply) pin with respect to ground (V_{SSMA})	—	–0.3	6.0	V
V_{DDMB}[1] V_{DDMC}[1]	SR	C	Voltage on VDDMB/C (stepper motor supply) pin with respect to ground (V_{SSMB})	—	–0.3	6.0	V
V_{SS}[2]	SR	C	I/O supply ground	—	0	0	V
V_{SSOSC}	SR	C	Voltage on VSSOSC (oscillator ground) pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{LCD}	SR	C	Voltage on VLCD (LCD supply) pin with respect to V_{SS}	—	0	V_{DDE_A} + 0.3	V
V_{IN}	SR	C	Voltage on any GPIO pin with respect to ground (V_{SS})	—	–0.3	6.0	V
		C		Relative to V_{DD}	–0.3	V_{DD} + 0.3[3]	
I_{INJPAD}	SR	C	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	C	Absolute sum of all injected input currents during overload condition	—	–50	50	
I_{MAX}	CC	D	Absolute maximum current drive rating	—	—	45	
$T_{STORAGE}$	SR	C	Storage temperature	—	–55	150	°C

1 Throughout the remainder of this document V_{DD} refers collectively to I/O voltage supplies, i.e., V_{DDE_A}, V_{DDE_B}, V_{DDE_C}, V_{DDE_E}, V_{DDMA}, V_{DDMB} and V_{DDMC}, unless otherwise noted.

2 Throughout the remainder of this document V_{SS} refers collectively to I/O voltage supply grounds, i.e., V_{SSE_A}, V_{SSE_B}, V_{SSE_C}, V_{SSE_E}, V_{SSMA}, V_{SSMB} and V_{SSMC}, unless otherwise noted.

3 As long as the current injection specification is adhered to, then a higher potential is allowed.

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

3.6.2 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

- Software recommendations — The software flowchart must include the management of runaway conditions such as:
  - — Corrupted program counter
  - — Unexpected reset
  - — Critical data corruption (control registers...)
- Prequalification trials — Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

3.6.3 Electromagnetic interference (EMI)

Table 18. EMI testing specifications[1]

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	SR	T	Scan range	150 kHz – 30 MHz: RBW 9 kHz, step size 5 kHz 30 MHz – 1 GHz: RBW 120 kHz, step size 80 kHz	0.15	—	1000	MHz
—	SR	T	Operating frequency	Crystal frequency 8 MHz	—	64	—	MHz
—	SR	T	V_{DD12}, V_{DDPLL} operating voltages	—	—	1.28	—	V
—	SR	T	VDD, VDDA operating voltages	—	—	5	—	V
—	SR	T	Maximum amplitude	No PLL frequency modulation	—	33	—	dBµV
				±2% PLL frequency modulation	—	30	—	
—	SR	T	Operating temperature	—	—	25	—	°C

[1] EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03.

3.6.4 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

3.6.4.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

- Fast pads — These provide maximum speed. There are used for improved NEXUS debugging capability.
- SMD pads — These provide additional current capability to drive stepper motor loads.
- Digital I/O with analog (J) pad — These provide input and output digital features and analog input for ADC.

M2 and Fast pads can disable slew rate to reduce electromagnetic emission, at the cost of reducing AC performance.

3.8.2 I/O input DC characteristics

Table 30 provides input DC electrical characteristics as described in Figure 14.

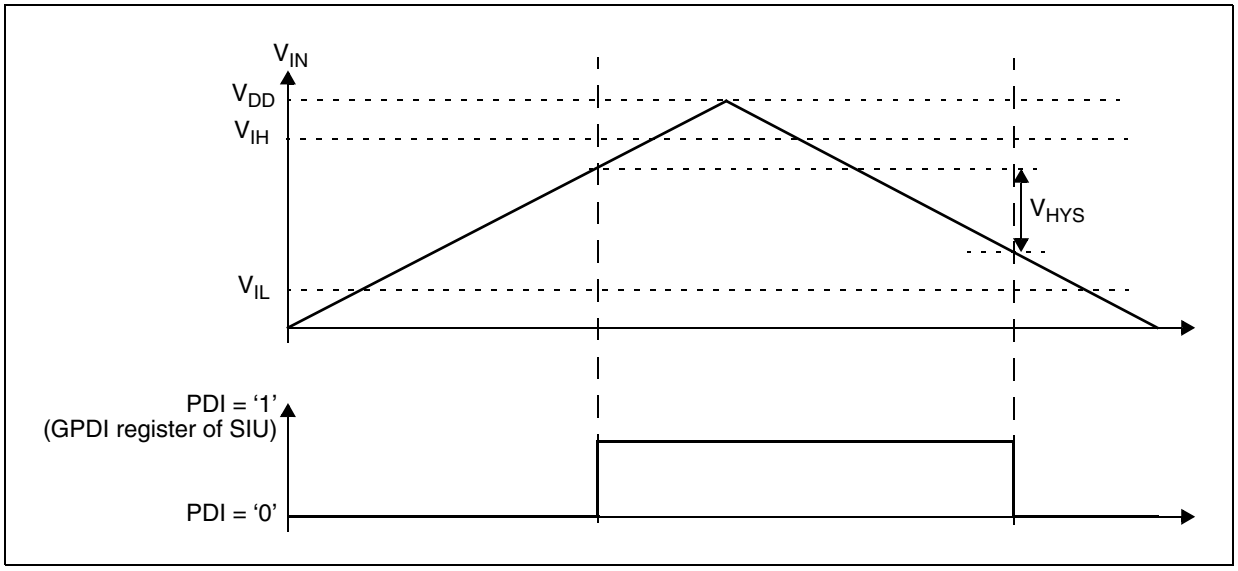


Figure 14. I/O input DC electrical characteristics definition

Table 30. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS Schmitt trigger	—	$0.65V_{DD}$	—	V_{DD} + 0.3	V
V_{IL}	SR	P	Input low level CMOS Schmitt trigger	—	–0.3	—	$0.35V_{DD}$	
V_{HYS}	CC	D	Input hysteresis CMOS Schmitt trigger	—	$0.1V_{DD}$	—	—	
I_{LKG}	CC	P	Input leakage current	—	–1	—	1	µA
				T_A = –40°C	—	2	—	nA
				T_A = 25°C	—	2	—	nA
		C		T_A = 105°C	—	12	500	nA
		P		T_J = 150°C	—	70	1000	nA
R_{ON}	CC	D	Resistance of the analog switch inside the J pad type[2]	Supply range 3.3–5 V	—	—	1	kΩ

[1] V_{DD} = 3.3 V ±10% / 5.0 V ±10%, T_A = –40 to 105 °C.

[2] Applies to the J pad type only.

3.8.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 31 provides weak pull figures. Both pull-up and pull-down resistances are supported.
- Table 32 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 33 provides output driver characteristics for I/O pads when in MEDIUM configuration (applies to both M1 and M2 type pads).
- Table 34 provides output driver characteristics for I/O pads when in FAST configuration.
- Table 35 provides SMD pad characteristics.

Table 31. I/O pull-up/pull-down DC electrical characteristics [1]

Symbol		C	Parameter	Conditions[2]		Value			Unit
						Min	Typ	Max	
$\lvert I_{W-PU} \rvert$	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD} = 5.0V ±10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[3]	10	—	250	
		P		$V_{IN} = V_{IL}$, V_{DD} = 3.3V ±10%	PAD3V5V = 1	10	—	150	
$\lvert I_{W-PD} \rvert$	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IL}$, V_{DD} = 5.0V ±10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1	10	—	250	
		P		$V_{IN} = V_{IL}$, V_{DD} = 3.3V ±10%	PAD3V5V = 1	10	—	150	

1 The pull currents are dependent on the HVE settings.

2 V_{DD} = 3.3 V ±10% / 5.0 V ±10%, T_A = –40 to 125 °C, unless otherwise specified.

3 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 32. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull, I_{OH} = –2 mA, V_{DD} = 5.0 V ±10%, PAD3V5V = 0 (recommended)	0.8V_{DD}	—	—	V
		D		Push Pull, I_{OH} = –2 mA, V_{DD} = 5.0 V ±10%, PAD3V5V = 1[2]	0.8V_{DD}	—	—	
		C		Push Pull, I_{OH} = –1 mA, V_{DD} = 3.3 V ±10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ±10%, PAD3V5V = 0 (recommended)	—	—	0.1V_{DD}	V
		D		Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ±10%, PAD3V5V = 1[2]	—	—	0.1V_{DD}	
		C		Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ±10%, PAD3V5V = 1 (recommended)	—	—	0.5	

Table 37. I/O consumption

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{SWTSLW}	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF, V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	20	mA
		D		C_L = 25 pF, V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	29	mA
		D		C_L = 25 pF, V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF, V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	110	mA
		D		C_L = 25 pF, V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root mean square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	2.3	mA
		D		C_L = 25 pF, 4 MHz V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	3.2	
		D		C_L = 100 pF, 2 MHz V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	6.6	
		D		C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	1.6	
		D		C_L = 25 pF, 4 MHz V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	2.3	
		D		C_L = 100 pF, 2 MHz V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	4.7	
I_{RMSMED}	CC	D	Root mean square I/O current for MEDIUM configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	6.6	mA
		D		C_L = 25 pF, 4 MHz V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	13.4	
		D		C_L = 100 pF, 2 MHz V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	18.3	
		D		C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	5.0	
		D		C_L = 25 pF, 4 MHz V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	8.5	
		D		C_L = 100 pF, 2 MHz V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	11.0	

Table 37. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{RMSFST}	CC	D	Root mean square I/O current for FAST configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	22.0	mA
		D		C_L = 25 pF, 4 MHz V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	33.0	
		D		C_L = 100 pF, 2 MHz V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	56.0	
		D		C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	14.0	
		D		C_L = 25 pF, 4 MHz V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	20.0	
		D		C_L = 100 pF, 2 MHz V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	25.0	
I_{DYNSEG}	SR	D	Sum of all the dynamic and static I/O current within a supply segment	V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	110	mA
		D		V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	65	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	70	mA
		D		V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	65	
$I_{DDMxAVG}$	SR	D	Sum of currents of two motors assigned to segment V_{DDMx}, V_{SSMx} pair	V_{DD} = 5.0 V ±10%, PAD3V5V = 0 T_J = 130 °C	—	—	90	
				V_{DD} = 5.0 V ±10%, PAD3V5V = 0 T_J = –40 °C	—	—	120	

[1] V_{DD} = 3.3 V ±10% / 5.0 V ±10%, T_A = –40 to 105 °C, unless otherwise specified

3.9 SSD specifications

3.9.1 Electrical characteristics

Table 38. SSD electrical characteristics

Symbol		C	Parameter	Value[1]			Unit
				Min	Typ	Max	
V_{VREF}	CC	P	Reference voltage (I_{VREF} = 0)	$V_{DDM}/2$ – 0.03	$V_{DDM}/2$	$V_{DDM}/2$ + 0.03	V
I_{VREF}	CC	P	Reference voltage output current	1.85	—	—	mA
R_{IN}	CC	D	Input resistance (against $V_{DDM}/2$)	0.8	1.0	1.2	MΩ
V_{IN}	CC	C	Input common mode range	V_{SSM}	—	V_{DDM}	V
SSD_{CONST}	CC	C	SSD constant	0.549	0.572	0.597	—

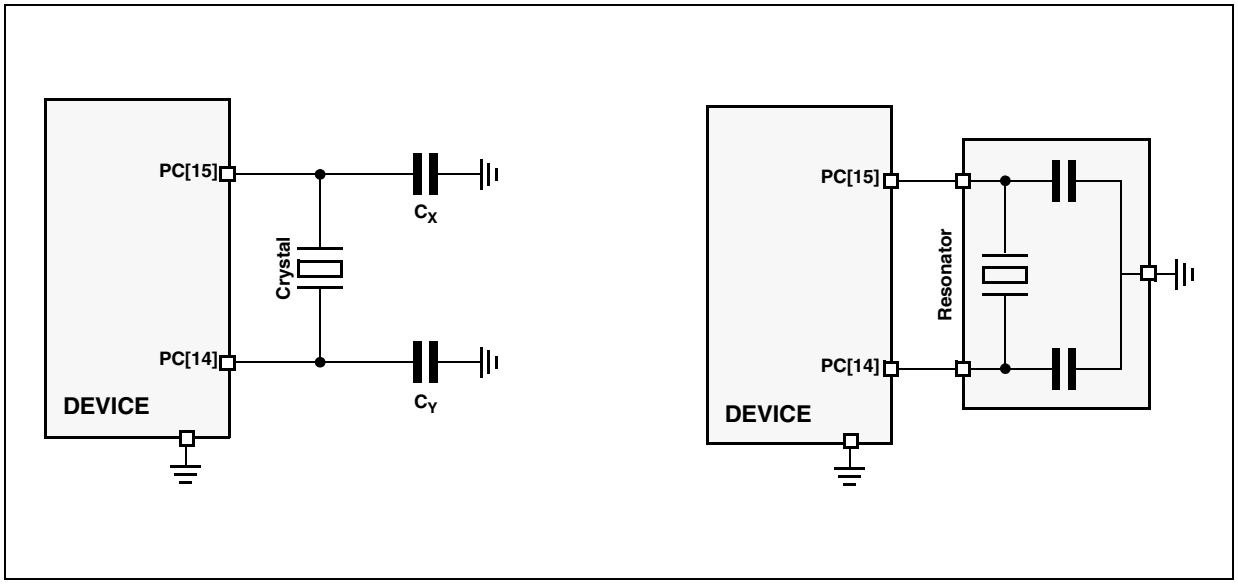


Figure 19. Crystal oscillator and resonator connection scheme

NOTE

PC[14]/PC[15] must not be directly used to drive external circuits.

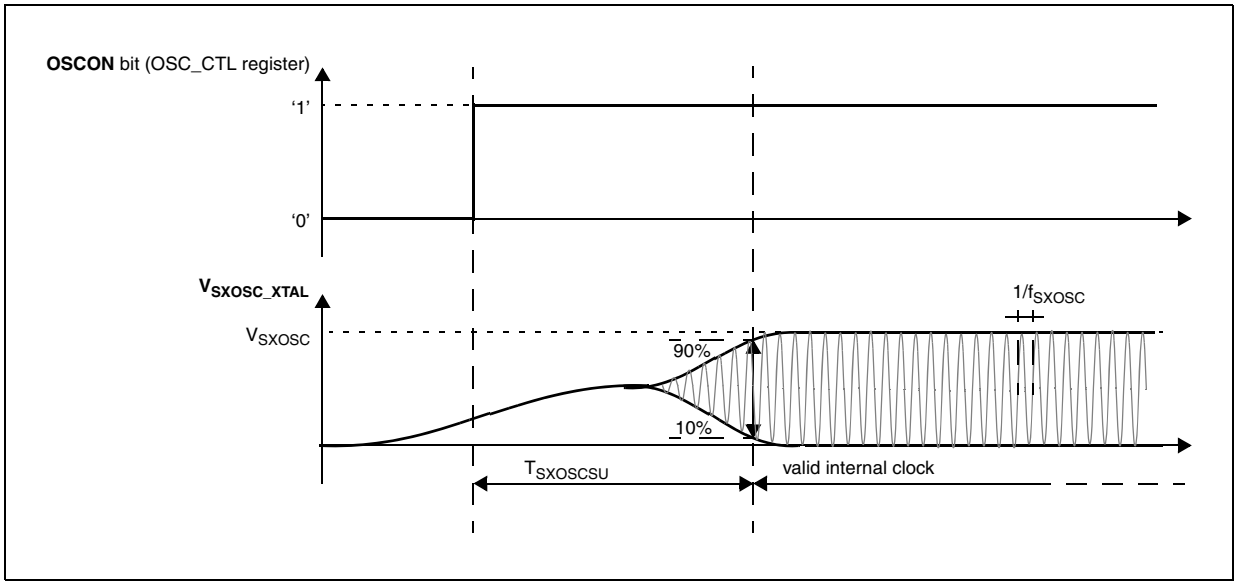


Figure 20. Slow external crystal oscillator (32 KHz) timing

Table 50. ADC conversion characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SSA}	SR	D	Voltage on VSSA (ADC reference) pin with respect to ground (V_{SS})[2]	—	–0.1	—	0.1	V
V_{DDA}	SR	D	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SS})	—	V_{DD} – 0.1	—	V_{DD} + 0.1	V
V_{AINx}	SR	D	Analog input voltage[3]	—	V_{SSA} – 0.1	—	V_{DDA} + 0.1	V
f_{ADC}	SR	D	ADC analog frequency[4]	—	6	—	32	MHz
t_{ADC_PU}	SR	D	ADC power up delay	—	—	—	1.5	µs
t_{ADC_S}	CC	T	Sample time[5,6]	f_{ADC} = 32 MHz, ADC_conf_sample_input = 17	0.5	—	—	µs
		T		f_{ADC} = 6 MHz, ADC_conf_sample_input = 127	—	—	21	
t_{ADC_C}	CC	T	Conversion time[7]	f_{ADC} = 32 MHz, ADC_conf_comp = 2	0.625	—	—	µs
C_S	CC	D	ADC input sampling capacitance	—	—	—	3	pF
C_{P1}	CC	D	ADC input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC input pin capacitance 3	—	—	—	1	pF
R_{SW1}	CC	D	Internal resistance of analog source	—	—	—	1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—	—	—	1	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—	—	—	0.1	kΩ
I_{INJ}	SR	T	Input current Injection	Current injection on one ADC input, different from the converted one	–5	—	5	mA
INL	CC	P	Integral Non Linearity	No overload	2.5	—	2.5	LSB
DNL	CC	P	Differential Non Linearity	No overload	–1.0	—	1.0	LSB
OFS	CC	T	Offset error	After offset cancellation	—	0.5	—	LSB
GNE	CC	T	Gain error	—	—	0.6	—	LSB
TUEx	CC	P	Total unadjusted error for extended channel	Without current injection	–3	—	3	LSB
		T		With current injection	–4	—	4	

Table 52. Pad AC specifications (5.0 V, PAD3V5V = 0)[1] (continued)

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
2	Medium	1	—	15	3	—	10	—	—	40	2.5	—	7	25
		1	—	15	5	—	20	—	—	20	2.5	—	7	50
		1	—	15	9	—	40	—	—	13	2.5	—	8	100
		1	—	15	12	—	70	—	—	7	2.5	—	8	200
3	Fast	1	—	6	1	—	4	—	—	100	18	—	55	25
		1	—	6	1.5	—	6	—	—	80	18	—	55	50
		1	—	6	3	—	12	—	—	40	18	—	55	100
		1	—	6	5	—	16	—	—	25	18	—	55	200
4	Pull Up/Down (5.5 V max)	—	—	—	—	—	5000	—	—	—	—	—	—	50
Parameter Classification		D			C			C			C			n/a

1 Propagation delay from $V_{DD}/2$ of internal signal to Pchannel/Nchannel on condition

2 Slope at rising/falling edge

Table 53. Pad AC specifications (3.3 V, PAD3V5V = 1)[1]

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	3	—	40	4	—	40	—	—	4	0.01	—	2	25
		3	—	40	6	—	50	—	—	2	0.01	—	2	50
		3	—	40	10	—	75	—	—	2	0.01	—	2	100
		3	—	40	14	—	100	—	—	2	0.01	—	2	200
2	Medium	1	—	15	2	—	12	—	—	40	2.5	—	7	25
		1	—	15	4	—	25	—	—	20	2.5	—	7	50
		1	—	15	8	—	40	—	—	13	2.5	—	7	100
		1	—	15	14	—	70	—	—	7	2.5	—	7	200

Table 57. LCD interface timing parameters—horizontal and vertical (continued)

Symbol		C	Parameter	Value	Unit
t_{BPV}	CC	D	VSYNC back porch width	BP_V × t_{HSP}	ns
t_{FPV}	CC	D	VSYNC front porch width	FP_V × t_{HSP}	ns
t_{SH}	CC	D	Screen height	DELTA_Y × t_{HSP}	ns
t_{VSP}	CC	D	VSYNC (frame) period	(PW_V + BP_V + FP_V + DELTA_Y) × t_{HSP}	ns

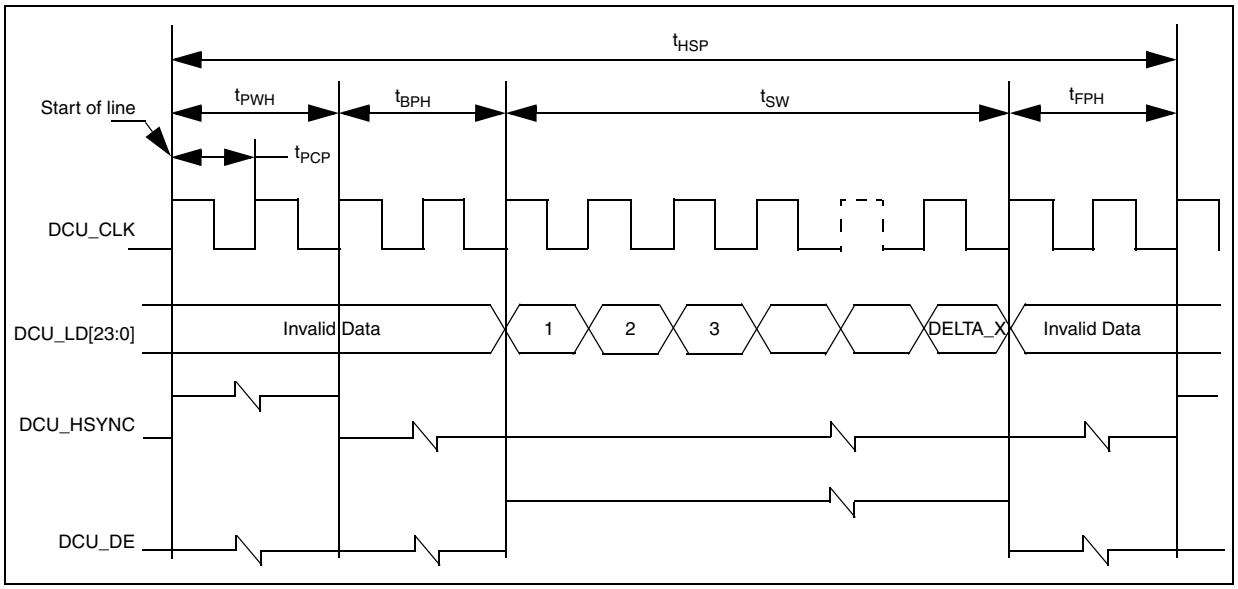


Figure 34. Horizontal sync timing

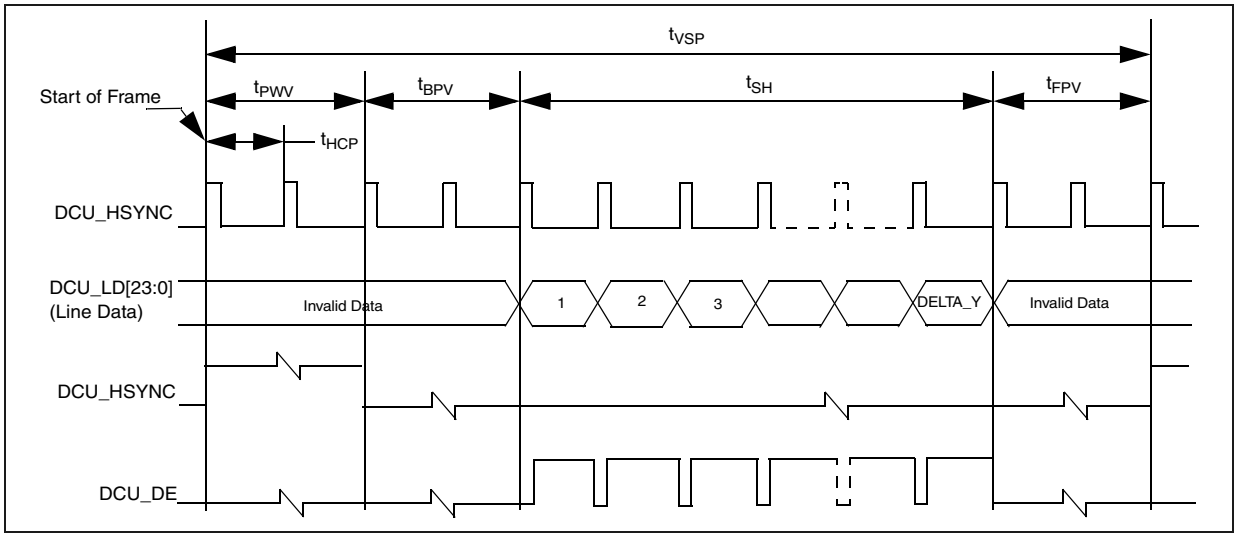


Figure 35. Vertical sync pulse

3.20.6 FlexCAN timing

The CAN functions are available as TX pins at normal I/O pads and as RX pins at the always on domain. There is no filter for the wakeup dominant pulse. Any high-to-low edge can cause wakeup if configured.

Table 61. FlexCAN timing[1]

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	t_{CANOV}	CC	D	CTNX Output Valid after CLKOUT Rising Edge (Output Delay)	—	22.48	ns
2	t_{CANSU}	CC	D	CNRX Input Valid to CLKOUT Rising Edge (Setup Time)	—	12.46	ns

1 FlexCAN timing specified at f_{SYS} = 64 MHz, V_{DD12} = 1.14 V to 1.32 V, VDDE_x = 3.0 V to 5.5 V, T_A = –40 to 105 °C, and C_L = 50 pF with SRC = 0b00.

3.20.7 Deserial Serial Peripheral Interface (DSPI)

Table 62. DSPI timing[1]

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{SCK}	CC	D	DSPI Cycle TIme[2,3]	Master (MTFE = 0) Slave (MTFE = 0) Slave Receive Only Mode	62 62 62	— — —	ns ns ns
2	t_{CSC}	CC	D	PCS to SCK Delay[4]	—	20	—	ns
3	t_{ASC}	CC	D	After SCK Delay[5]	—	20	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle	—	0.4 x t_{SCK}	0.6 x t_{SCK}	ns
5	t_A	CC	D	Slave Access Time (PCSx active to SOUT driven)	SS active to SOUT valid	—	40	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time (PCSx inactive to SOUT High-Z or invalid)	SS inactive to SOUT High-Z or invalid	—	10	ns
7	t_{PCSC}			PCSx to PCSS time	—	20	—	ns
8	t_{PASC}			PCSS to PCSx time	—	20	—	ns
9	t_{SUI}	CC	D	Data Setup Time for Inputs	Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[6] Master (MTFE = 1, CPHA = 1)	35 2 20 35	— — — —	ns ns ns ns
10	t_{HI}	CC	D	Data Hold Time for Inputs	Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[6] Master (MTFE = 1, CPHA = 1)	–5 5 10 –5	— — — —	ns ns ns ns

The clock profile in Figure 49 is measured at 30% to 70% levels of VDDE.

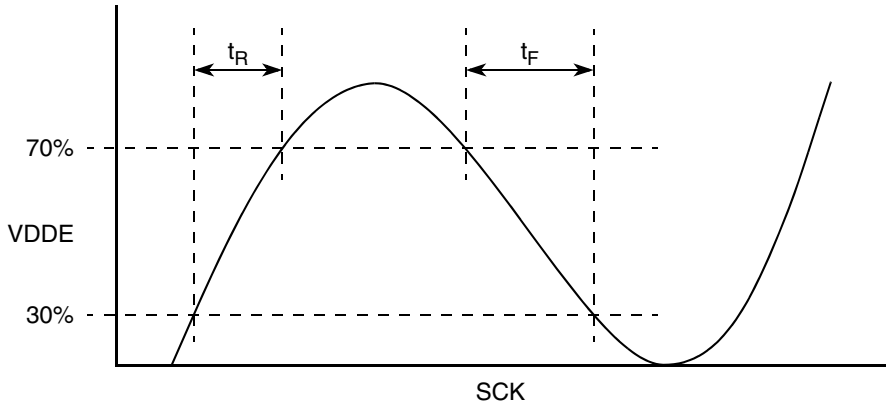
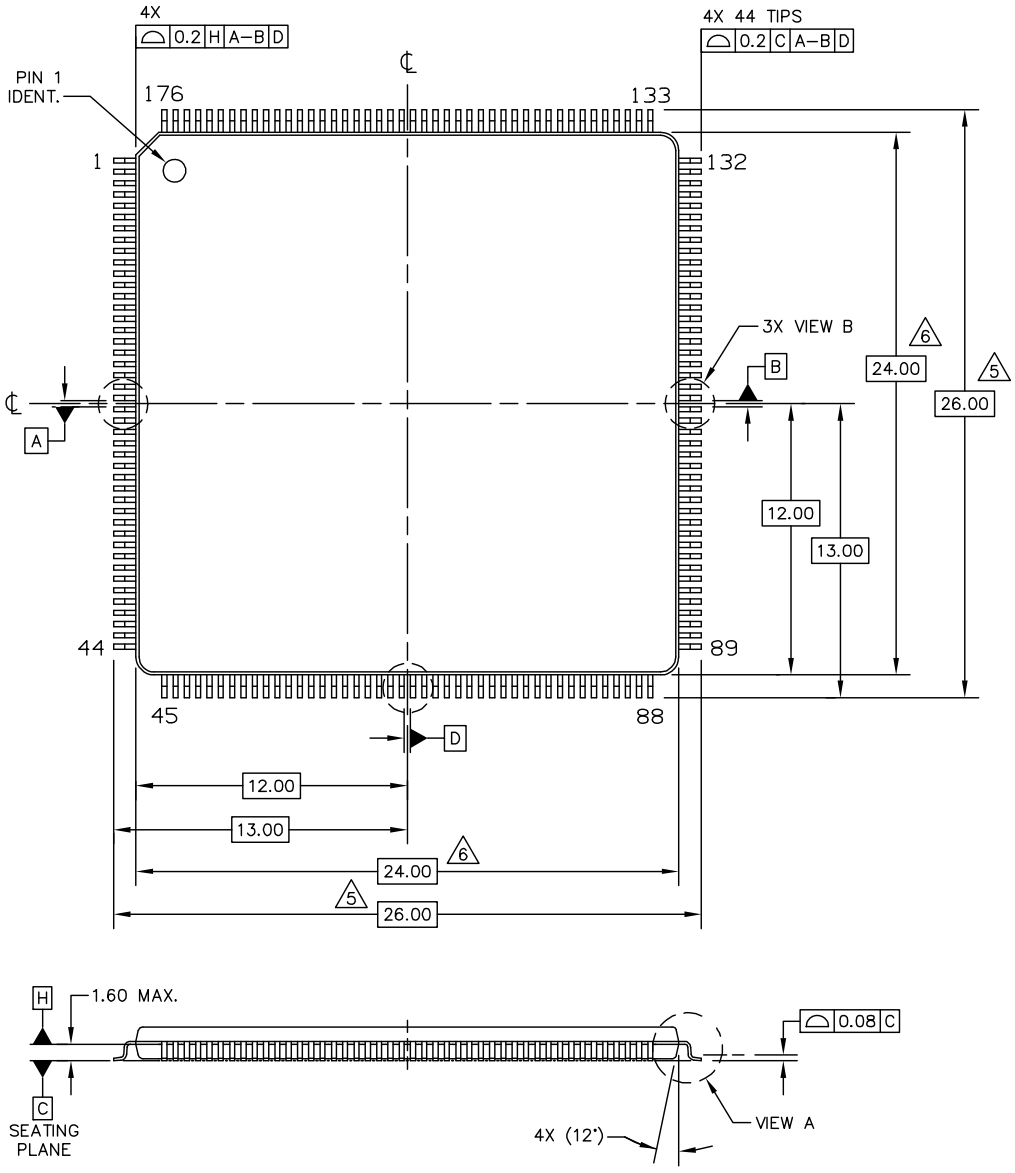


Figure 49. QuadSPI clock profile

4.2 176 LQFP



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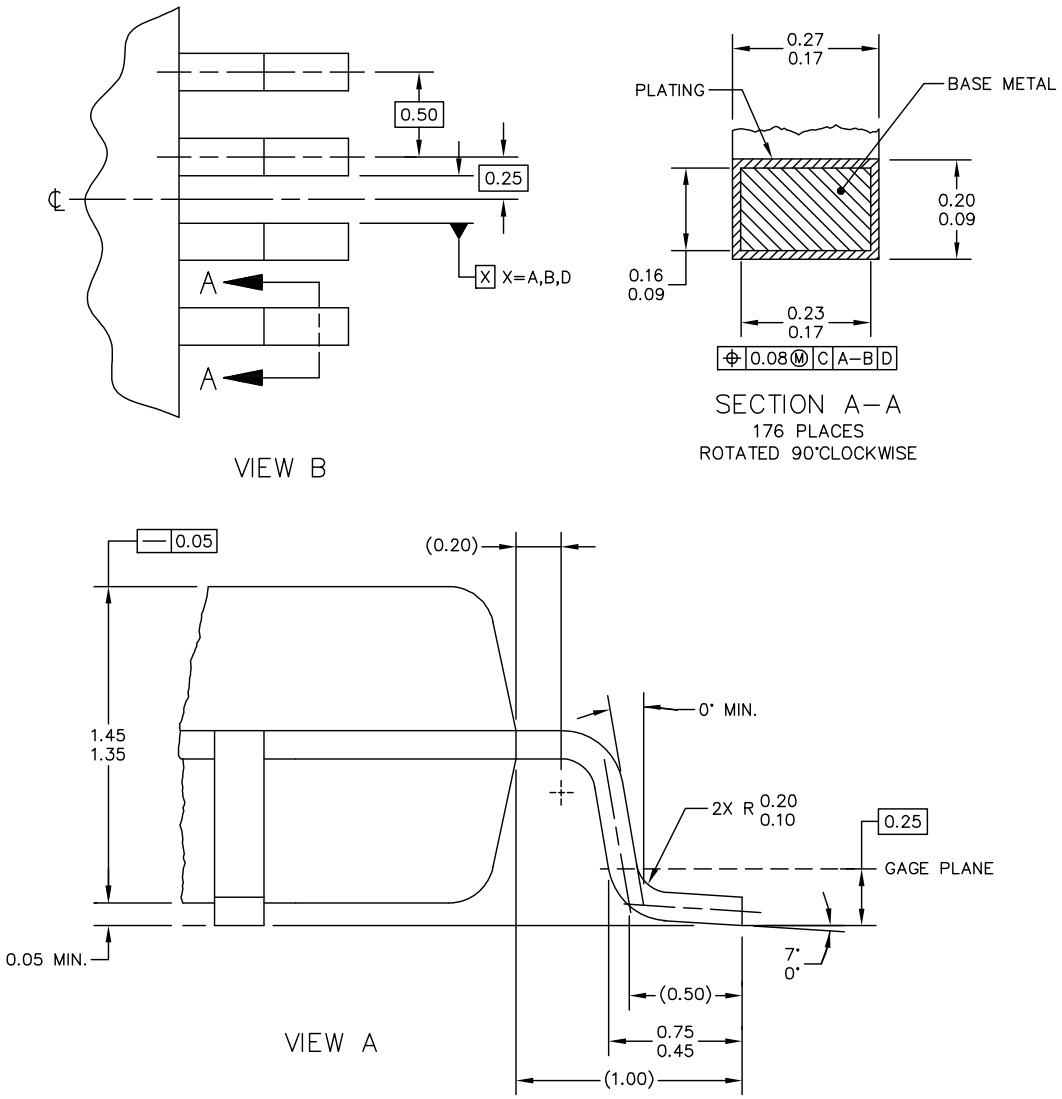
	CASE NUMBER: 1101–01	02 JUN 2005
	STANDARD: JEDEC MS–026 BGA	

Figure 53. LQFP176 mechanical drawing (Part 1 of 3)



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	CASE NUMBER: 1101–01	02 JUN 2005
	STANDARD: JEDEC MS–026 BGA	

Figure 54. LQFP176 mechanical drawing (Part 2 of 3)

Table 66. Document revision history

Revision	Date	Substantive changes
6	14 Jan 2011	Editorial changes and improvements. Swapped XTAL and EXTAL pins for the 208-pin BGA package and throughout. In the “Pinout and signal descriptions” section, changed WARNING labels to CAUTION labels. Updated the “Absolute maximum ratings” and “Recommended operating conditions” tables. Added footnote reference to V_{ss12} in “Recommended operating conditions (3.3 V)” table. Updated the “Connecting power supply pins” section. Removed footnote regarding characterization in the “Thermal characteristics” table. Updated the V_{DD12}/V_{DDPLL} operating voltages in the “Electromagnetic interference” table. Added typical values and updated the “Voltage regulator electrical characteristics,” “Low-power voltage regulator electrical characteristics,” and “Ultra-low-power voltage regulator electrical characteristics” tables. Updated classifications and values in the “Low voltage monitor electrical characteristics” table. Made major modifications and updates to the “DC electrical characteristics” table. Made major modifications and updates to the “I/O input DC electrical characteristics” table. Made major modifications and updates to the “I/O pull-up/pull-down DC electrical characteristics” table. Changed “SMC” pads to “SMD” pads throughout. Made updates to the “SMD pad electrical characteristics” table. Added run current during RESET to the “Reset electrical characteristics” table. Updated the FMPLL jitter (peak to peak) specification in the “FMPLL electrical characteristics” table. Updated f_{FIRC} and t_{FIRCSU} in the “Fast internal RC oscillator (16 MHz) electrical characteristics” table. Updated f_{SIRC} and t_{SIRCSU} in the “Slow internal RC oscillator (128 kHz) electrical characteristics” table. Removed “symmetric” pad type from the “Pad AC specifications (5.0 V, PAD3V5V = 0)” table. Removed “symmetric” pad type from the “Pad AC specifications (3.3 V, PAD3V5V = 1)” table. Updated V_{DD12} post-trimming minimum value in the “Low-power voltage regulator electrical characteristics” table. Updated V_{DD12} post-trimming minimum value in the “Ultra-low-power voltage regulator electrical characteristics” table. Updated $V_{LVDLVCORH}$ maximum value in the “Low voltage monitor electrical characteristics” table. Updated $V_{LVDLVCORL}$ minimum value in the “Low voltage monitor electrical characteristics” table. Updated value of V_{DD12}/V_{DDPLL} operating voltages in the “Input DC electrical characteristics” table. Corrected erroneous value of I_{LKG} (105°C case) in the “Input DC electrical characteristics” table.