Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, QSPI, SCI, SPI
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	136
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5606sf2vlu6

mode), and UART support; compliant with LIN protocol rev 2.1
- 2 full CAN 2.0B controllers with 64 configurable buffers each; bit rate programmable up to 1 Mbit/s
- Up to 4 Inter-integrated circuit (I^2C) internal bus controllers with master/slave bus interface
- Up to 133 configurable general purpose pins supporting input and output operations
- Real Time Counter (RTC) with multiple clock sources:
  - 128 kHz slow internal RC oscillator or 16 MHz fast internal RC oscillator supporting autonomous wakeup with 1 ms resolution with maximum timeout of 2 seconds
  - 32 kHz slow external crystal oscillator, supporting wakeup with 1 s resolution and maximum timeout of one hour
  - 4–16 MHz fast external crystal oscillator
- System timers:
  - 4-channel 32-bit System Timer Module (STM)—included in processor platform
  - 4-channel 32-bit Periodic Interrupt Timer (PIT) module
  - Software Watchdog Timer (SWT)
- System Integration Unit (SIU) module to manage resets, external interrupts, GPIO, and pad control
- System Status and Configuration Module (SSCM) to provide information for identification of the device, last boot mode, or debug status, and provides an entry point for the censorship password mechanism
- Clock Generation Module (MC_CGM) to generate system clock sources and provide a unified register interface, enabling access to all clock sources
- Clock Monitor Unit (CMU) to monitor the integrity of the main crystal oscillator and the PLL and act as a frequency meter, measuring the frequency of one clock source and comparing it to a reference clock
- Mode Entry Module (MC_ME) to control the device power mode, in other words, Run, Halt, Stop, or Standby control mode transition sequences, and manage the power control, voltage regulator, clock generation, and clock management modules
- Reset Generation Module (MC_RGM) to manage reset assertion and release to the device at initial startup
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class Two Plus standard
- Device/board boundary-scan testing supported per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator controller for regulating the 3.3 or 5 V supply voltage down to 1.2 V for core logic (requires external ballast transistor)
- The MPC5606S microcontrollers are offered in the following packages:[1]
  - 144 LQFP, 0.5 mm pitch, 20 mm × 20 mm outline
  - 176 LQFP, 0.5 mm pitch, 24 mm × 24 mm outline
  - 208 MAPBGA, 1.0 mm pitch, 17 mm × 17 mm outline (not a production package; available in limited quantities for tool development only)

1. See the device comparison table or orderable parts summary for package offerings for each device in the family.

1 Overview

1.1 Document overview

This document describes the device features and highlights important electrical and physical characteristics. For functional characteristics, see the *MPC5606S Microcontroller Reference Manual*.

1.2 Description

The MPC5606S family of chips is designed to enable the development of automotive instrument cluster applications by providing a single-chip solution capable of hosting real-time applications and driving a TFT display directly using an on-chip color TFT display controller.

MPC5606S chips incorporate a cost-efficient host processor core compliant with the Power Architecture® embedded category. The processor is 100% user-mode compatible with the Power Architecture and capitalizes on the available development infrastructure of current Power Architecture devices with full support from available software drivers, operating systems and configuration code to assist with users' implementations.

Offering high performance processing at speeds up to 64 MHz, the MPC5606S family is optimized for low power consumption and supports a range of on-chip SRAM and internal flash memory sizes. The version with 1 MB of flash memory (MPC5606S) features 160 KB of on-chip graphics SRAM.

See Table 1 for specific memory and feature sets of the product family members.

1.3 Device comparison

Table 1. MPC5606S family device comparison

Feature	MPC5602S	MPC5604S	MPC5606S
CPU	e200z0h		
Execution speed	Static – 64 MHz		
Flash memory (ECC)	256 KB	512 KB	1 MB
EEPROM Emulation Block (ECC)	4 × 16 KB		
RAM (ECC)	24 KB	48 KB	48 KB
Graphics RAM	No	No	160 KB
MPU	12 entry		
eDMA	16 channels		
Display Control Unit (DCU)	No	No	Yes
Parallel Data Interface	No	No	Yes
Stepper Motor Controller (SMC)	6 motors		
Stepper Stall Detect (SSD)	Yes		
Sound Generation Logic (SGL)	Yes		
LCD driver	40 × 4, 38 × 6[1]		
32 KHz slow external crystal oscillator	Yes		

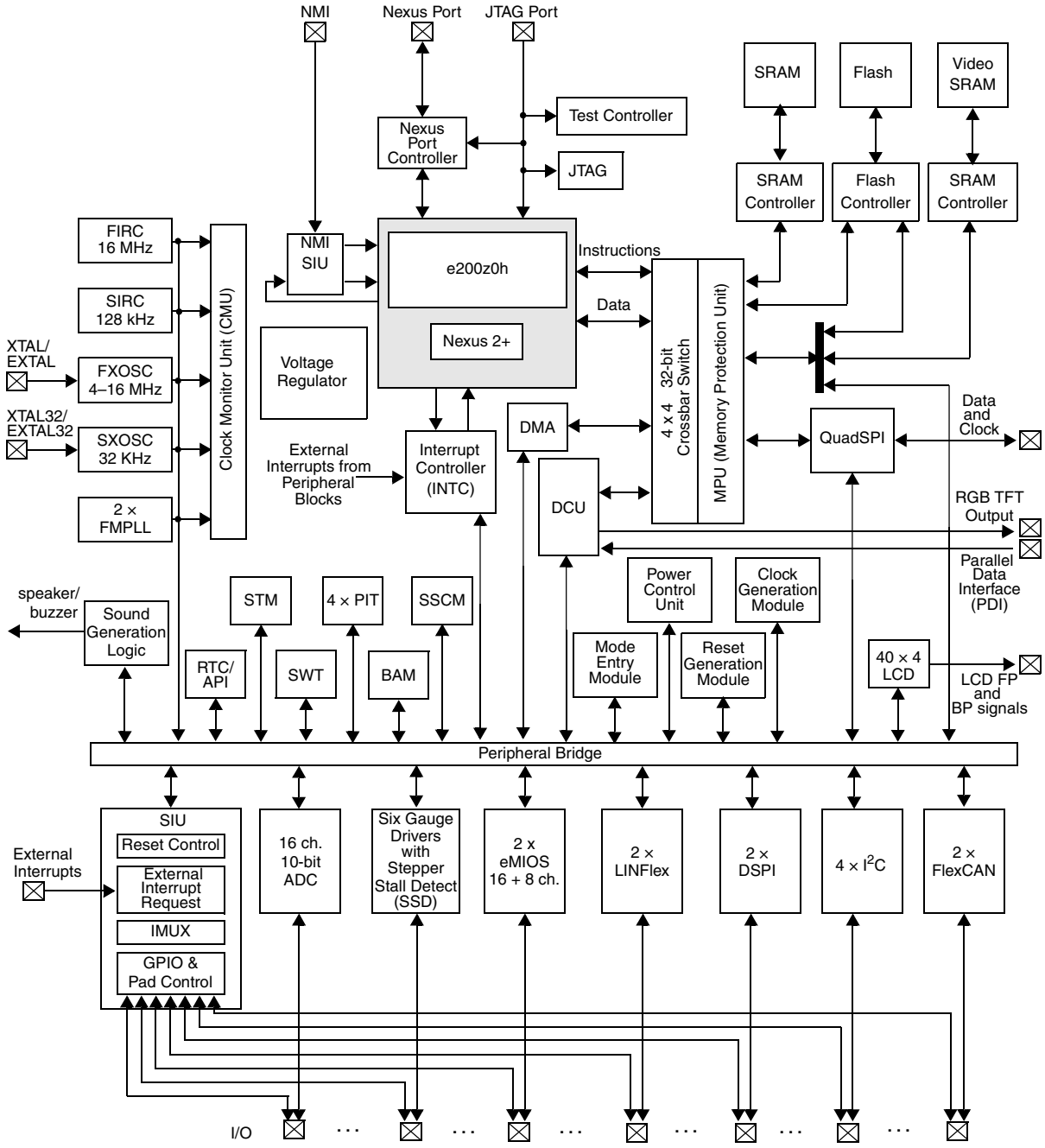


Figure 1. MPC5606S series block diagram

Table 2 summarizes the operating modes of MPC5606S devices.

Table 2. Operating mode summary[1]

	Operating modes:	Run	Halt	Stop	Standby		POR
SoC features	Core	On	CG	CG	Off	Off	—
	Peripherals	OP	OP	CG	Off[2]	Off	—
	Flash memory	OP	OP	CG	Off	Off	—
	SRAM	On	On	CG	CG[3]	8 KB[4]	—
	Graphics RAM	On	On	CG	Off	Off	—
Clock sources	Main PLL	OP	OP	CG	Off	Off	—
	Auxiliary PLL	OP	OP	CG	Off	Off	—
	16 MHz IRC	On	On	OP	OP	OP	—
	FXOSC	OP	OP	OP	OP	OP	—
	128 kHz IRC	On	On	On	On	On	—
	32 KHz XOSC	OP	OP	OP	OP	OP	—
Periodic wakeup		—	OP	OP	OP	OP	—
Wakeup input		—	OP	OP	OP	OP	—
VREG mode		FP	FP	LP	LP	LP	—
Wakeup times[5]	VREG startup	—	—	50 µs	250 µs	250 µs	250 µs[6]
	IRC wakeup	—	—	4 µs	4 µs	8 µs	8 µs
	Flash memory recovery	—	—	20 µs	100 µs	100 µs	100 µs
	OSC stabilization	—	—	1 ms	1 ms	1 ms	1 ms
	PLL lock	—	—	200 µs	200 µs	200 µs	200 µs
	S/W reconfig	—	—	—	Var	Var	—
	Mode switch over	—	200.69 µs	24 µs	28 µs	28 µs	BAM

1 Table Key:
On—Powered and clocked
OP—Optionally configurable to be enabled or disabled (clock gated)
CG—Clock Gated, Powered but clock stopped
Off—Powered off and clock gated
FP—VREG Full Performance mode
LP—VREG low-power mode, reduced output capability of VREG but lower power consumption
Var—Variable duration, based on the required reconfiguration and execution clock speed
BAM—Boot Assist Module Software and Hardware used for device startup and configuration

2 The LCD can optionally be kept running while the device is in Standby mode.

3 All of the RAM content is retained, but not accessible in Standby mode.

4 8 KB of the RAM content is retained, but not accessible in Standby mode.

- Two-wire bi-directional serial bus for on-board communications
- Compatibility with I^2C bus standard
- Multimaster operation
- Software-programmable for one of 256 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

1.5.6 Interrupt Controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high-priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software-configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource cannot preempt each other.

Multiple processors can assert interrupt requests to each other through software-settable interrupt requests. These same software-settable interrupt requests also can be used to break the work involved in servicing an interrupt request into a high-priority portion and a low-priority portion. The high-priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software-settable interrupt request to finish the servicing in a lower priority ISR. Therefore these software-settable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS. The INTC provides the following features:

- Unique 9-bit vector for each of the possible 128 separate interrupt sources
- Eight software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority
  - Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources
- External NMI directly accessing the main core critical interrupt mechanism
- 32 external interrupts

1.5.7 QuadSPI serial flash controller

The QuadSPI module enables use of external serial flash memories supporting single, dual, and quad modes of operation. It features the following:

- Memory mapping of external serial flash memory
- Automatic serial flash read command generation by CPU, DMA, or DCU read access on AHB bus
- Supports single, dual, and quad serial flash read commands
- Flexible buffering scheme to maximize read bandwidth of serial flash

- Legacy mode allowing QuadSPI to be used as a standard DSPI (no DSI or CSI mode)

1.5.8 System Integration Unit (SIU)

The SIU controls MCU, pad configuration, external interrupt, general purpose I/O (GPIO) and internal peripheral multiplexing.

The GPIO features the following:

- As many as four levels of internal pin multiplexing, allowing exceptional flexibility in the allocation of device functions for each package
- Centralized general purpose input output (GPIO) control of as many as 132 input/output pins (package dependent)
- All GPIO pins can be independently configured to support pullup, pulldown, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit-wide ports
- All peripheral pins can be alternatively configured as both general purpose input or output pins, except ADC channels which support alternative configuration as general purpose inputs
- Direct readback of the pin value supported on all digital output pins through the SIU
- Configurable digital input filter that can be applied to as many as 14 general purpose input pins for noise elimination on external interrupts
- Register configuration protected against change with soft lock for temporary guard or hard lock to prevent modification until next reset

1.5.9 Flash memory

The MPC5606S microcontroller has the following flash memory features:

- As nuch as 1 MB of burst flash memory
  - Typical flash memory access time: 0 wait state for buffer hits, 2 wait states for page buffer miss at 64 MHz
  - Two 4×128-bit page buffers with programmable prefetch control
    - One set of page buffers can be allocated for code-only, fixed partitions of code and data, all available for any access
    - One set of page buffers allocated to Display Controller Unit and the eDMA
  - 64-bit ECC with single-bit correction, double-bit detection for data integrity
  - 64 KB data flash memory — separate 4×16 KB flash block for EEPROM emulation with prefetch buffer and 128-bit data access port
- Small block flash memory arrangement to support features such as boot block, operating system block
- Hardware-managed flash memory writes, erases and verify sequences
- Censorship protection scheme to prevent flash memory content visibility
- Separate dedicated 64 KB data flash memory for EEPROM emulation
  - Four erase sectors each containing 16 KB of memory
  - Offers Read-While-Write functionality from main program space
  - Same data retention and program erase specification as main program flash memory array

1.5.10 SRAM

The MPC5606S microcontrollers have as much as 48 KB general-purpose on-chip SRAM with the following features:

- Typical SRAM access time: 0 wait-state for reads and 32-bit writes; 1 wait state for 8- and 16-bit writes if back to back with a read to same memory block
- 32-bit ECC with single-bit correction, double bit detection for data integrity
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- User transparent ECC encoding and decoding for byte, half word, and word accesses

- Edge-aligned output pulse width modulation
  - Programmable pulse period and duty cycle
  - Supports 0% and 100% duty cycle
  - Shared or independent time bases
- Programmable phase shift between channels
- Selectable combination of pairs of eMIOS outputs to support sound generation
- DMA transfer support
- Selectable clock source from the primary FMPLL, auxiliary FMPLL, external 4–16 MHz oscillator, or the 16 MHz internal RC oscillator.

The channel configuration options for the 16-channel eMIOS module are summarized in Table 3.

Table 3. 16-Channel eMIOS module channel configuration

Channel mode	Channel number				
	8 IC/OC Counter	9–15 IC/OC	16 PWM Counter	17–22 PWM	23 PWM Counter
General Purpose Input/Output	X	X	X	X	X
Single Action Input Capture	X	X	X	X	X
Single Action Output Compare	X	X	X	X	X
Modulus Counter Buffered[1]	X		X		X
Output Pulse Width and Frequency Modulation Buffered			X	X	X
Output Pulse Width Modulation Buffered			X	X	X

[1] Modulus up and down counters to support driving local and global counter buses.

The channel configuration options for the eight-channel eMIOS module are summarized in Table 4.

Table 4. Eight-channel eMIOS module channel configuration

Channel mode	Channel number		
	16 PWM Counter	17–22 PWM	23 PWM Counter
General Purpose Input/Output	X	X	X
Single Action Input Capture	X	X	X
Single Action Output Compare	X	X	X
Modulus Counter Buffered[1]	X		X
Output Pulse Width and Frequency Modulation Buffered	X	X	X
Output Pulse Width Modulation Buffered	X	X	X

[1] Modulus up and down counters to support driving local and global counter buses.

1.5.15 Analog-to-Digital Converter (ADC)

The ADC features the following:

- 10-bit A/D resolution
- 0 to 5 V common mode conversion range
- Supports conversions speeds of up to 1 µs
- 16 internal and eight external channel support
- As many as 16 single-ended input channels
  - All channels configured to have alternate function as general purpose input/output pins
    - 10-bit ±3 counts accuracy (TUE)
- External multiplexer support to increase as many as 23 channels
  - Automatic 1 × 8 multiplexer control
  - External multiplexer connected to a dedicated input channel
  - Shared register between the eight external channels
- Result register available for every non-multiplexed channel
- Configurable left- or right-aligned result format
- Supports for one-shot, scan, and injection conversion modes
- Injection mode status bit implemented on adjacent 16-bit register for each result
  - Supports access to result and injection status with single 32-bit read
- Independent enabling of function for channels:
  - Offset refresh
- Conversion Triggering support
  - Internal conversion triggering from periodic interrupt timer (PIT)
- Four configurable analog comparator channels offering range comparison with triggered alarm
  - Greater than
  - Less than
  - Out of range
- All unused analog inputs can be used as general purpose input and output pins
- Power Down mode
- Optional support for DMA transfer of results

1.5.16 Deserial Serial Peripheral Interface (DSPI)

The deserial serial peripheral interface (DSPI) modules provide a synchronous serial interface for communication between the MPC5606S MCU and external devices.

The DSPI features the following:

- As many as two DSPI modules
- Full-duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- As many as six chip select lines available, depending on package and pin multiplexing, enable 64 external devices to be selected using external muxing from a single DSPI

- Configurable break duration as long as 36-bit times
- Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
- Diagnostic features
  - — Loopback
  - — Self-test
  - — LIN bus stuck dominant detection
- Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features
  - — Autonomous LIN header handling
  - — Autonomous LIN response handling
  - — Discarding of irrelevant LIN responses using as many as 16 ID filters
- UART mode
  - — Full-duplex operation
  - — Standard non-return-to-zero (NRZ) mark/space format
  - — Data buffers with 4-byte receive, 4-byte transmit
  - — Configurable word length (8-bit or 9-bit words)
  - — Error detection and flagging
    - – Parity, noise, and framing errors
  - — Interrupt driven operation with four interrupt sources
  - — Separate transmitter and receiver CPU interrupt sources
  - — 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - — Two receiver wakeup methods

1.5.19 System clocks and clock generation modules

The system clock on the MPC5606S can be derived from an external oscillator, an on-chip FMPLL, or the internal 16 MHz oscillator.

- Source system clock frequency can be changed via an on-chip programmable clock divider (÷1 to ÷32)
- Additional programmable peripheral bus clock divider ratio (÷1 to ÷16)
- Two on-chip FMPLLs—the primary module and an auxiliary module
  - — Each FMPLL features:
    - – Input clock frequency from 4 MHz to 16 MHz
    - – Lock detect circuitry continuously monitoring lock status
    - – Loss Of Clock (LOC) detection for reference and feedback clocks
    - – On-chip loop filter (for improved electromagnetic interference performance and reduction of number of external components required)
    - – Support for frequency ramping from PLL
  - — The primary FMPLL module is for use as a system clock source; the auxiliary FMPLL is available for use as an alternate, modulated or non-modulated clock source to eMIOS modules and as alternate clock to the DCU for pixel clock generation
- The main oscillator provides the following features:
  - — Input frequency range 4–16 MHz
  - — Square-wave input mode
  - — Oscillator input mode 3.3 V (5.0 V)
  - — Automatic level control
  - — PLL reference

  - Static debug
  - Watchpoint messaging
  - Ownership trace messaging
  - Program trace messaging
  - Real time read/write of any internally memory-mapped resources through JTAG pins
  - Overrun control, which selects whether to stall before Nexus overruns or else keep executing and allow overwrite of information
  - Watchpoint triggering, watchpoint triggers program tracing
- Configured via the IEEE 1149.1 (JTAG) port
- Nexus Auxiliary port supported on the 176 LQFP and 208-pin BGA package FOR DEVELOPMENT ONLY
  - Narrow Auxiliary Nexus port supporting support trace, with two MDO pins
  - Wide Auxiliary Nexus port supporting higher bandwidth trace, with four MDO pins

2 Pinout and signal descriptions

2.1 144 LQFP package pinouts

This section shows the pinouts for the 144-pin LQFP packages.

CAUTION

Any pins labeled “NC” must not be connected to any external circuit.

Table 8. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number		
									144 LQFP	176 LQFP	208 MAPBGA
PA[8]	PCR[8]	Option 0 Option 1 Option 2 Option 3	GPIO[8] DCU_G0 eMIOSB[23] SCL_2	FP15	SIUL DCU PWM/Timer I^2C_2	I/O	M1	None, None	143	175	F1
PA[9]	PCR[9]	Option 0 Option 1 Option 2 Option 3	GPIO[9] DCU_G1 eMIOSB[18] SDA_2	FP14	SIUL DCU PWM/Timer I^2C_2	I/O	M1	None, None	144	176	F2
PA[10]	PCR[10]	Option 0 Option 1 Option 2 Option 3	GPIO[10] DCU_G2 eMIOSB[20] —	FP13	SIUL DCU PWM/Timer —	I/O	M1	None, None	1	1	G1
PA[11]	PCR[11]	Option 0 Option 1 Option 2 Option 3	GPIO[11] DCU_G3 eMIOSA[13] —	FP12	SIUL DCU PWM/Timer —	I/O	M1	None, None	2	2	G2
PA[12]	PCR[12]	Option 0 Option 1 Option 2 Option 3	GPIO[12] DCU_G4 eMIOSA[12] —	FP11	SIUL DCU PWM/Timer —	I/O	M1	None, None	3	3	H1
PA[13]	PCR[13]	Option 0 Option 1 Option 2 Option 3	GPIO[13] DCU_G5 eMIOSA[11] —	FP10	SIUL DCU PWM/Timer —	I/O	M1	None, None	4	4	H2
PA[14]	PCR[14]	Option 0 Option 1 Option 2 Option 3	GPIO[14] DCU_G6 eMIOSA[10] —	FP9	SIUL DCU PWM/Timer —	I/O	M2	None, None	5	5	J2
PA[15]	PCR[15]	Option 0 Option 1 Option 2 Option 3	GPIO[15] DCU_G7 eMIOSA[9] —	FP8	SIUL DCU PWM/Timer —	I/O	M1	None, None	6	6	H3

3 Electrical characteristics

3.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by internal pull up and pull down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 11 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 11. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 NVUSRO register

Portions of the device configuration, such as high voltage supply, oscillator margin, and watchdog enable/disable after reset are controlled via bit values in the Nonvolatile User Options (NVUSRO) register. For a detailed description of the NVUSRO register, please see the chip reference manual.

3.3.1 NVUSRO[PAD3V5V] field description

Table 12 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 12. PAD3V5V field description[1]

Value[2]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1 See the device reference manual for more information on the NVUSRO register.
2 Default manufacturing value before Flash initialization is '1' (3.3 V)

The DC electrical characteristics are dependent on the PAD3V5V bit value.

3.3.2 NVUSRO[OSCILLATOR_MARGIN] field description

Table 12 shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 13. OSCILLATOR_MARGIN field description[1]

Value[2]	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

1 See the device reference manual for more information on the NVUSRO register.
2 Default manufacturing value before Flash initialization is '1'

The 4–16 MHz fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value.

3.4 Absolute maximum ratings

Table 14. Absolute maximum ratings

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{DDA}	SR	C	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SSA})	—	–0.3	6.0	V
V_{SSA}	SR	C	Voltage on VSSA (ADC reference) pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DDPLL}	CC	C	Voltage on VDDPLL (1.2 V PLL supply) pin with respect to ground (V_{SSPLL})	—	–0.1	1.4	V
V_{SSPLL}	SR	C	Voltage on VSSPLL pin with respect to V_{SS12}	—	V_{SS12} – 0.1	V_{SS12} + 0.1	V
V_{DDR}	SR	C	Voltage on VDDR pin (regulator supply) with respect to ground (V_{SSR})	—	–0.3	6.0	V
V_{SSR}	SR	C	Voltage on VSSR (regulator ground) pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD12}	CC	C	Voltage on VDD12 pin with respect to ground (V_{SS12})	—	–0.1	1.4	V
V_{SS12}	CC	C	Voltage on VSS12 pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DDE_A}[1]	SR	C	Voltage on VDDE_A (I/O supply) pin with respect to ground (V_{SSE_A})	—	–0.3	6.0	V

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using Equation 4:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 4}$$

where:

T_T = thermocouple temperature on top of the package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
805 East Middlefield Rd.
Mountain View, CA 94043 USA
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

3.6 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

3.6.1 EMC requirements on board

The following practices help minimize noise in applications.

- Place a 100 nF capacitor between each of the V_{DD12}/V_{SS12} supply pairs and also between the V_{DDPLL}/V_{SSPLL} pair. The voltage regulator also requires stability capacitors for these supply pairs.
- Place a 10 µF capacitor on VDDR.
- Isolate VDDR with ballast emitter to avoid voltage droop during STANDBY mode exit.
- Enable pad slew rate only as necessary to eliminate I/O noise:
  - Enabling slew rate for SMD pads will reduce noise on motors.
  - Disabling slew rate for non-SMD pads will reduce noise on non-SMD I/Os.
- Enable PLL modulation (± 2%) for system clock.
- Place decoupling capacitors for all HV supplies close to the pins.

Table 38. SSD electrical characteristics (continued)

Symbol		C	Parameter	Value[1]			Unit
				Min	Typ	Max	
SSD_{OFFSET}	CC	C	SSD offset (unipolar, N_{sample} = 256)	–9	—	9	counts
			SSD offset (bipolar, N_{sample} = 256)	–8	—	8	
			SSD offset (bipolar with offset cancellation, N_{sample} = 256)	–5	—	5	
f_{SSDSMP}	CC	D	SSD cmpout sample rate	0.5	—	2.0	MHz

1 Vdd = 5.0V ±10%, Tj = –40 to +150 °C.

3.9.2 Accumulator values

Equation 5 describes the accumulator value in unipolar configuration. The voltage V_{in} is applied between the integrator input and V_{DDM}. The internal generated reference voltage is not connected. The accumulator value is a function of V_{DDM}, the number of samples (Nsample) taken and the SSD constant (SSDconst). The SSD constant and offset (SSDconst, SSDoffset) vary with temperature and process.

$$ACCval = \frac{V_{in} - (VDDM)/2}{VDDM \cdot SSDconst} \cdot Nsample + SSDoffset$$

Eqn. 5

Equation 6 describes the accumulator value in bipolar configuration. The voltage V_{in} is applied between the integrator input and the reference output. The accumulator value depends on the same parameters as in the unipolar case but the inaccuracy of the voltage reference (Vvref) is compensated.

$$ACCval = \frac{V_{in}}{VDDM \cdot SSDconst} \cdot Nsample + SSDoffset$$

Eqn. 6

3.10 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

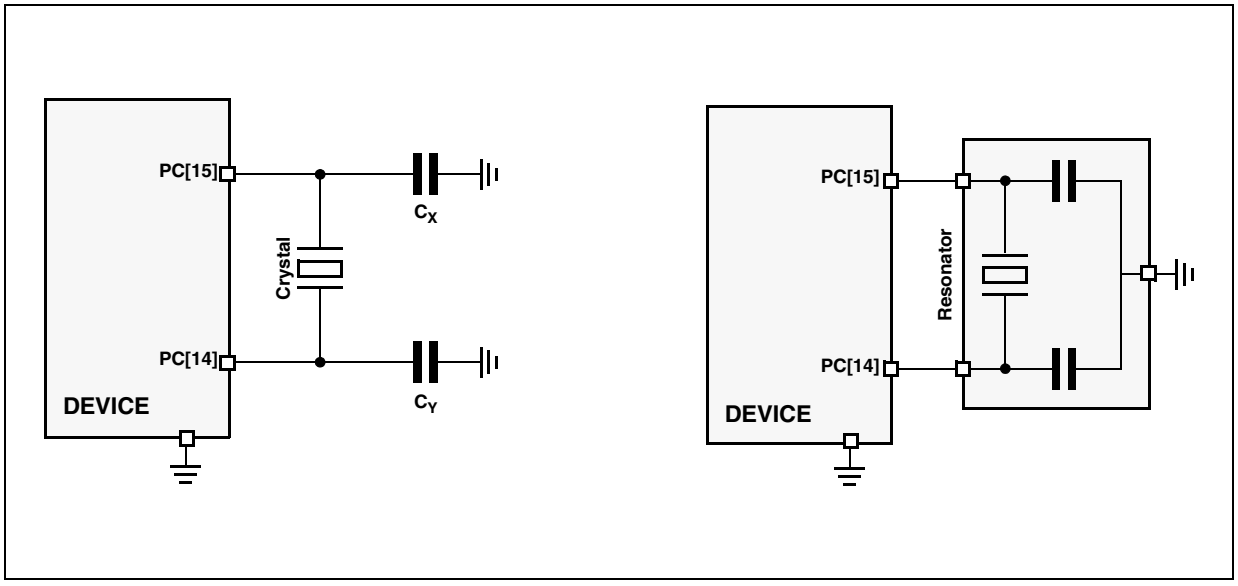


Figure 19. Crystal oscillator and resonator connection scheme

NOTE

PC[14]/PC[15] must not be directly used to drive external circuits.

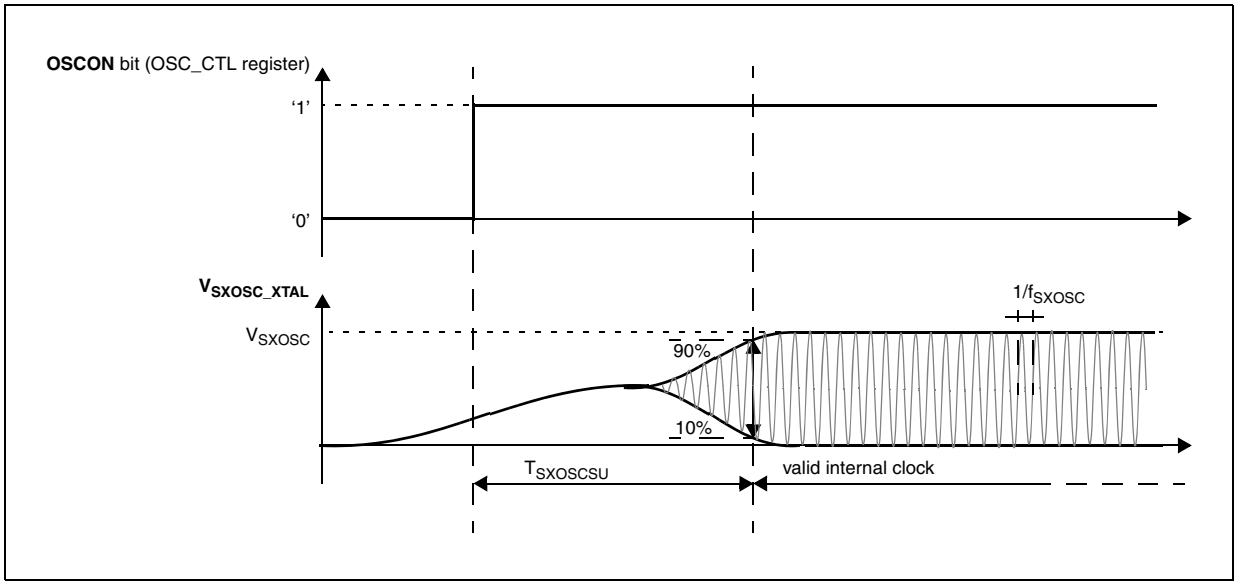


Figure 20. Slow external crystal oscillator (32 KHz) timing

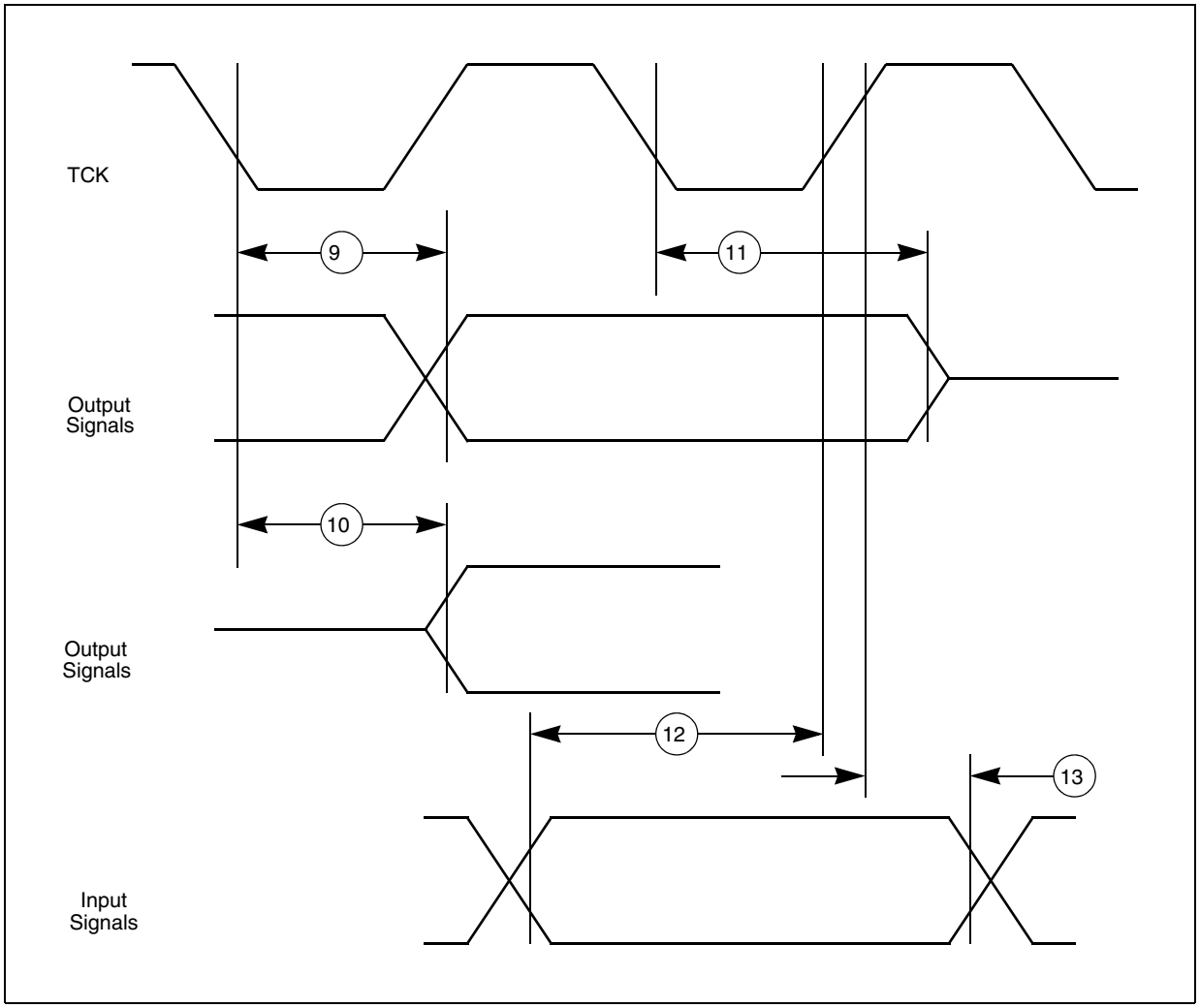
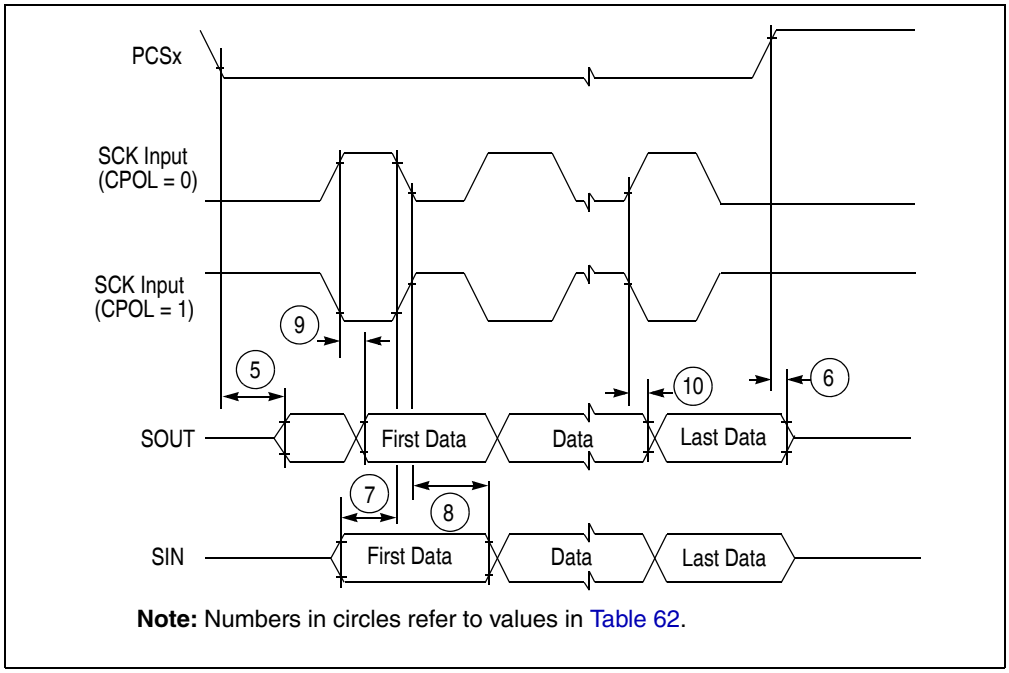


Figure 29. JTAG boundary scan timing

3.20.2 Nexus debug interface

Table 56. Nexus debug port timing[1]

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	t_{MCYC}	CC	D	MCKO Cycle Time	22	—	ns
2	Δ_{MDC}	CC	D	MCKO Duty Cycle	40	60	%
3	t_{MDOV}	CC	D	MCKO Low to MDO Data Valid[2]	–2	14	ns
4	t_{MSEOV}	CC	D	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[2]	–2	14	ns
5	t_{EVTOV}	CC	D	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[2]	–2	14	ns
6	t_{EVTIPW}	CC	D	$\overline{\text{EVTI}}$ Pulse Width	4	—	t_{TCYC}
7	t_{EVTOPW}	CC	D	$\overline{\text{EVTO}}$ Pulse Width	1	—	t_{MCYC}



Note: Numbers in circles refer to values in Table 62.

Figure 45. DSPI modified transfer format timing — slave, CPHA = 1

3.20.8 I^2C timing

Table 63. I^2C Input Timing Specifications — SCL and SDA

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	—	CC	D	Start condition hold time	2	—	IP-Bus Cycle[1]
2	—	CC	D	Clock low time	8	—	IP-Bus Cycle[1]
4	—	CC	D	Data hold time	0.0	—	ns
6	—	CC	D	Clock high time	4	—	IP-Bus Cycle[1]
7	—	CC	D	Data setup time	0.0	—	ns
8	—	CC	D	Start condition setup time (for repeated start condition only)	2	—	IP-Bus Cycle[1]
9	—	CC	D	Stop condition setup time	2	—	IP-Bus Cycle[1]

[1] Inter Peripheral Clock is the clock at which the I^2C peripheral is working in the device.

6 Revision history

Table 66. Document revision history

Revision	Date	Substantive changes
1	10-2008	Initial release.
2	18 Aug 2009	Editorial changes and improvements. Harmonized oscillator naming throughout document Features: Updated description of ADC channels Table 2: Changed max number of GPIOs from 132 to 133 for LQFP176 Table 3: Corrected “Peripheral interrupt timer (PIT)” to “Periodic interrupt timer (PIT)” Figure 2: – Added GPIOs to pin function names – Changed function of pin 32: was NC—is VREG_BYPASS – Pin 55: Changed XTAL32 to OSC32K_XTAL – Pin 56: Changed EXTAL32 to OSC32K_EXTAL Figure 5: – Added GPIOs to pin function names – Changed function of pin 32: was NC—is VREG_BYPASS – Pin 71: Changed XTAL32 to OSC32K_XTAL – Pin 72: Changed EXTAL32 to OSC32K_EXTAL Table 6: – Removed pins EXTAL32, XTAL32 and NMI – Updated VRC_CTL I/O direction and pad type Table 7: – Replaced “A” with “I” in pad type column – Modified table footnote 3 to replace pad type “A” definition with pad type “I” definition Table 8: Moved MA[0:2] to follow AN[0:15] Added Section 3.2, “Parameter classification and added classification tags to electrical characteristics tables where appropriate Added Section 3.3, “NVUSRO register Table 14: Removed ESD_{HBM} Table 17: Merged 144- and 176-pin LQFP characteristics into single table Added Section 3.6, “Electromagnetic compatibility (EMC) characteristics Table 26: Removed “T_A = 25 °C, after trimming” from conditions for V_{PORH}, V_{LVDH3V} and V_{LVDH5V} Table 27: – Changed T_A = –40 to 125 °C to T_A = –40 to 105 °C in note 1 – Added STANDBY1 and STANDBY2 mode current characteristics Figure 14: Updated to reference GPDI register and values for bit PDI Section 3.8.1, “I/O pad types: Corrected “four main I/O pad types” to read “three main I/O pad types” Section 3.8.3, “I/O output DC characteristics: Replaced ipp_hve with PAD3V5V

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: MPC5606S
Rev. 8
11/2011