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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, QSPI, SCI, SPI
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	136
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5606sf2vlu6r

Table 2 summarizes the operating modes of MPC5606S devices.

Table 2. Operating mode summary[1]

	Operating modes:	Run	Halt	Stop	Standby		POR
SoC features	Core	On	CG	CG	Off	Off	—
	Peripherals	OP	OP	CG	Off[2]	Off	—
	Flash memory	OP	OP	CG	Off	Off	—
	SRAM	On	On	CG	CG[3]	8 KB[4]	—
	Graphics RAM	On	On	CG	Off	Off	—
Clock sources	Main PLL	OP	OP	CG	Off	Off	—
	Auxiliary PLL	OP	OP	CG	Off	Off	—
	16 MHz IRC	On	On	OP	OP	OP	—
	FXOSC	OP	OP	OP	OP	OP	—
	128 kHz IRC	On	On	On	On	On	—
	32 KHz XOSC	OP	OP	OP	OP	OP	—
Periodic wakeup		—	OP	OP	OP	OP	—
Wakeup input		—	OP	OP	OP	OP	—
VREG mode		FP	FP	LP	LP	LP	—
Wakeup times[5]	VREG startup	—	—	50 µs	250 µs	250 µs	250 µs[6]
	IRC wakeup	—	—	4 µs	4 µs	8 µs	8 µs
	Flash memory recovery	—	—	20 µs	100 µs	100 µs	100 µs
	OSC stabilization	—	—	1 ms	1 ms	1 ms	1 ms
	PLL lock	—	—	200 µs	200 µs	200 µs	200 µs
	S/W reconfig	—	—	—	Var	Var	—
	Mode switch over	—	200.69 µs	24 µs	28 µs	28 µs	BAM

1 Table Key:
On—Powered and clocked
OP—Optionally configurable to be enabled or disabled (clock gated)
CG—Clock Gated, Powered but clock stopped
Off—Powered off and clock gated
FP—VREG Full Performance mode
LP—VREG low-power mode, reduced output capability of VREG but lower power consumption
Var—Variable duration, based on the required reconfiguration and execution clock speed
BAM—Boot Assist Module Software and Hardware used for device startup and configuration

2 The LCD can optionally be kept running while the device is in Standby mode.

3 All of the RAM content is retained, but not accessible in Standby mode.

4 8 KB of the RAM content is retained, but not accessible in Standby mode.

- Separate internal power domain applied to full SRAM block, 8 KB SRAM block during Standby modes to retain contents during low-power mode.

1.5.11 On-chip graphics SRAM

The MPC5606S microcontroller has 160 KB on-chip graphics SRAM with the following features:

- Usable as general purpose SRAM
- Typical SRAM access time: 0 wait-state for reads and 32-bit writes
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory

1.5.12 Memory Protection Unit (MPU)

The MPU features the following:

- 12 region descriptors for per-master protection
- Start and end address defined with 32-byte granularity
- Overlapping regions supported
- Protection attributes can optionally include process ID
- Protection offered for three concurrent read ports
- Read and write attributes for all masters
- Execute and supervisor/user mode attributes for processor masters

1.5.13 Boot Assist Module (BAM)

The BAM is a block of read-only memory that is programmed once by Freescale. The BAM program is executed every time the MCU is started up or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (a program is downloaded into RAM via FlexCAN or LINFlex and then executed)
- Booting from external memory

Additionally the BAM:

- Enables and manages the transition of the MCU from reset to user code execution
- Configures device for serial bootload
- Enables multiple bootcode starting locations out of reset through implementation of search for valid Reset Configuration Halfword

1.5.14 Enhanced Modular Input/Output System (eMIOS)

MPC5606S microcontrollers have two eMIOS modules—one with 16 channels and one with eight—with input/output channels supporting a range of 16-bit input capture, output compare, and Pulse Width Modulation functions.

The modules are configurable and can implement 8-channel, 16-bit input capture/output compare or 16-channel, 16-bit output pulse width modulation/input compare/output compare. As many as five additional channels are configurable as modulus counters.

eMIOS other features include:

- Selectable clock source from main FMPLL, auxiliary FMPLL, external 4–16 MHz oscillator or 16 MHz internal RC oscillator
- Timed I/O channels with 16-bit counter resolution
- Buffered updates
- Support for shifted PWM outputs to minimize occurrence of concurrent edges

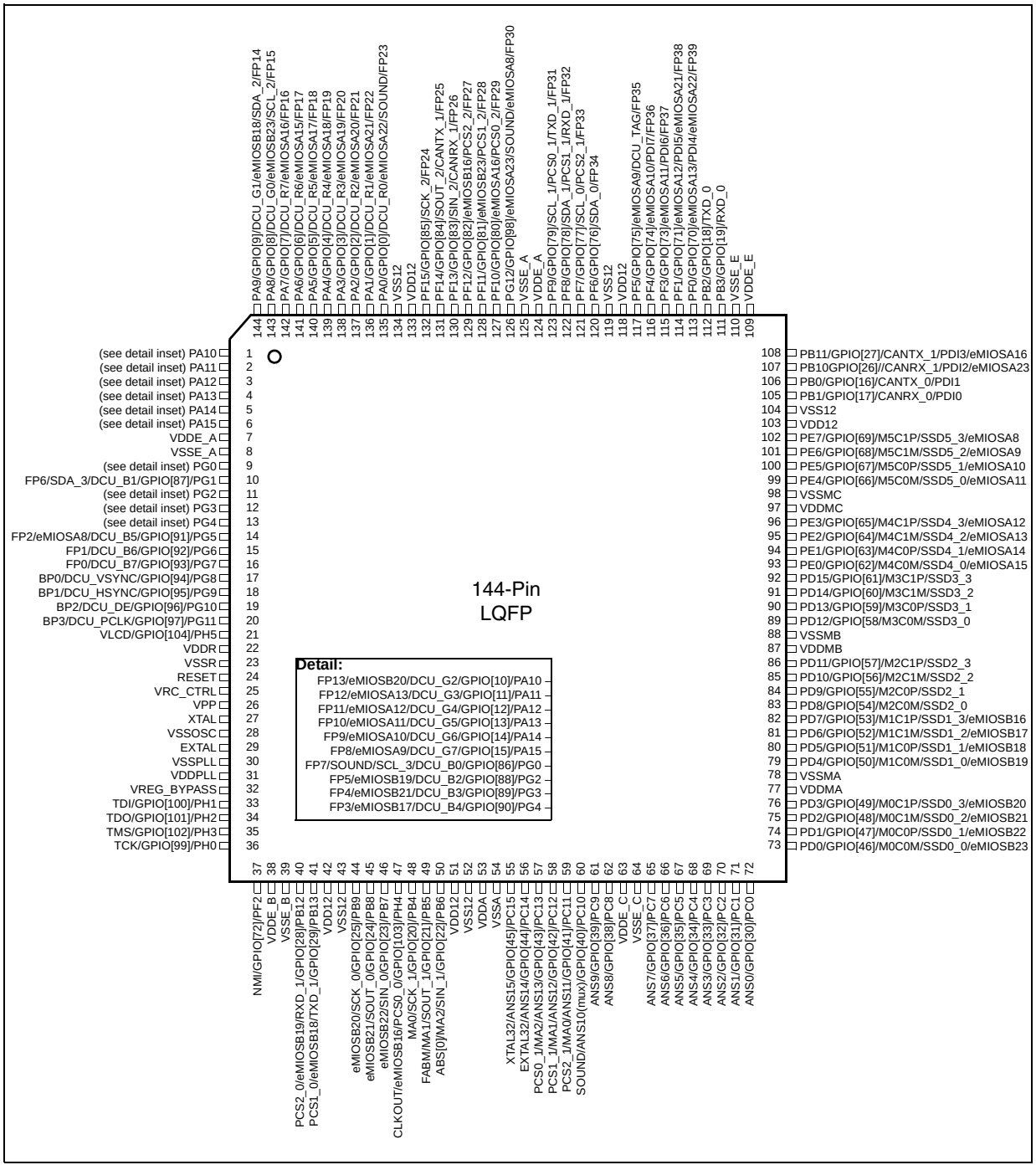


Figure 2. 144-pin LQFP pinout for MPC5606S

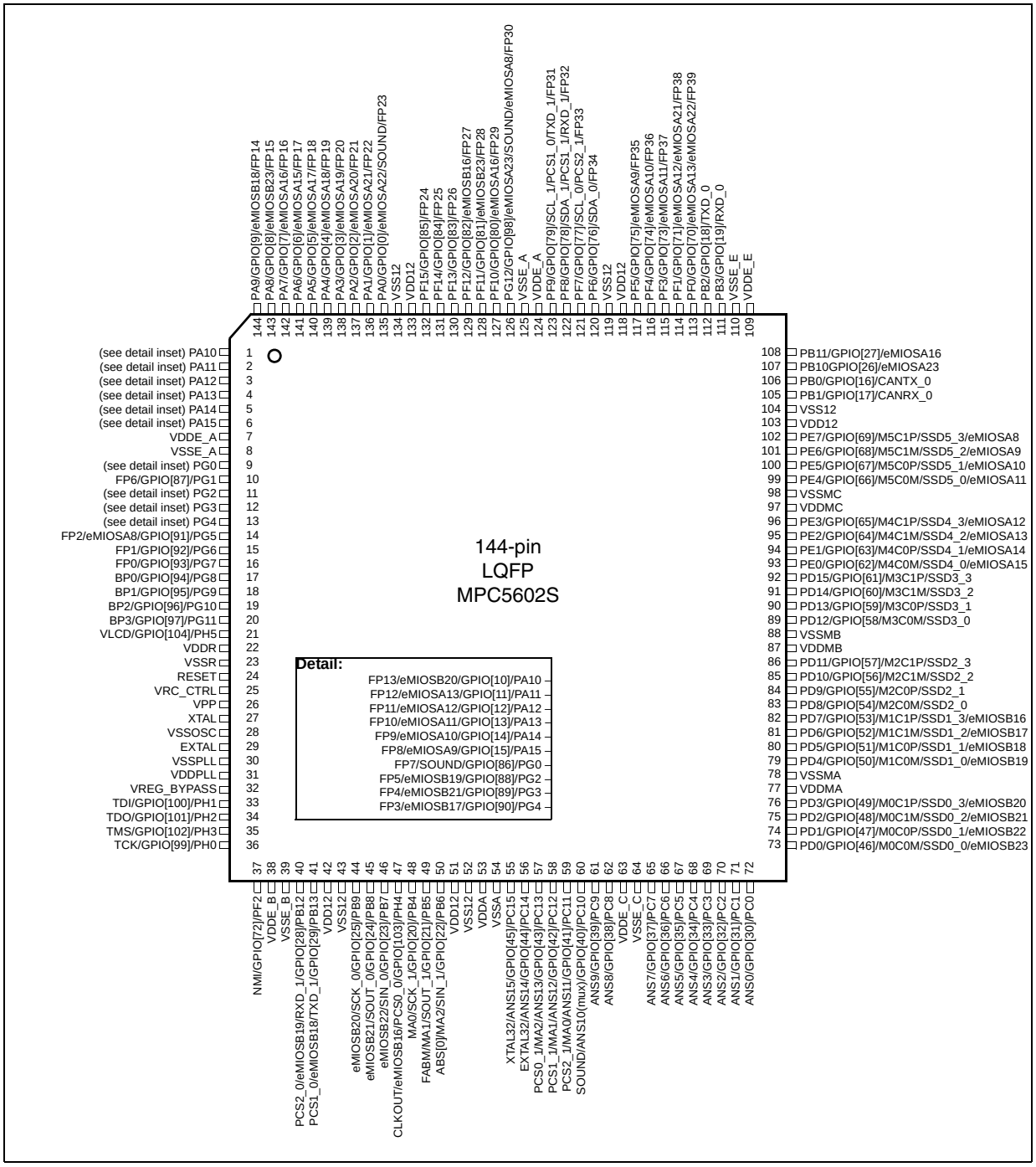


Figure 4. 144-pin LQFPpinout for MPC5602S

2.2 176 LQFP package pinout

Figure 5 shows the pinout for the 176-pin LQFP package.

CAUTION

Any pins labeled “NC” must not be connected to any external circuit.

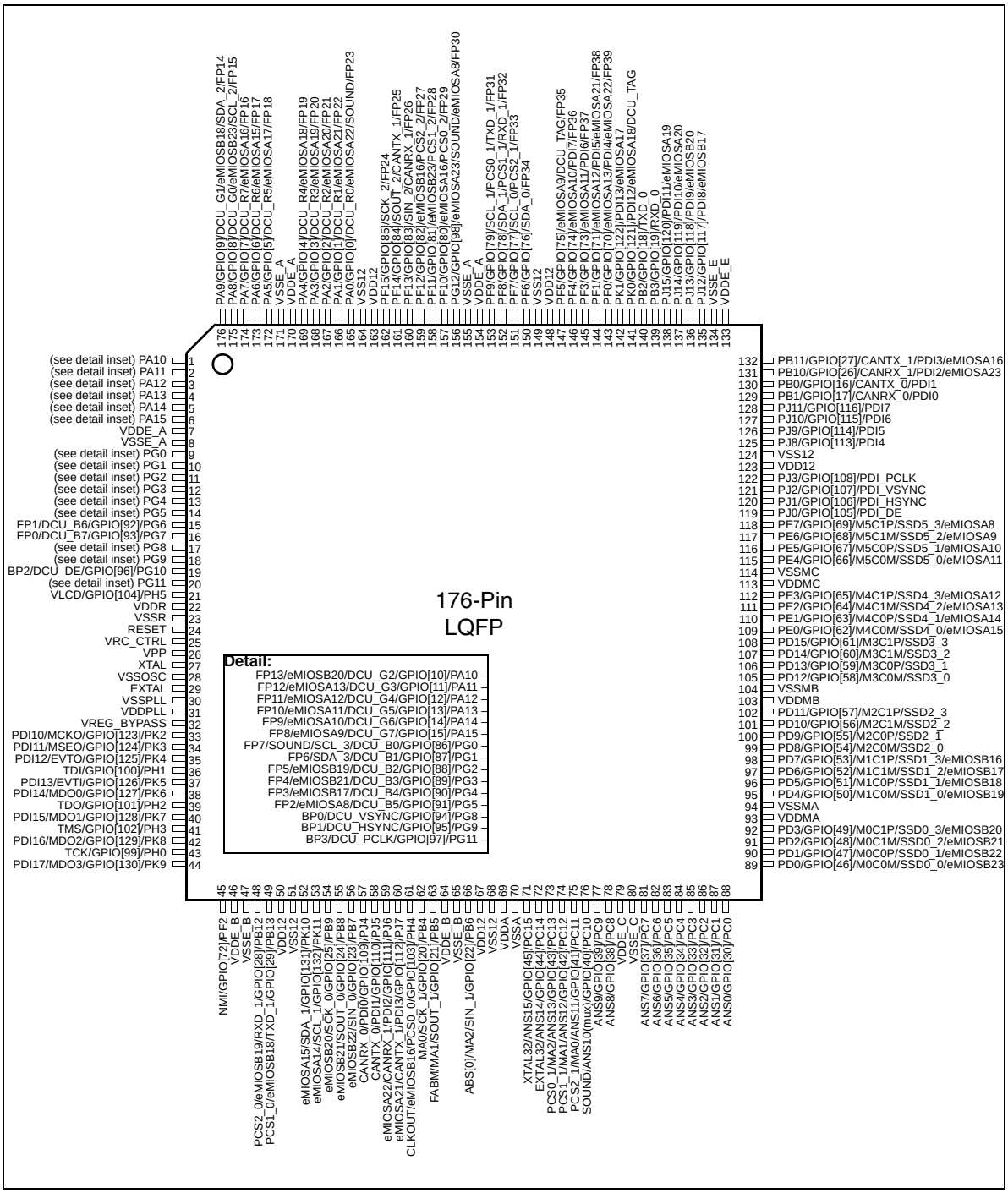


Figure 5. 176-pin LQFP Pinout

Table 5. Voltage supply pin descriptions

Supply Pin	Function	Pin number	
		144 LQFP	176 LQFP
VDD12[1]	1.2 V core supply	42, 51, 103, 118, 133	50, 67, 123, 148, 163
VDDA	3.3 V/5 V ADC supply source	53	69
VDDE_A	3.3 V/5 V I/O supply	7, 124	7, 154, 170
VDDE_B	3.3 V/5 V I/O supply	38	46, 64
VDDE_C	3.3 V/5 V I/O supply	63	79
VDDE_E	3.3 V/5 V I/O supply	109	133
VDDMA[2]	Motor pads 5 V supply	77	93
VDDMB[2]	Motor pads 5 V supply	87	103
VDDMC[2]	Motor pads 5 V supply	97	113
VDDPLL	1.2 V PLL supply	31	31
VDDR	VREG reg supply	22	22
VPP[3]	9 V–12 V flash test analog write signal	26	26
VSS	Digital ground	8, 23, 39, 43, 52, 64, 104, 110, 119, 125, 134	8, 23, 47, 51, 68, 80, 124, 134, 149, 155, 164, 65, 171
VSSA	ADC ground	54	70
VSSMA	Stepper motor ground	78	94
VSSMB	Stepper motor ground	88	104
VSSMC	Stepper motor ground	98	114
VSSOSC	MHz oscillator ground	28	28
VSSPLL	PLL ground	30	30

1 Decoupling capacitors must be connected between these pins and the nearest V_{SS12} pin.

2 All stepper motor supplies need to be at same level (3.3 V or 5 V).

3 This signal needs to be connected to ground during normal operation.

2.6 Pad types

The pads available for system pins and functional port pins are described in:

- The port pin summary table
- The pad type descriptions
- The description of the pad configuration registers in Chapter 37, System Integration Unit Lite (SIUL)
- The device data sheet

2.7 System pins

The system pins are listed in Table 6.

Table 8. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number		
									144 LQFP	176 LQFP	208 MAPBGA
PH[2][7]	PCR[101]	Option 0 Option 1 Option 2 Option 3	GPIO[101] TDO — —	—	SIUL JTAG — —	I/O	M1	Output, None	34	39	N3
PH[3][7]	PCR[102]	Option 0 Option 1 Option 2 Option 3	GPIO[102] TMS — —	—	SIUL JTAG — —	I/O	S	Input, Pullup	35	41	M3
PH[4]	PCR[103]	Option 0 Option 1 Option 2 Option 3	GPIO[103] PCS0_0 eMIOSB[16] CLKOUT	—	SIUL DSPI_0 PWM/Timer Control	I/O	F	None, None	47	61	R5
PH[5]	PCR[104]	Option 0 Option 1 Option 2 Option 3	GPIO[104] VLCD[8] — —	—	SIUL LCD — —	I/O	S	None, None	21	21	N2
PH[6]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[7]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[8]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[9]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[10]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[11]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[12]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[13]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[15]	—	—	Reserved	—	—	—	—	—	—	—	—
PJ[0]	PCR[105]	Option 0 Option 1 Option 2 Option 3	GPIO[105] PDI_DE — —	—	SIUL PDI — —	I/O	S	None, None	—	119	A2

Table 10. Signal details (continued)

Signal	Peripheral	Description
RXD_1	LINFlex	SCI/LIN Receive data signal. Input pad for the LIN SCI module. Connects to the internal LIN second port.
TXD_0	LINFlex	SCI/LIN Transmit data signal. This port is used to download the code for the BAM boot sequence.
TXD_1	LINFlex	SCI/LIN Transmit data signal—Transmit (output) port for the second LIN module in the chip.
SOUND	SGL	Sound signal to the speaker/buzzer.
SSD[0:5]_0 SSD[0:5]_1 SSD[0:5]_2 SSD[0:5]_3	SSD	Bidirectional control of stepper motors using stall detection module.
M[0:5]C0M M[0:5]C0P M[0:5]C1M M[0:5]C1P	SMC	Controls stepper motors in various configurations.
CLKOUT	MC_CGM	Output clock—It can be selected from several internal clocks of the device from the clock generation module.

Table 19. ESD absolute maximum ratings[1] [2]

Symbol		C	Ratings	Conditions	Class	Max value	Unit
$V_{ESD(HBM)}$	CC	T	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	CC	T	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	CC	T	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
						750 (corners)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3.6.4.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 20. Latch-up results

Symbol		C	Parameter	Conditions	Class
LU	CC	T	Static latch-up class	T_A = 105 °C conforming to JESD 78	II level A

3.7 Power management electrical characteristics

3.7.1 Voltage regulator electrical characteristics

The internal high power or main regulator (HPREG) requires an external NPN ballast transistor (see Table 21 and Table 22) to be connected as shown in Figure 7 as well as an external capacitance (C_{REG}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 15 nH.

For the MPC5606S microcontroller, 100 nF should be placed between each of the V_{DD12}/V_{SS12} supply pairs and also between the V_{DDPLL}/V_{SSPLL} pair. These decoupling capacitors are in addition to the required stability capacitance. Additionally, 10 µF should be placed between the V_{DDR} pin and the adjacent V_{SS} pin.

V_{DDR} = 3.0 V to 3.6 V / 4.5 V to 5.5 V, T_A = –40 to 105 °C, unless otherwise specified.

Table 24. Low-power voltage regulator electrical characteristics (continued)

Symbol		C	Parameter		Conditions	Value			Unit
						Min	Typ	Max	
	CC	D	Power supply rejection	@ DC @ no load	C_L = 10 µF × 4	—	—	55	dB
		D		any frequency @ no load				32	
		D		@ DC @ max load				24	
		D		any frequency @ max load				12	
	CC	D	Load current transient		C_L = 10 µF × 4	—	—	10% to 90% of I_L in 10 µs	
t_{SU}	CC	C	Start-up time after input supply stabilizes[2]		C_L = 10 µF × 4	—	—	700	µs

1 On this device, the ultra-low-power regulator is always enabled when the low-power regulator is enabled. Therefore, the total low-power current capacity is the sum of I_L values for the two regulators.

2 Time after the input supply to the voltage regulator has ramped up (V_{DDR}) and the voltage regulator has asserted the Power OK signal.

Table 25. Ultra-low-power voltage regulator electrical characteristics

Symbol		C	Parameter		Conditions	Value			Unit
						Min	Typ	Max	
T_J	SR	C	Junction temperature		—	–40	—	150	°C
I_{REG}	CC	C	Current consumption		Reference included, @ 55 °C No load @ Full load	—	—	2 100	µA
I_L	CC	C	Output current capacity		DC load current	—	—	5	mA
V_{DD12}	CC	C	Output voltage (value @ I_L = 0 @ 27 °C)		Pre-trimming sigma < 7 mV	—	1.33	—	V
					Post-trimming	1.15	1.24	—	
	CC	D	Power supply rejection	@ DC @ no load	—	—	—	25	dB
		D		any frequency @ no load				7	
		D		@ DC @ max load				25	
		D		any frequency @ max load				8	
	CC	D	Load current transient		—	—	—	10 to 90 µA in 70 µs	

3.7.2 Voltage monitor electrical characteristics

The device implements a Power-on Reset (POR) module to ensure correct power-up initialization, as well as four low voltage detectors (LVDs) to monitor the V_{DD} and the V_{DD12} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply

Table 27. DC electrical characteristics

Symbol		C	Parameter	Conditions[1]	T_A	Value			Unit
						Min	Typ	Max	
I_{DDRUN}[2]	CC	P	RUN mode current	—		—	130	180	mA
I_{DDHALT}	CC	P	HALT mode current	—		—	4	25	mA
I_{DDSTOP}	CC	P	STOP mode current	16 MHz fast internal RC oscillator off, HPVREG off	25°C	—	250	1800	µA
					105°C	—	5	20	mA
				16 MHz fast internal RC oscillator off, HPVREG on	25°C	—	2.5	6.5	mA
					105°C	—	7	25	mA
$I_{DDSTDBY}$	CC	C	STANDBY mode current	See Table 28					
$I_{DDSTDBY1}$[3]	CC	P	STANDBY1 mode current		25°C	—	20	100	µA
					105°C	—	180	—	µA
				T_J = 150°C	—	—	350	1500	µA
$I_{DDSTDBY2}$[4]	CC	P	STANDBY2 mode current		25°C	—	30	100	µA
					105°C	—	350	—	µA
				T_J = 150°C	—	—	600	2500	µA

1 V_{DD} = 3.3 V ±10% / 5.0 V ±10%, T_A = –40 to 105 °C

2 Value is for maximum peripherals turned on. May vary significantly based on different configurations, active peripherals, operating frequency, etc.

3 ULPreg on, HP/LPVreg off, 8 KB RAM on, device configured for minimum consumption, all possible modules switched off.

4 ULPreg on, HP/LPVreg off, 32 KB RAM on, device configured for minimum consumption, all possible modules switched off.

Table 28. IDDSTDBY specification[1]

Temperature (T_A,°C)	FIRC off, 8 KB RAM on		FIRC on, 8 KB RAM on		32 kHz SXOSC on, 8 KB RAM on		32 kHz SXOSC on, all RAM on	
	3.3 V	5.5 V	3.3 V	5.5 V	3.3 V	5.5 V	3.3 V	5.5 V
–40	16 µA	25 µA	326 µA	340 µA	16 µA	26 µA	22 µA	32 µA
0	18 µA	29 µA	334 µA	347 µA	19 µA	29 µA	26 µA	37 µA
25	23 µA	33 µA	342 µA	355 µA	24 µA	34 µA	34 µA	45 µA
55	41 µA	51 µA	363 µA	377 µA	42 µA	53 µA	69 µA	80 µA
85	93 µA	104 µA	421 µA	435 µA	100 µA	110 µA	182 µA	195 µA
105	173 µA	185 µA	502 µA	517 µA	181 µA	194 µA	344 µA	358 µA
125[2]	320 µA	334 µA	648 µA	667 µA	321 µA	335 µA	620 µA	638 µA
150[2]	681 µA	698 µA	1005 µA	1028 µA	654 µA	677 µA	1270 µA	1300 µA

1 All current values are typical values.

2 Values provided for reference only. The permitted temperature range of the chip is specified separately.

3.7.4 Recommended power-up and power-down order

Figure 10 shows the recommended order for powering up the power supplies on this device.

The 1.2 V regulator output starts after the device's internal POR (VDDREG HV) is deasserted at approximately 2.7 V on VDDREG.

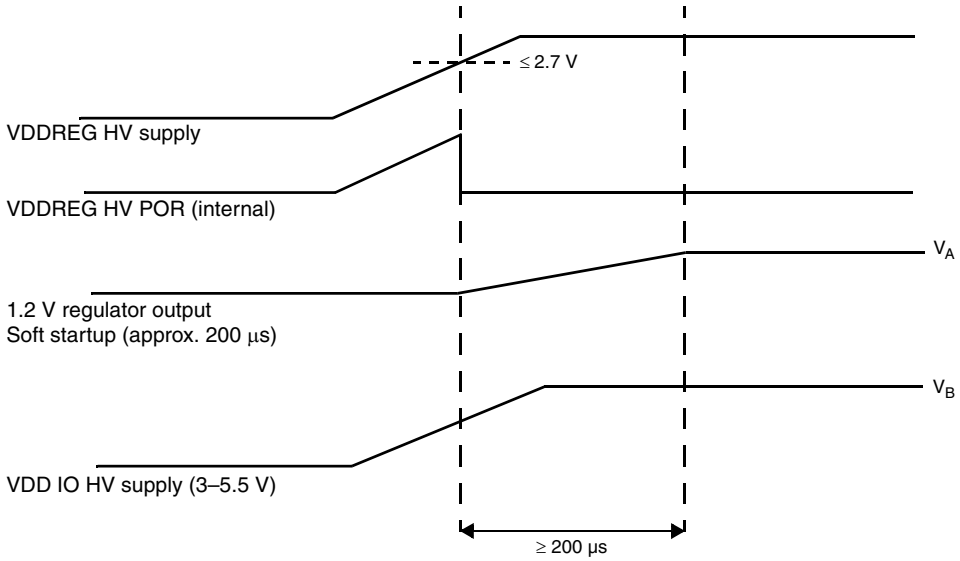


Figure 10. Recommended order for powering up the power supplies

CAUTION

The voltages V_A and V_B in Figure 10 must always obey the relation $V_B \geq V_A - 0.7$ V. Otherwise, currents from the 1.2 V supply to the 3.3 V supply may result.

Figure 11 shows the recommended order for powering down the power supplies on this device.

It is acceptable for the VDD IO HV supply to ramp down faster than the 1.2 V regulator output, even if the latter takes time to discharge the high 40 µF capacitance. (The capacitor will ultimately discharge.)

Table 32. SLOW configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
T_{tr}	CC	T	Output transition time output pin[3] SLOW configuration	C_L = 25 pF, V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF, V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	100	
		T		C_L = 100 pF, V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	125	
		T		C_L = 25 pF, V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	40	
		T		C_L = 50 pF, V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	50	
		T		C_L = 100 pF, V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	75	
ΔI_{tr50}	CC	D	Current slew at C_L = 50 pF SLOW configuration	recommended configuration at V_{DD} = 5.0 V ±10%, PAD3V5V = 0 V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	2	mA/ns
		D		V_{DD} = 5.0 V ±10%, PAD3V5V = 1	—	—	7	

1 V_{DD} = 3.3 V ±10% / 5.0 V ±10%, T_A = –40 to 105 °C, unless otherwise specified

2 This is a transient configuration during power-up. All pads but $\overline{\text{RESET}}$ and NEXUS output (MDOx, EVTO, MCK) are configured in input or in high impedance state.

3 C_L calculation should include device and package capacitances (C_{PKG} < 5 pF).

Table 33. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{OH}	CC	P	Output high level MEDIUM configuration	Push Pull, I_{OH} = –2 mA, V_{DD} = 5.0 V ±10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	V
		D		Push Pull, I_{OH} = –1 mA, V_{DD} = 5.0 V ±10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C		Push Pull, I_{OH} = –1 mA, V_{DD} = 3.3 V ±10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level MEDIUM configuration	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ±10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		D		Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ±10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C		Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ±10%, PAD3V5V = 1 (recommended)	—	—	0.5	

Table 43. Slow external crystal oscillator (32 KHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	T	Slow external crystal oscillator frequency	—	32	—	40	kHz
V_{SXOSC}	CC	T	Oscillation amplitude	V_{DD} = 3.3 V ± 10%	1.12	1.33	1.74	V
		T		V_{DD} = 5.0 V ± 10%	1.12	1.37	1.74	
I_{SXOSC}	CC	D	Slow external crystal oscillator consumption	—	—	—	5	µA
$T_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	—	2[2]	s
V_{IH}	SR	D	Input high level CMOS Schmitt Trigger	Oscillator bypass mode	0.65V_{DD}	—	V_{DD} + 0.4	V
V_{IL}	SR	D	Input low level CMOS Schmitt Trigger	Oscillator bypass mode	–0.4	—	0.35V_{DD}	V

1 V_{DD} = 3.3 V ±10% / 5.0 V ±10%, T_A = –40 to 105 °C, unless otherwise specified

2 The quoted figure is based on a board that is properly laid out and has no stray capacitances.

3.13 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 44. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	T	FMPLL reference clock[2]	—	4	—	64	MHz
Δ_{PLLIN}	SR	T	FMPLL reference clock duty cycle[2]	—	40	—	60	%
f_{PLLOUT}	CC	T	FMPLL output clock frequency	—	16	—	64	MHz
f_{CPU}	CC	T	System clock frequency	—	—	—	64[3]	MHz
t_{LOCK}	CC	T	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)	—	—	200	µs
Δt_{PKJIT}	CC	T	FMPLL jitter (peak to peak)	f_{PLLIN} = 16 MHz (resonator)	—	—	220	ps
Δt_{LTJIT}	CC	T	FMPLL long term jitter	f_{PLLIN} = 16 MHz (resonator)	—	—	1.5	ns
I_{PLL}	CC	D	FMPLL consumption	T_A = 25 °C	—	—	4	mA

1 V_{DDPLL} = 1.2 V ±10%, T_A = –40 to 105 °C, unless otherwise specified.

2 PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.

3 f_{CPU} 64 MHz can be achieved only at temperatures up to T_A = 105 °C with a maximum FM depth of 2%.

Table 53. Pad AC specifications (3.3 V, PAD3V5V = 1)[1] (continued)

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
3	Fast	1	—	6	1	—	4	—	—	72	3	—	40	25
		1	—	6	1.5	—	7	—	—	55	3	—	40	50
		1	—	6	3	—	12	—	—	40	3	—	40	100
		1	—	6	5	—	18	—	—	25	3	—	40	200
4	Pull Up/Down (3.6 V max)	—	—	—	—	—	7500	—	—	—	—	—	—	50
Parameter Classification		D			C			C			C			n/a

[1] Propagation delay from $V_{DD}/2$ of internal signal to Pchannel/Nchannel on condition

[2] Slope at rising/falling edge

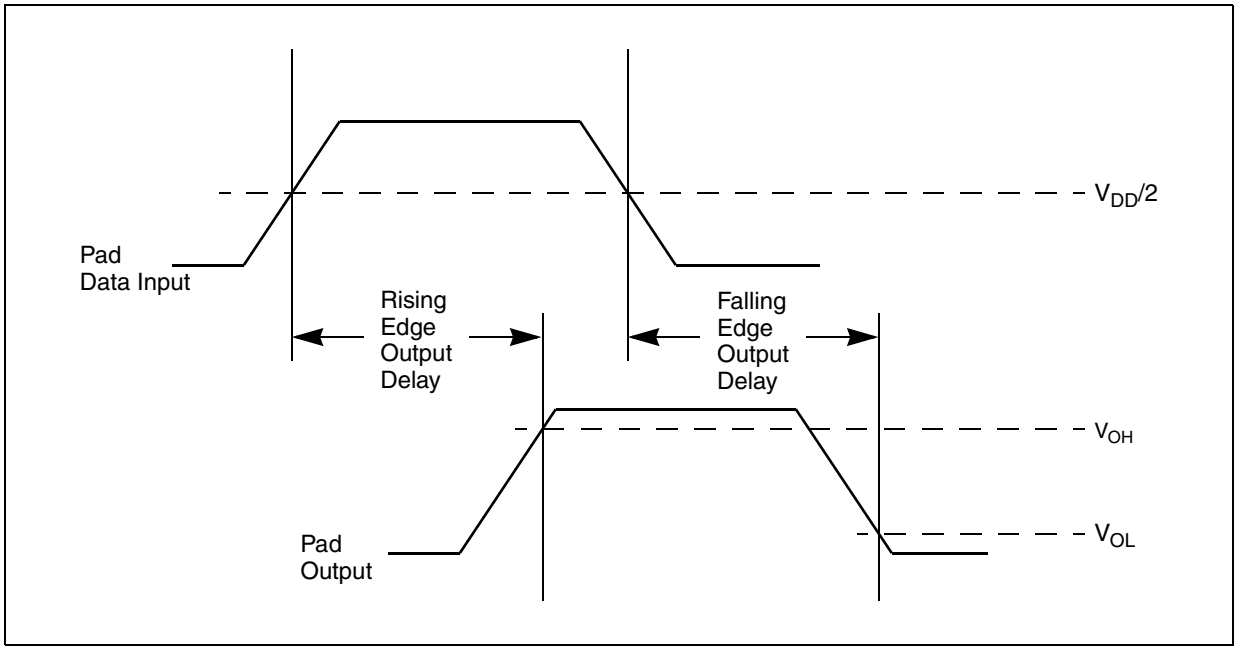


Figure 26. Pad output delay

3.20.6 FlexCAN timing

The CAN functions are available as TX pins at normal I/O pads and as RX pins at the always on domain. There is no filter for the wakeup dominant pulse. Any high-to-low edge can cause wakeup if configured.

Table 61. FlexCAN timing[1]

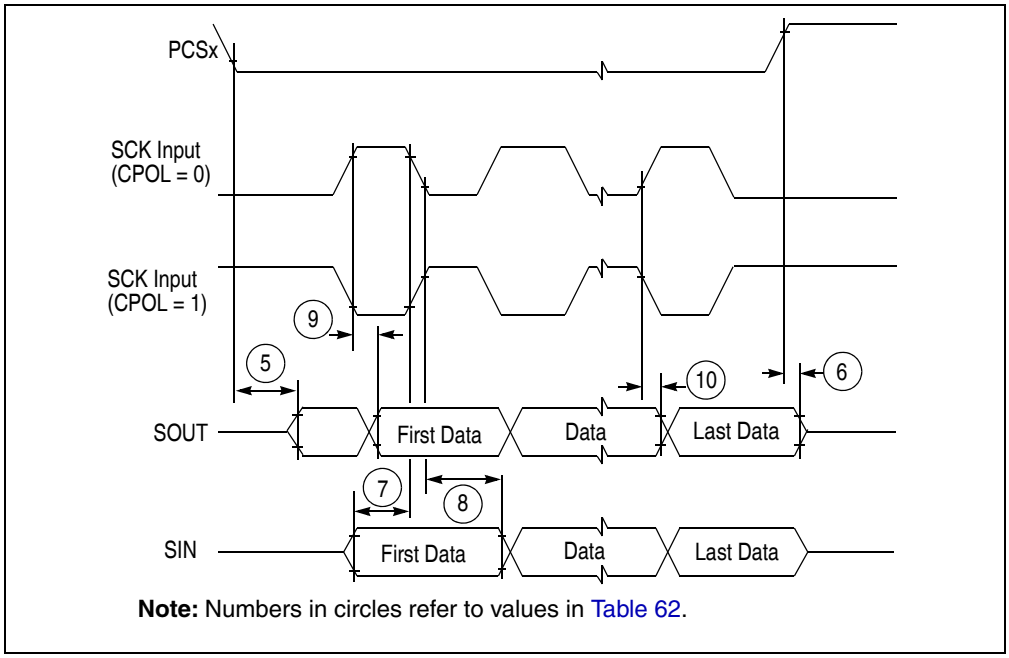
No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	t_{CANOV}	CC	D	CTNX Output Valid after CLKOUT Rising Edge (Output Delay)	—	22.48	ns
2	t_{CANSU}	CC	D	CNRX Input Valid to CLKOUT Rising Edge (Setup Time)	—	12.46	ns

1 FlexCAN timing specified at f_{SYS} = 64 MHz, V_{DD12} = 1.14 V to 1.32 V, VDDE_x = 3.0 V to 5.5 V, T_A = –40 to 105 °C, and C_L = 50 pF with SRC = 0b00.

3.20.7 Deserial Serial Peripheral Interface (DSPI)

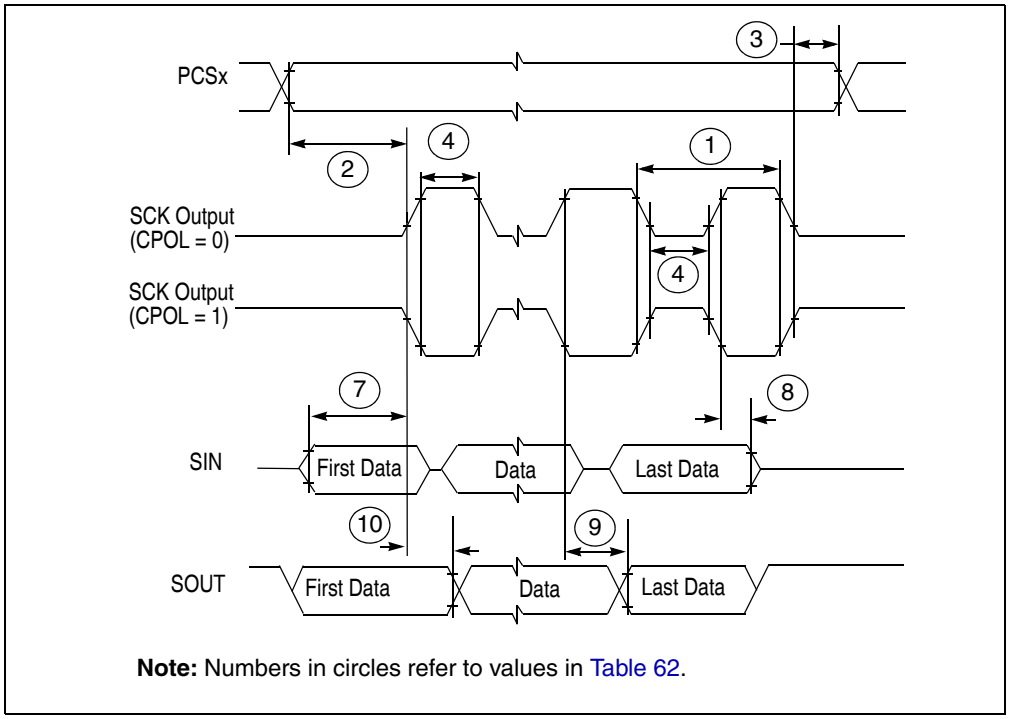
Table 62. DSPI timing[1]

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{SCK}	CC	D	DSPI Cycle TIme[2,3]	Master (MTFE = 0) Slave (MTFE = 0) Slave Receive Only Mode	62 62 62	— — —	ns ns ns
2	t_{CSC}	CC	D	PCS to SCK Delay[4]	—	20	—	ns
3	t_{ASC}	CC	D	After SCK Delay[5]	—	20	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle	—	0.4 x t_{SCK}	0.6 x t_{SCK}	ns
5	t_A	CC	D	Slave Access Time (PCSx active to SOUT driven)	SS active to SOUT valid	—	40	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time (PCSx inactive to SOUT High-Z or invalid)	SS inactive to SOUT High-Z or invalid	—	10	ns
7	t_{PCSC}			PCSx to PCSS time	—	20	—	ns
8	t_{PASC}			PCSS to PCSx time	—	20	—	ns
9	t_{SUI}	CC	D	Data Setup Time for Inputs	Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[6] Master (MTFE = 1, CPHA = 1)	35 2 20 35	— — — —	ns ns ns ns
10	t_{HI}	CC	D	Data Hold Time for Inputs	Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[6] Master (MTFE = 1, CPHA = 1)	–5 5 10 –5	— — — —	ns ns ns ns



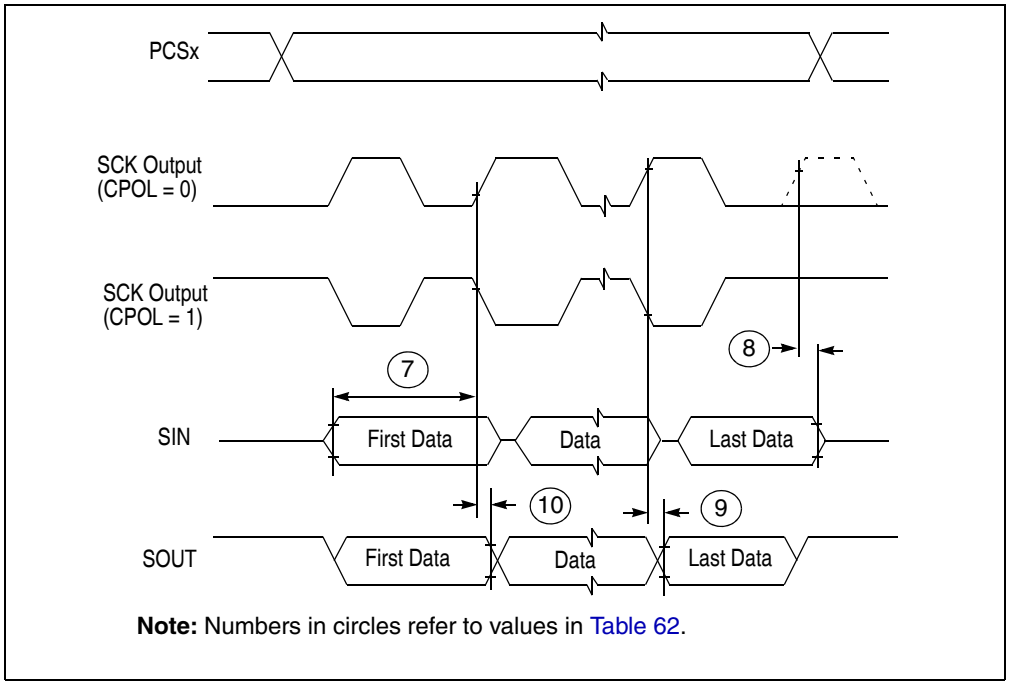
Note: Numbers in circles refer to values in Table 62.

Figure 41. DSPI classic SPI timing — slave, CPHA = 1



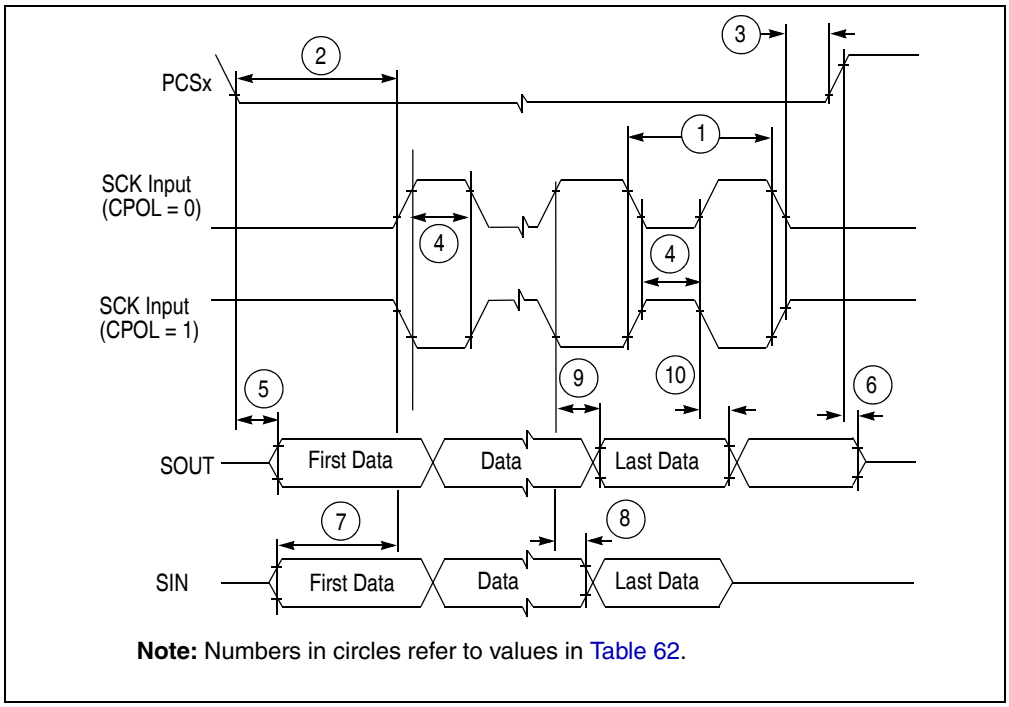
Note: Numbers in circles refer to values in Table 62.

Figure 42. DSPI modified transfer format timing — master, CPHA = 0



Note: Numbers in circles refer to values in Table 62.

Figure 43. DSPI modified transfer format timing — master, CPHA = 1



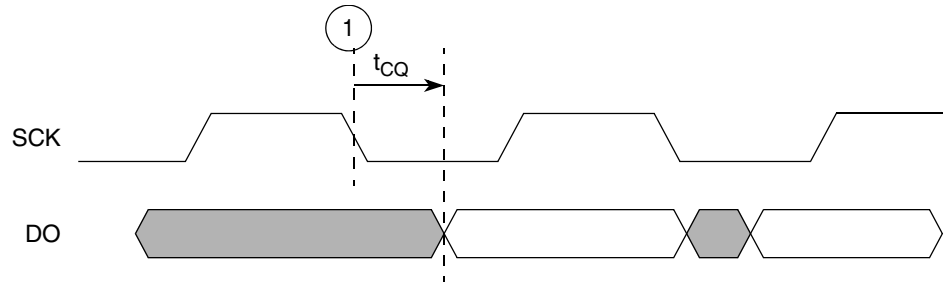
Note: Numbers in circles refer to values in Table 62.

Figure 44. DSPI modified transfer format timing — slave, CPHA = 0

- Timings correspond to QSPI_SMPR = 0x0000_000x. See the *MPC5606S Microcontroller Reference Manual* for details.
- A negative value of hold is an indication of pad delay on the clock pad (delay between the edge capturing data inside the device and the edge appearing at the pin).
- Values are with a load of 15 pF on the output pins.

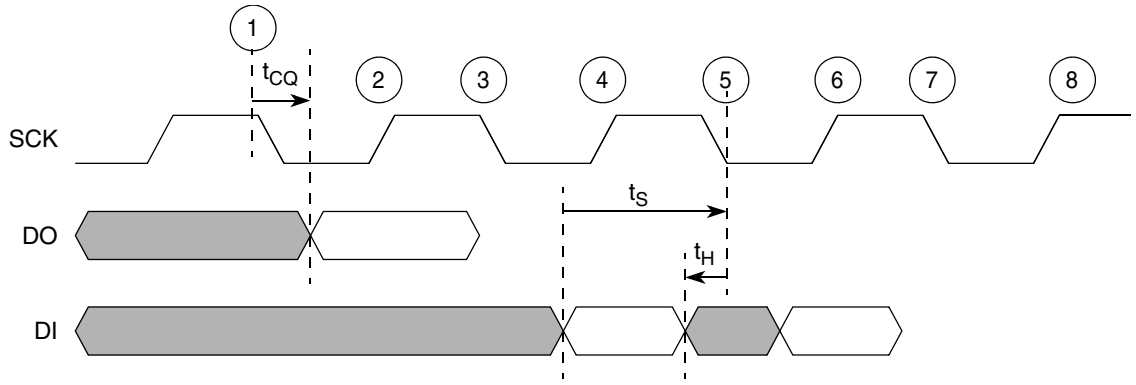
Table 65. QuadSPI timing

Symbol		C	Parameter	Value			Unit
				Min	Typ	Max	
t_{CQ}	CC	T	Clock to Q delay	1.60	2.4	5.33	ns
t_S	CC	T	Setup time for incoming data	6.1	9.4	12.1	ns
t_H	CC	T	Hold time requirement for incoming data	–12.5	–8.5	–7.5	ns
t_R	CC	T	Clock pad rise time	0.4	0.6	1.0	ns
t_F	CC	T	Clock pad fall time	0.3	0.5	0.9	ns



1. Last address out

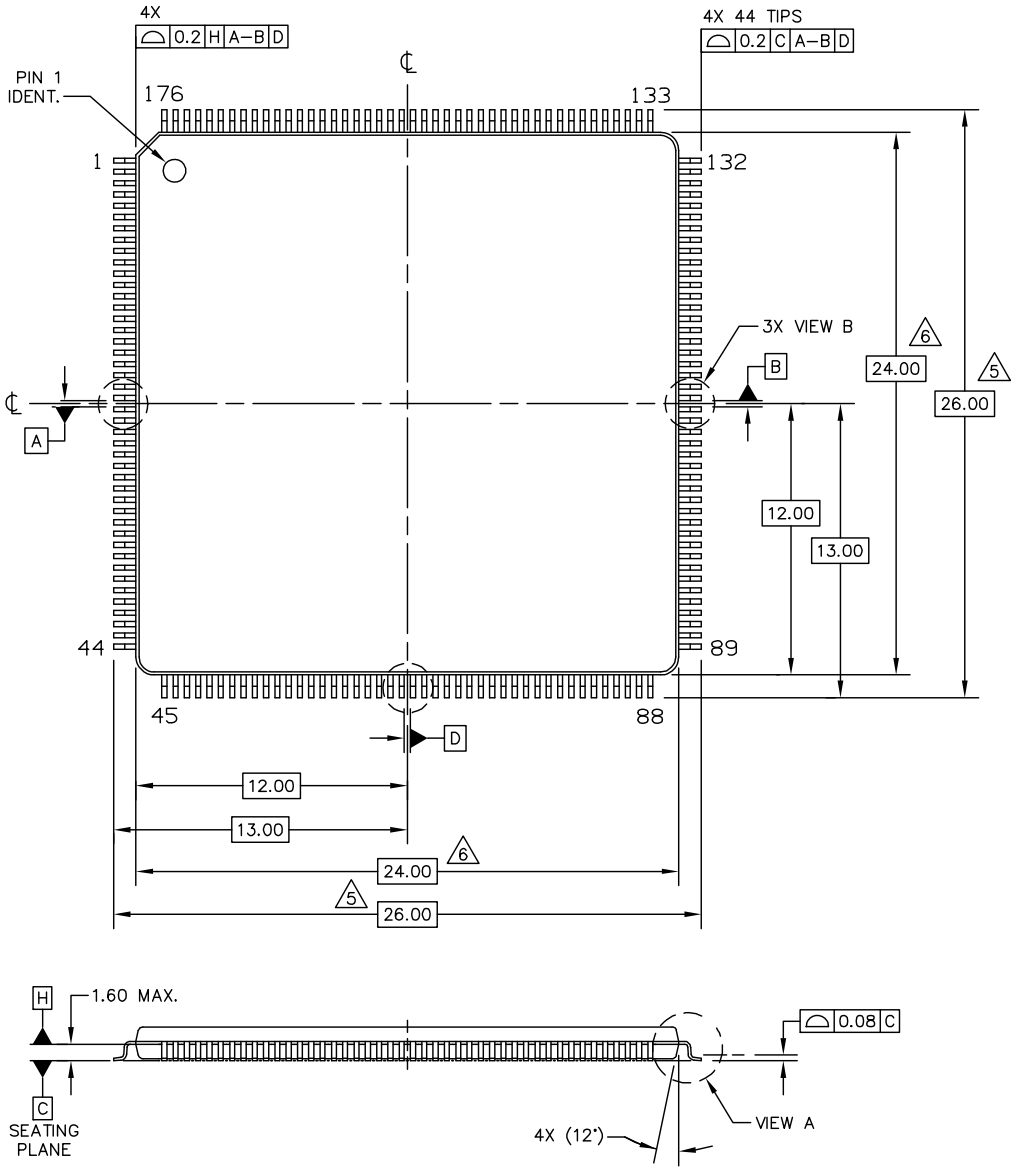
Figure 47. QuadSPI output timing diagram



1. Last address out
2. Address captured at flash
3. Data out from flash
4. Ideal data capture edge
5. Delayed data capture edge with QSPI_SMPR=0x0000_000x
6. Delayed data capture edge with QSPI_SMPR=0x0000_002x
7. Delayed data capture edge with QSPI_SMPR=0x0000_004x
8. Delayed data capture edge with QSPI_SMPR=0x0000_006x

Figure 48. QuadSPI input timing diagram

4.2 176 LQFP



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TITLE: 176 LD TQFP, 24 X 24 PKG, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23479W	REV: B
	CASE NUMBER: 1101–01	02 JUN 2005
	STANDARD: JEDEC MS–026 BGA	

Figure 53. LQFP176 mechanical drawing (Part 1 of 3)