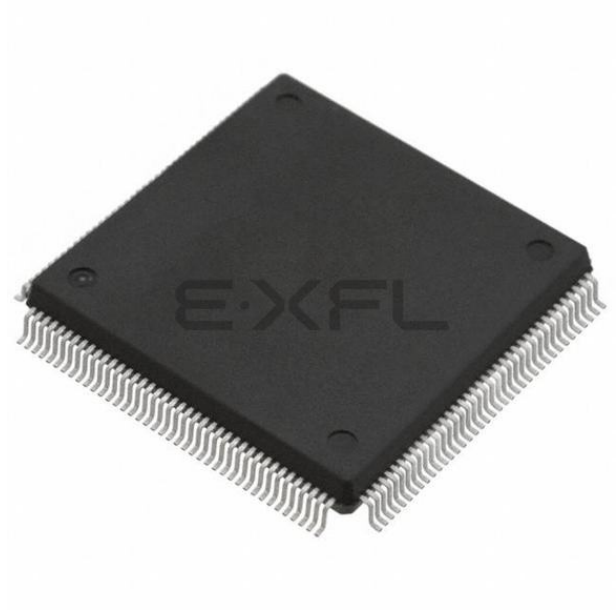

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	40MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	160-BQFP
Supplier Device Package	160-QFP (28x28)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5206eft40

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

2.5.2 Size (SIZ[1:0])

These three-state bidirectional signals indicate the transfer data size for the bus cycle. When an alternate bus master is controlling the bus, the MCF5206e monitors these signals to determine the data size for asserting the appropriate memory control signals. Table 2-7 shows the definitions of the SIZ[1:0] encoding.

Table 2-7. Data Transfer Size Encoding

SIZ[1:0]	DATA TRANSFER SIZE
00	Longword
01	Byte
10	Word
11	Line

2.5.3 Transfer Type (TT[1:0])

These three-state output signals indicate the type of access for the current bus cycle. TT[1:0] are not sampled by the MCF5206e during alternate master transfers. Table 2-8 lists the definitions of the TT[1:0] encodings.

Table 2-8. Bus Cycle Transfer Type Encoding

TT[1:0]	TRANSFER TYPE
0 0	Normal Access
0 1	DMA Access
1 0	Emulator Access
1 1	CPU Space or Interrupt Acknowledge

2.5.4 Access Type and Mode (ATM)

This three-state output signal provides supplemental information for each transfer cycle type. ATM is not sampled by the MCF5206e during alternate master transfers. Table 2-9 lists the encoding for normal, debug and CPU space/interrupt-acknowledge transfer types.

Table 2-9. ATM Encoding

TRANSFER TYPE	INTERNAL TRANSFER MODIFIER	ATM (TS=0)	ATM (TS=1)
00 (Normal Access)	Supervisor Code	1	1
	Supervisor Data	0	1
	User Code	1	0
	User Data	0	0

3.2.2 MAC Unit User Programming Model

The MAC portion of the user programming model available on the 5206e microprocessor core is shown below. It consists of the following registers:

- 32-bit accumulator (ACC)
- 16-bit mask register (MASK)
- 8-bit MAC status register (MACSR)

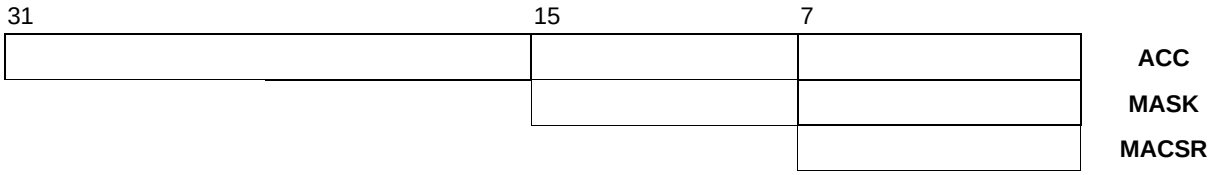


Figure 3-3. MAC Unit User Programming Model

3.2.3 Hardware Divide Module

The MCF5206e processor includes a hardware divider which performs a number of integer divide operations. The supported divide functions include: 32/16 producing a 16-bit quotient and 16-bit remainder, 32/32 producing a 32-bit quotient, and 32/32 producing 32-bit remainder.

3.2.4 Supervisor Programming Model

Only system programmers use the supervisor programming model to implement sensitive operating system functions, I/O control, and memory management. All accesses that affect the control features of ColdFire processors are in the supervisor programming model, which consists of the registers available to users as well as the following control registers:

- 16-bit status register (SR)
- 32-bit vector base register (VBR)

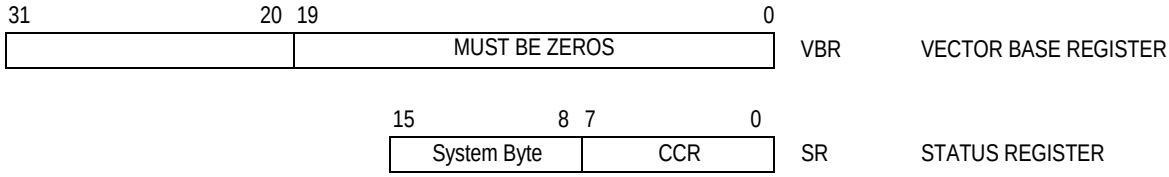


Figure 3-4. Supervisor Programming Model

Additional registers may be supported on a part-by-part basis.

The following paragraphs describe the supervisor programming model registers.

3.2.4.1 STATUS REGISTER. The SR stores the processor status and includes the CCR, the interrupt priority mask, and other control bits. In the supervisor mode, software can access the entire SR. In user mode, only the lower 8 bits are accessible (CCR). The control

3.5.10 Fault-on-Fault Halt

If a V2 processor encounters any type of fault during the exception processing of another fault, the processor immediately halts execution with the catastrophic “fault-on-fault” condition. A reset is required to force the processor to exit this halted state.

3.5.11 Reset Exception

Asserting the reset input signal to the processor causes a reset exception. The reset exception has the highest priority of any exception; it provides for system initialization and recovery from catastrophic failure. Reset also aborts any processing in progress when the reset input is recognized. Processing cannot be recovered.

The reset exception places the processor in the supervisor mode by setting the S bit and disables tracing by clearing the T bit in the SR. This exception also clears the M bit and sets the processor’s interrupt priority mask in the SR to the highest level (level 7). Next, the VBR is initialized to zero ($00000000). The control registers specifying the operation of any memories (e.g., cache and/or RAM modules) connected directly to the processor are disabled.

Note

Other implementation-specific supervisor registers are also affected. Refer to each of the modules in this user’s manual for details on these registers.

Once the processor is granted the bus and it does not detect any other alternate masters taking the bus, the core then performs two longword read bus cycles. The first longword at address 0 is loaded into the stack pointer and the second longword at address 4 is loaded into the program counter. After the initial instruction is fetched from memory, program execution begins at the address in the PC. If an access error or address error occurs before the first instruction is executed, the processor enters the fault-on-fault halted state.

3.6 INSTRUCTION EXECUTION TIMING

This section presents V2 processor instruction execution times in terms of processor core clock cycles. The number of operand references for each instruction is enclosed in parentheses following the number of clock cycles. Each timing entry is presented as **C**(r/w) where:

- **C** - number of processor clock cycles, including all applicable operand fetches and writes, and all internal core cycles required to complete the instruction execution.
- r/w - number of operand reads (r) and writes (w) required by the instruction. An operation performing a read-modify-write function is denoted as (1/1).

This section includes the assumptions concerning the timing values and the execution time details.

3.6.1 Timing Assumptions

For the timing data presented in this section, the following assumptions apply:

to a chip select or default memory, the assertion of TA is controlled by the number of wait states and the setting of the external master automatic acknowledge (EMAA) bit in the Chip Select Control Registers (CSCRs) or the Default Memory Control Register (DMCR). If the external master-requested transfer is a DRAM access, the MCF5206e drives TA as an output and is asserted at the completion of the transfer.

6.2.10 Transfer Error Acknowledge (TEA)

The external slave asserts this active-low input signal to indicate an error condition for the current transfer. The assertion of TEA immediately aborts the bus cycle. The assertion of TEA has precedence over the assertion of asynchronous transfer acknowledge (ATA) and transfer acknowledge (TA).

NOTE

TEA can be asserted up to one clock after the assertion of asynchronous transfer acknowledge (ATA) and still be recognized.

TEA has no affect during DRAM accesses.

6.3 BUS EXCEPTIONS

6.3.1 Double Bus Fault

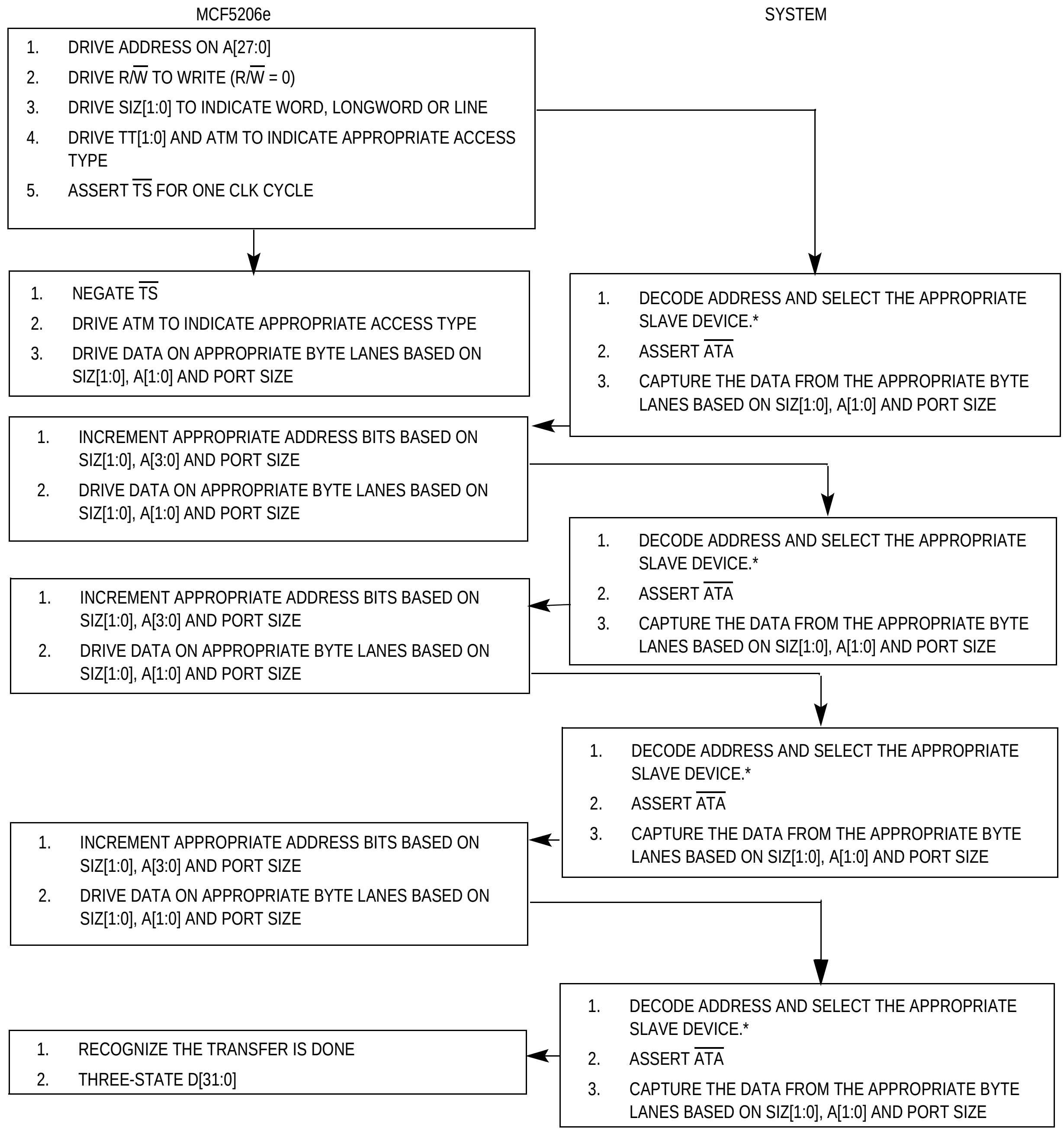
If the MCF5206e experiences a double bus fault, it enters the halted state. To exit the halt state, reset the MCF5206e.

6.4 BUS CHARACTERISTICS

The MCF5206e uses the address bus (A[27:0]) to specify the location for a data transfer and the data bus (D[31:0]) to transfer the data. Control and attribute signals indicate the beginning and type of a bus cycle as well as the address space, direction, and size of the transfer. The selected device or the number of wait states programmed in the memory control register (the Chip Select Control Register (CSCR), the DRAM Controller Control Registers (DCCR, including the DRAM Controller Timing Register (DCTR)), or the Default Memory Control Register (DMCR)) control the length of the cycle.

The MCF5206e clock is distributed internally to provide logic timing. All bus signals are synchronous with the rising edge of CLK with the exception of row address strobes (RAS[1:0]) and column address strobes (CAS[3:0]), which can be asserted and negated synchronous with the falling edge of CLK.

Inputs to the MCF5206e (other than the interrupt priority level signals (IPLx), reset in (RSTI) and ATA signals) are synchronously sampled and must be stable during the sample window defined by t_{si} and t_{hi} (as shown in Figure 6-1) to guarantee proper operation. The asynchronous IPLx, RSTI and ATA signals are internally synchronized to resolve the input to a valid level before being used.



*TO INSERT WAIT STATES, ATA IS DRIVEN NEGATED.

Figure 6-22. Word-, Longword-, and Line-Write Transfer Flowchart with Asynchronous Termination

Table 6-14. Signal Source During External Master Accesses

MEMORY SPACE	ADDRESS (DRIVEN BY)	CONTROL SIGNALS	TRANSFER ACKNOWLEDGE
Chip Select	External Master	CS[7:0], WE[3:0]	MCF5206e: if EMAA in CSCR is set to 1
DRAM	MCF5206e: if DCAR in DCCR is set to 1	$\overline{RAS}$[1:0], $\overline{CAS}$[3:0], $\overline{DRAMW}$	MCF5206e
Default Memory	External Master	-	MCF5206e: if EMAA in DMCR is set to 1

6.10.1 External Master Read Transfer Using MCF5206e Termination

The basic read cycle of an external master transfer using MCF5206e-generated termination is the same as a ColdFire core initiated transfer with one additional CLK cycle between the assertion of $\overline{TS}$ by the external master and the starting of the internal wait-state counter by the MCF5206e. During this CLK cycle, the MCF5206e decodes the external master address to determine the appropriate memory control and termination signals that must be asserted. For more information on chip select transfers and DRAM transfers, refer to **Section 8 Chip Selects** and **Section 10 DRAM Controller**.

Figure 6-41 is a flow chart for external master read transfers using MCF5206e-generated automatic acknowledge to access 8-, 16-, or 32-bit ports. Bus operations are similar for each case and vary only with the size indicated, the portion of the data bus used for the

SECTION 7
DMA CONTROLLER MODULE

7.1 INTRODUCTION

The Direct Memory Access Controller (DMA) Module provides a quick and efficient process for moving blocks of data with minimal processor overhead. The DMA module, shown in Figure 7-1, provides two channels that allow byte, word, or longword operand transfers. These transfers can be single or dual address to off-chip devices or dual address to on-chip devices.

7.4.2 Destination Address Register (DAR)

The destination address register (DAR) is a 32-bit register containing the address to which the DMA Controller Module will send data during a transfer. Note that this register is only used during dual address transfers.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DAR31	DAR30	DAR29	DAR28	DAR27	DAR26	DAR25	DAR24	DAR23	DAR22	DAR21	DAR20	DAR19	DAR18	DAR17	DAR16
Reset:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAR15	DAR14	DAR13	DAR12	DAR11	DAR10	DAR9	DAR8	DAR7	DAR6	DAR5	DAR4	DAR3	DAR2	DAR1	DAR0
Reset:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Destination Address Register (DAR)

7.4.3 Byte Count Register (BCR)

The byte count register (BCR) is a 16-bit register containing the number of bytes remaining to be transferred for a given block. The BCR count is the number of bytes remaining to be written.

The BCR decrements on the successful completion of the address phase of either a write transfer in dual address mode or any transfer in single address mode. The amount the BCR decrements is 1, 2, 4, or 16 for byte, word, longword, or line accesses, respectively.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCR15	BCR4	BCR13	BCR12	BCR11	BCR10	BCR9	BCR8	BCR7	BCR6	BCR5	BCR4	BCR3	BCR2	BCR1	BCR0
Reset:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Byte Count Register (BCR)

The DONE bit in the DMA Status Register is set when the entire block transfer is complete, when BCR = $00.

When a transfer sequence is initiated and the BCR contains a value that is not divisible by 16, 4, or 2 when the DMA is configured for line, longword, or word transfers, respectively, the configuration error bit in the DMA status register (DSR) is set and the transfer is not performed.

set to the top priority if a higher priority master constantly demands the bus. Possible solutions to this problem are:

- Changing the ARBCTRL setting at regular intervals to allow for different masters to share the highest priority.
- Using lower priority masters for “non-essential” tasks which can be completed in the idle bus cycles of the top priority master.
- Writing code which executes from the instruction cache or single-cycle on-chip SRAM and therefore provides more idle bus cycles for other masters to use.

The internal arbiter has been specifically designed to recognize bus cycles that hit in the cache and are prematurely terminated. These killed cycles often happen sequentially as the processor executes a line from the cache. When the arbiter sees an instruction fetch that has been killed, it will lower the priority of the ColdFire core for the next bus cycle. This allows the DMA channels to utilize bus bandwidth the ColdFire core would otherwise be wasting. The DMA channels should always use the largest transfer of which they are capable, to transfer the most data in any opportunity. When using interrupts, caution should be exercised if the ColdFire core is not the highest priority and not immediately able to answer the interrupt. This could result in a spurious interrupt condition. Use of the Bus Timeout Monitor is always recommended for use with non-core masters, since it can provide a method of escaping a master requesting bad transfers.

The NOARB bit simply disables arbiter operation. Setting the NOARB bit causes the MCF5206e to behave similarly to the MCF5206, however DMA transfers are not now allowed, since the DMA channels cannot arbitrate for the bus. This functionality has been provided primarily for customers upgrading older MCF5206 designs where the DMA would not be used.

NOARB - Arbiter operation disable.

0 = Arbitration enabled

1 = Arbitration disabled (MCF5206 mode)

The ARBCTRL bit determines the highest priority on the internal master bus. These options are shown in table 8-9:

Table 8-9. Arbitration Control Encodings (ARBCTRL)

ARBCTRL	HIGHEST PRIORITY BUS MASTER	LOWEST PRIORITY BUS MASTER
0	ColdFire Core	Internal DMA Channels
1	Internal DMA Channels	ColdFire Core

ARBCTRL - Set the arbitration priority for the internal master bus.

0 = Arbitration order = ColdFire Core, Internal DMA channels

1 = Arbitration order = Internal DMA channels, ColdFire Core

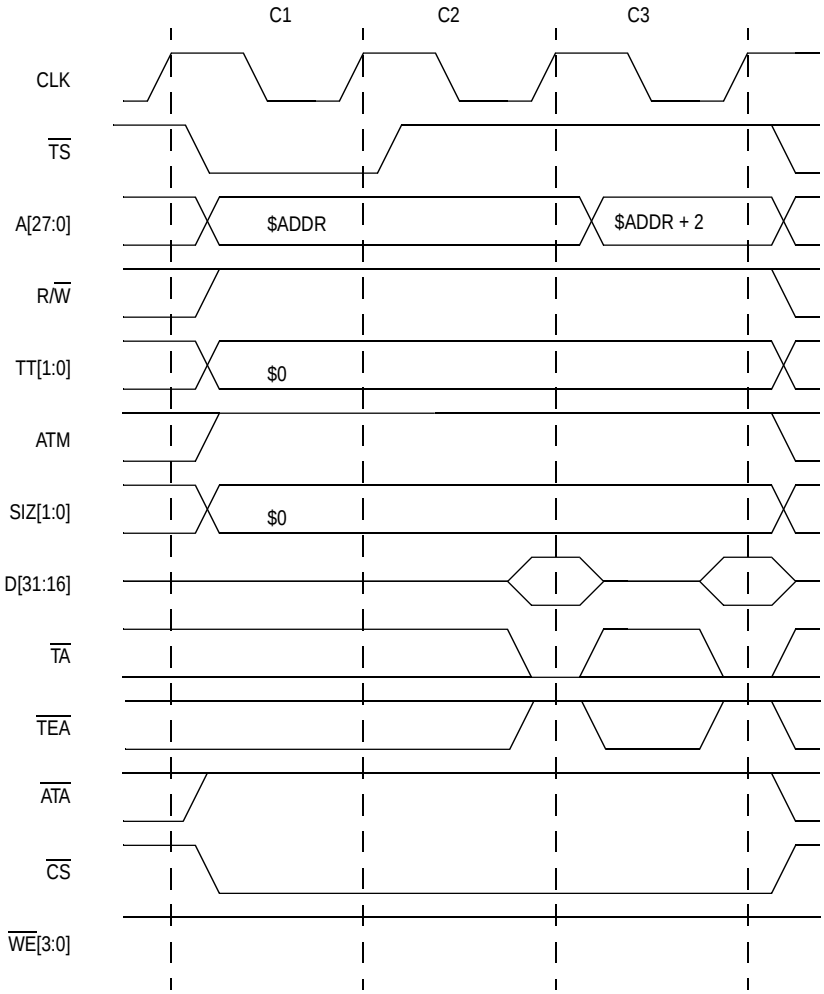


Figure 9-5. Longword Burst Read Transfer from a 16-Bit Port (No Wait States, No Address Setup, No Address Hold)

Clock 1 (C1)

The burst read cycle starts in C1. During C1, the MCF5206e places valid values on the address bus (A[27:0]) and transfer control signals. The transfer type (TT[1:0]) signals identify the specific access type and access type and mode (ATM) is driven high to identify the transfer as code. The read/write (R/W) and write enable (WE[3:0]) signals are driven high for a read cycle, and the size signals (SIZ[1:0]) are driven low to indicate a longword transfer. The MCF5206e asserts transfer start (TS) to indicate the beginning of a bus cycle and asserts the appropriate chip select (CS) for the address being accessed.

Clock 2 (C2)

During C2, the MCF5206e negates transfer start (TS), drives access type and mode (ATM) high to identify the transfer as supervisor. The selected device(s) places the addressed data onto D[31:16] and asserts the transfer acknowledge (TA). At the end of

Figure 11-9 shows the timing of a page being opened by a word write transfer to a 16-bit port in Fast Page Mode. The first word write transfer is followed by a page-hit word write transfer. The timing of the page-hit write transfer is the same regardless of whether the page was opened by a burst read, burst write, nonburst read, or nonburst write transfer.

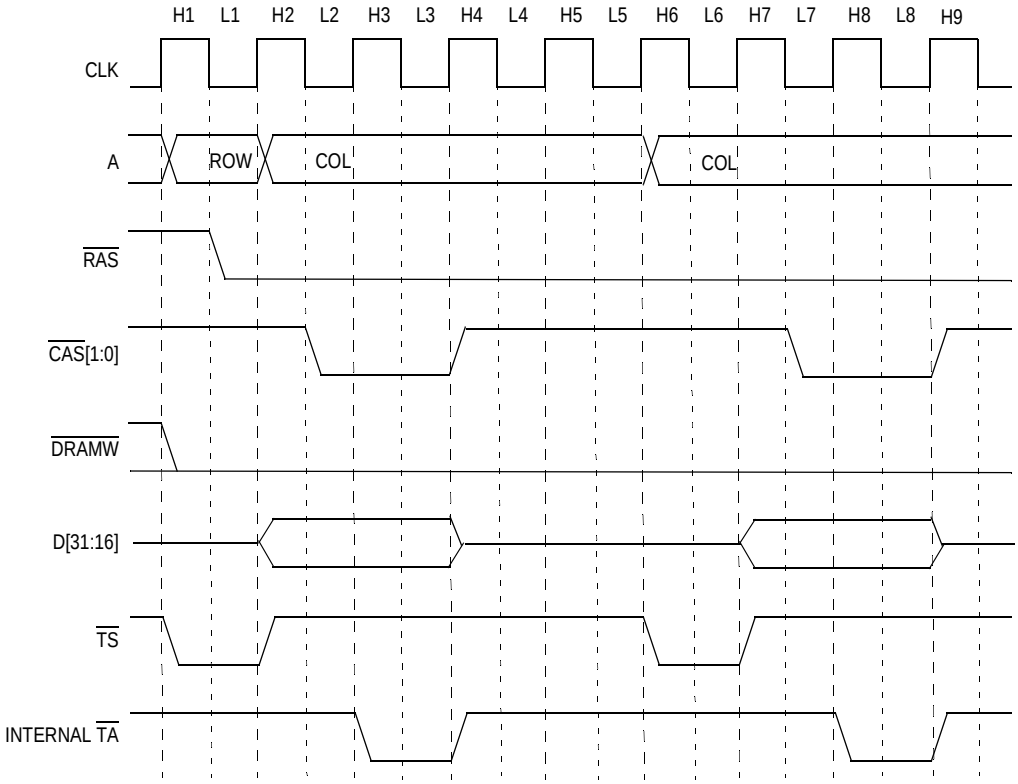


Figure 11-9. Word Write Transfer Followed by a Page-Hit Word Write Transfer in Fast Page Mode with 16-bit DRAM

Clock H1

The first word write transfer starts in H1. During H1, the MCF5206e drives the row address on A[27:9], drives DRAMW low indicating a DRAM write transfer, drives SIZ[1:0] to $2 indicating a word transfer, and asserts TS.

Clock L1

The MCF5206e asserts RAS to indicate the row address is valid on A[27:9].

Clock H2

The MCF5206e negates TS, drives the column address on A[27:9], and begins driving the data on D[31:16].

control the $\overline{CAS}$ assertion and negation time during fast page mode and burst page mode transfers. Refer to Figure 11-21 for a timing diagram of EDO DRAM page mode transfers.

0 = DRAM banks are populated with standard DRAM, do not use EDO $\overline{CAS}$ timing
1 = DRAM banks are populated with EDO DRAM, use EDO $\overline{CAS}$ timing

NOTE

If neither fast page mode or burst page mode are enabled in the DRAM Control Register (DCCR), the EDO Enable bit has no effect on the DRAM waveform timing.

RCD - $\overline{RAS}$-to-$\overline{CAS}$ Delay Time

This field controls the number of system clocks between the assertion of $\overline{RAS}$ and the assertion of $\overline{CAS}$ for transfers in normal mode and for the initial transfer to a page in fast page mode and burst page mode. Because the column address is always driven 0.5 system clocks prior to the assertion of $\overline{CAS}$, RCD affects the driving of the column address. RCD does not affect refresh cycles. Refer to Figure 11-17 for normal mode timing. Refer to Figures 11-18 and 11-19 for fast page mode and burst page mode timing.

0 = $\overline{RAS}$ asserts 1.0 system clock before the assertion of $\overline{CAS}$
1 = $\overline{RAS}$ asserts 2.0 system clocks before the assertion of $\overline{CAS}$

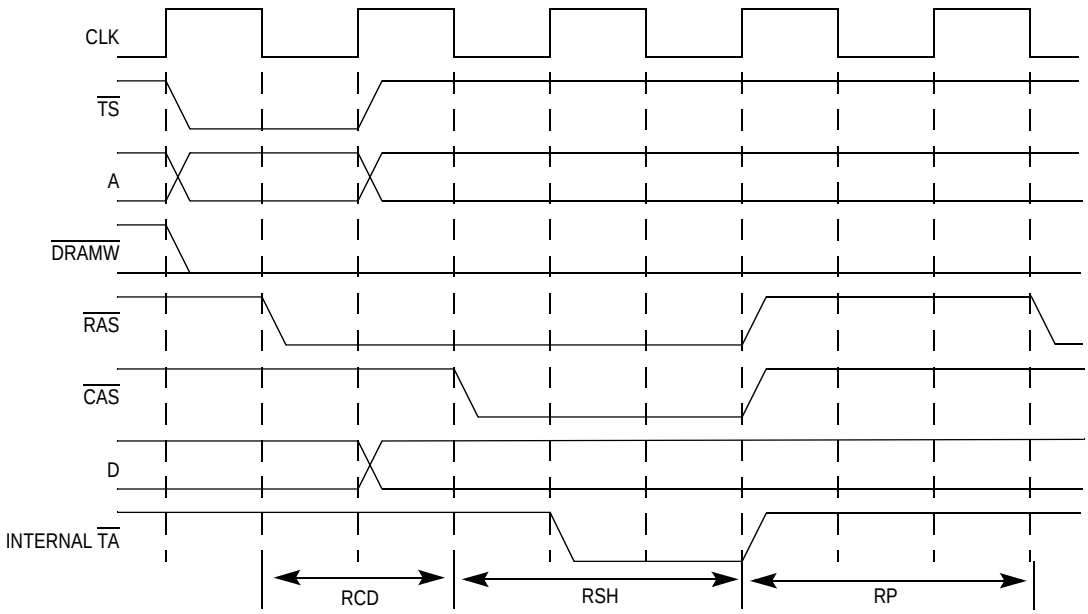


Figure 11-17. Normal Mode DRAM Transfer Timing

address bits as $0. In order for a bank to be accessible to an external master, the address bits that are unavailable to the external master must either be set to 0 in the DCAR or be masked in the DCMR.

11.4.2.4 DRAM CONTROLLER MASK REGISTER (DCMR0 - DCMR1). Each DCMR holds the address mask for each of the DRAM banks as well the definition of which types of transfers are allowed for the DRAM banks. Each DCMR is a 32-bit read/write control register. All bits in DCMR0 - DCMR1 are unaffected by either Master Reset or normal reset.

DRAM Controller Mask Register(DCMR)

Address MBAR + $50 (Bank 0)
Address MBAR + $5C (Bank 1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BAM31	BAM30	BAM29	BAM28	BAM27	BAM26	BAM25	BAM24	BAM23	BAM22	BAM21	BAM20	BAM19	BAM18	BAM17	-
NORMAL OR MASTER RESET:															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	SC	SD	UC	UD	-
NORMAL OR MASTER RESET:															
0	0	0	0	0	0	0	0	0	0	0	-	-	-	-	0

BAM [31:17] - Base Address Mask

This field defines the DRAM address space through the use of address mask bits. Any bit set to 1 masks the corresponding base address register (DCAR) bit (the base address bit becomes a ‘‘don’t care’’ in the address comparison). Unmasked base address bits are compared to the ColdFire core or external master transfer address to determine if the transfer is accessing a DRAM address space.

0 = Corresponding address bit is used in DRAM bank decode
1 = Corresponding address bit is a ‘‘don’t care’’ in DRAM bank decode

SC, SD, UC, UD - Supervisor Code, Supervisor Data, User Code, User Data Transfer Mask

This field masks allows specific types of transfers to be inhibited from accessing the DRAM bank. If a transfer mask bit is cleared, a transfer of that type can access the corresponding DRAM bank. If a transfer mask bit is set to 1, an transfer of that type can not access the corresponding DRAM bank. The transfer mask bits are:

SC = Supervisor Code mask
SD = Supervisor Data mask
UC = User Code mask
UD = User Data mask

NOTE

The UIMR does not mask reading of the UISR. True status is provided regardless of the contents of UIMR. A UART module reset clears the contents of UISR.

UISR MBAR + $194

7	6	5	4	3	2	1	0
COS	—	—	—	—	DB	RXRDY	TXRDY
RESET:							
0	0	0	0	0	0	0	0
READ ONLY					SUPERVISOR OR USER		

COS — Change-of-State

1 = A change-of-state has occurred at the $\overline{\text{CTS}}$ input and has been selected to cause an interrupt by programming bit 0 of the UACR.
0 = COS bit in the UIPCR is not selected.

DB — Delta Break

1 = The receiver has detected the beginning or end of a received break.
0 = No new break-change condition to report. Refer to **Section 12.4.1.5 Command Register (UCR)** for more information on the reset break-change interrupt command.

RxRDY — Receiver Ready or FIFO Full

UMR1 bit 6 programs the function of this bit. It is a duplicate of either the FFULL or RxRDY bit of USR.

TxRDY — Transmitter Ready

This bit is the duplication of the TxRDY bit in USR.

1 = The transmitter holding register is empty and ready to be loaded with a character.
0 = The CPU loads the transmitter-holding register or the transmitter is disabled. Characters loaded into the transmitter-holding register when TxRDY=0 are not transmitted.

12.4.1.11 INTERRUPT MASK REGISTER (UIMR). The UIMR selects the corresponding bits in the UISR that cause an interrupt. By setting the bit, the interrupt is enabled. If one of the bits in the UISR is set and the corresponding bit in the UIMR is also set, the internal interrupt output is asserted. If the corresponding bit in the UIMR is zero,

14.4.1.5 TIMER EVENT REGISTER (TER). The TER is an 8-bit register that reports events the timer recognizes. When the timer recognizes an event, it sets the appropriate bit in the TER, regardless of the corresponding interrupt-enable bits (ORI and CE) in the TMR.

TER appears as a memory-mapped register and can be read at any time.

You should write a one to a bit to clear it (writing a zero does not affect bit value); more than one bit can be cleared at a time. The REF and CAP bits must be cleared before the timer will negate the IRQ to the interrupt controller. Reset clears this register.

Timer Event Register (TER) Address MBAR+$111,MBAR+$131

	7	6	5	4	3	2	1	0
	RESERVED READ AS 0						REF	CAP
RESET	0	0	0	0	0	0	0	0

Read/Write Supervisor or User Mode

Bits 7–2 — Reserved for future use.

These bits are currently 0 when read.

CAP — Capture Event

If a one is read from this bit, the counter value has been latched into the TCR. The CE bit in the TMR enables the interrupt request caused by this event. You should write a one to this bit to clear the event condition.

REF — Output Reference Event

If a one is read from this bit, the counter has reached the TRR value. The ORI bit in the TMR enables the interrupt request caused by this event. You should write a one to this bit to clear the event condition.

Example code: Timer Initialization

There are two timers on the MCF5206e. With a 54MHZ clock, the maximum period is 5 seconds and a resolution of 18.5 ns. They can be free running or count to a value and reset. The following examples set up the timers:

Timer 1 will count to $AFAF, toggle its output, and reset back to $0000. This will continue infinitely until the timer is disabled or a reset occurs. No interrupts are set. Prescale is set at 256 and the system clock is divided by 16, therefore resolution is (16*(256))/25MHz = 163.84us. Timeout period is (16*256*44976)/25mhz = 7.369s. ($0 - $AFAF = 44976 decimal)

Timer 2 will be free-running and send out a logic pulse every time it compares the count value in the TRR register. value, which for now, is randomly chosen as $1234. Prescale is set at 127 with the sys_clock initially divided by 16 (by setting bits 2&1 of the TMR register to 10 therefore, resolution is (16*(127))/25mhz = 81.28us. Interrupts are NOT enabled.

NOTE

The timers were initialized in the SIM to have interrupt values. The examples below have the interrupts disabled. The initialization in the SIM configuration was for reference. The Timers CANNOT provide interrupt vectors, only autovectors.

Autovectors and ICRs have been set up as follows. The interrupt levels and priorities were chosen by random for demonstrative purposes. You should define the interrupt level and priorities for your specific application.

SIMR register

The SIMR is set up as follows:

1)Disable watchdog when FREEZE is asserted (bit 7)

2)Disable bus monitor when FREEZE is asserted (bit 6)

3)5206 will negate the /BD signal

```
move.b  #%11000000,D0   ;set up the SIMR (pg 7-9)
move.b  D0,SIMR;
```

NOTE*

The timer & MBUS peripherals cannot provide interrupt vectors. Timer & MBUS peripherals are only autovectored. Interrupt values were chosen randomly for demonstrative purposes. You should change these for your own application needs.

```
move.b  #%10000100,D0 ;set up Timer 1 Interrupt
move.b  D0,ICR9   ;Level 2 interrupt, Priority 0,
                   ;Autovector=ON,
  ;avect 24+1=25

move.b  #%10001001,D0 ;set up Timer 2 Interrupt
move.b  D0,ICR10          ;Level 2 interrupt, Priority 1,
  ;Autovector=ON,avect 24+2=26,

move.b  #%10001010,D0 ;set up MBUS Interrupt
move.b  D0,ICR11          ;Level 2 interrupt, Priority 2,
  ;Autovector=On,AVECT 24+3 = 27

move.b  #%00011011,D0 ;set up UART1 Interrupt
move.b  D0,ICR12          ;Level 6 interrupt, Priority 3,
  ;Autovector=Off

move.b  #%00001001,D0 ;set up UART2 Interrupt
move.b  D0,ICR13          ;Level 1 interrupt, Priority 1,
  ;Autovector=Off
```

SECTION 15
DEBUG SUPPORT

This section details the hardware debug support functions within the ColdFire® 5200 Family of processors.

The general topic of debug support is divided into three separate areas:

1. Real-Time Trace Support
2. Background Debug Mode (BDM)
3. Real-Time Debug Support

Each of the three areas is addressed in detail in the following subsections.

The logic required to support these three areas is contained in a debug module, which is shown in the system block diagram in Figure 15-1.

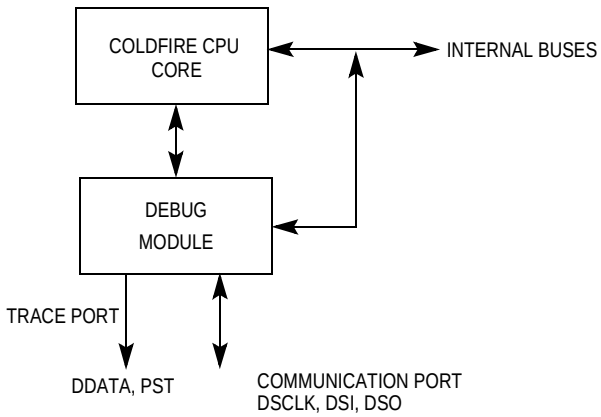


Figure 15-1. Processor/Debug Module Interface

15.1 REAL-TIME TRACE

In the area of debug functions, one fundamental requirement is support for real-time trace functionality (i.e., definition of the dynamic execution path). The ColdFire Family solution is to include a parallel output port providing encoded processor status and data to an external development system. This port is partitioned into two 4-bit nibbles: one nibble allows the processor to transmit information concerning the execution status of the core (processor status, PST[3:0]), while the other nibble allows data to be displayed (debug data, DDATA[3:0]).

15.2.2 BDM Serial Interface

Once the CPU is halted and the halt status reflected on the PST outputs (PST[3:0]=$F), the development system can send unrestricted commands to the Debug module. The Debug module implements a synchronous protocol using a three-pin interface: development serial clock (DSCLK), development serial input (DSI), and development serial output (DSO). The development system serves as the serial communication channel master and is responsible for generation of the clock (DSCLK). The operating range of the serial channel is DC to one-half of the processor frequency. The channel uses a full duplex mode, where data is transmitted and received simultaneously by both master and slave devices.

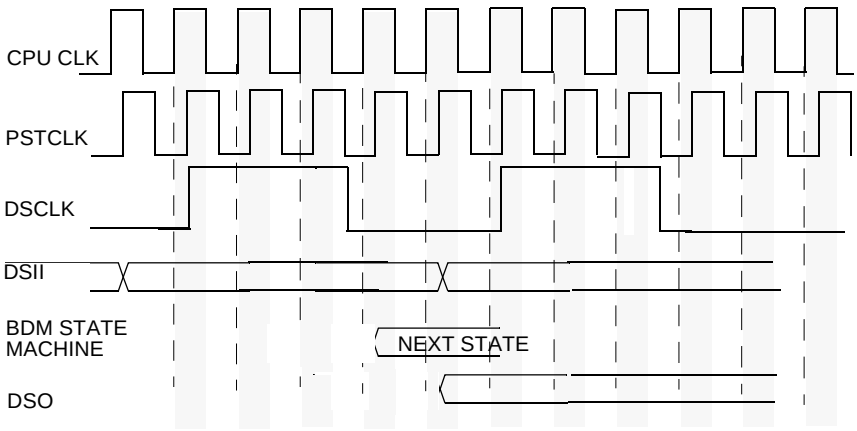


Figure 15-3. DBM Serial Transfer

Both DSCLK and DSI are synchronous inputs and must meet input setup and hold times with respect to CLK. DSCLK essentially acts as a pseudo “clock enable” and is sampled on the rising edge of CLK. If the setup time of DSCLK is met, then the internal logic transitions on the rising edge of CLK, and DSI is sampled on the same CLK rising edge. The DSO output is specified as a delay from the DSCLK-enabled CLK rising edge. All events in the