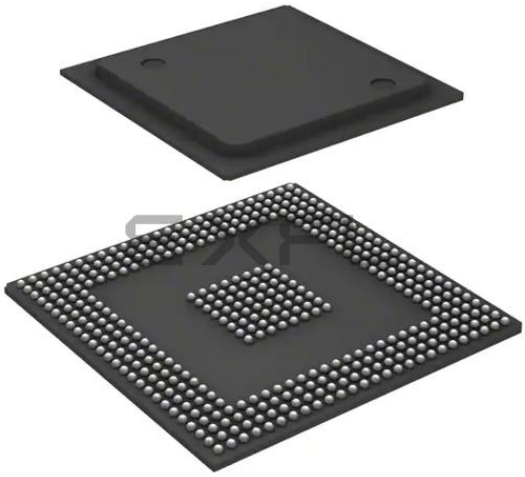
Infineon Technologies - TC1793F512F270EBABKXUMA1 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	270MHz
Connectivity	ASC, CANbus, EBI/EMI, FlexRay, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	221
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	192K x 8
RAM Size	288K x 8
Voltage - Supply (Vcc/Vdd)	1.17V ~ 3.63V
Data Converters	A/D 8x10b, 44x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BGA
Supplier Device Package	PG-BGA-416
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1793f512f270ebabkxuma1

Table of Contents

1 Summary of Features 1-1

2 System Overview of the TC1793 2-10
2.1 Block Diagram 2-11

3 Pinning 3-14
3.1 TC1793 Pin Configuration 3-15

4 Identification Registers 4-88

5 Electrical Parameters 5-90
5.1 General Parameters 5-90
5.1.1 Parameter Interpretation 5-90
5.1.2 Pad Driver and Pad Classes Summary 5-91
5.1.3 Absolute Maximum Ratings 5-92
5.1.4 Pin Reliability in Overload 5-94
5.1.5 Operating Conditions 5-96
5.1.5.1 Extended Range Operating Conditions 5-100
5.2 DC Parameters 5-103
5.2.1 Input/Output Pins 5-103
5.2.2 Analog to Digital Converters (ADCx) 5-121
5.2.3 Fast Analog to Digital Converter (FADC) 5-126
5.2.4 Oscillator Pins 5-130
5.2.5 Temperature Sensor 5-131
5.2.6 Power Supply Current 5-132
5.2.6.1 Calculating the 1.3 V Current Consumption 5-135
5.3 AC Parameters 5-137
5.3.1 Testing Waveforms 5-137
5.3.2 Power Sequencing 5-138
5.3.3 Power, Pad and Reset Timing 5-140
5.3.4 Phase Locked Loop (PLL) 5-142
5.3.5 ERAY Phase Locked Loop (ERAY_PLL) 5-145
5.3.6 JTAG Interface Timing 5-146
5.3.7 DAP Interface Timing 5-148
5.3.8 Micro Link Interface (MLI) Timing 5-149
5.3.9 Micro Second Channel (MSC) Interface Timing 5-152
5.3.10 SSC Master/Slave Mode Timing 5-154
5.3.11 ERAY Interface Timing 5-157
5.3.12 EBU Timings 5-159
5.3.12.1 BFCLKO Output Clock Timing 5-159
5.3.12.2 EBU Asynchronous Timings 5-159
5.3.12.3 EBU Burst Mode Access Timing 5-168

  - 128 Kbyte Data Scratch-Pad RAM (DSPR)
  - 16 Kbyte Instruction Cache (ICACHE)
  - 32 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 16 Kbyte Data Cache (DACHE)
  - 128 Kbyte Memory (SRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- 8-Channel Safe DMA (SDMA) Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Cross Bar Interconnect between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (SFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Four High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - Four SSC Guardian (SSCG) modules, one for each SSC
  - Two serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - Two High-Speed Micro Link interfaces (MLI) for serial inter-processor communication
  - One External Bus Interface (EBU) supporting different memories: asynchronous memories e.g. SRAM, peripheral devices; synchronous devices e.g. burst NOR flash, PSRAM; and DDR NOR flash e.g. LPDDR-NVM (Jedec 42.2), ONFI 2.0 (limited frequency at 1.8 V I/O supply)
  - One MultiCAN Module with 4 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - Two Capture / Compare 6 modules
  - Two General Purpose 12 Timer Units (GPT120 and GPT121)
- 44 analog input lines for ADC
  - 4 independent kernels (ADC0, ADC1, and ADC2)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of f_{FADC} clock

Table 2 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
Port 0				
A9	P0.0	I/O	A1+/ PU	**Port 0 General Purpose I/O Line 0**
	HWCFG0	I		**Hardware Configuration Input 0**
	OUT56	O1		**OUT56 Line of GPTA0**
	OUT56	O2		**OUT56 Line of GPTA1**
	OUT80	O3		**OUT80 Line of LTCA2**
A8	P0.1	I/O	A1/ PU	**Port 0 General Purpose I/O Line 1**
	HWCFG1	I		**Hardware Configuration Input 1**
	OUT57	O1		**OUT57 Line of GPTA0**
	OUT57	O2		**OUT57 Line of GPTA1**
	OUT81	O3		**OUT81 Line of LTCA2**
A7	P0.2	I/O	A2/ PU	**Port 0 General Purpose I/O Line 2**
	HWCFG2	I		**Hardware Configuration Input 2**
	OUT58	O1		**OUT58 Line of GPTA0**
	OUT58	O2		**OUT58 Line of GPTA1**
	OUT82	O3		**OUT82 Line of LTCA2**
B8	P0.3	I/O	A1/ PU	**Port 0 General Purpose I/O Line 3**
	HWCFG3	I		**Hardware Configuration Input 3**
	OUT59	O1		**OUT59 Line of GPTA0**
	OUT59	O2		**OUT59 Line of GPTA1**
	OUT83	O3		**OUT83 Line of LTCA2**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
E4	P6.9	I/O	A2/ PU	**Port 6 General Purpose I/O Line 9**
	TXDCAN0	O1		**CAN Node 0 Transmitter Output**
	TXD0	O2		**ASC0 Transmitter Output B**
	T60FL	O3		**GPT120**
F2	P6.10	I/O	A2/ PU	**Port 6 General Purpose I/O Line 10**
	RXDCAN1	I		**CAN Node 1 Receiver Input 0** **CAN Node 0 Receiver Input 1**
	RXD1B	I		**ASC1 Receiver Input/Output B**
	Reserved	O1		**-**
	RXD1B	O2		**ASC1 Receiver Input/Output B**
	TXENA	O3		**E-Ray Channel A transmit Data Output enable** [2]
E2	P6.11	I/O	A2/ PU	**Port 6 General Purpose I/O Line 11**
	TXDCAN1	O1		**CAN Node 1 Transmitter Output**
	TXD1	O2		**ASC1 Transmitter Output B**
	TXENB	O3		**E-Ray Channel B transmit Data Output enable** [2]
E1	P6.12	I/O	A1/ PU	**Port 6 General Purpose I/O Line 12**
	RXDCAN2	I		**CAN Node 2 Receiver Input 0** **CAN Node 1 Receiver Input 1**
	RXDA1	I		**E-Ray Channel A Receive Data Input 1** [2]
	Reserved	O1		**-**
	Reserved	O2		**-**
	COUT61	O3		**CCU60**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
T2	P7.5	I/O	A1+/ PU	**Port 7 General Purpose I/O Line 5**
	REQ7	I		**External trigger Input 7**
	AD2EMUX1	O1		**ADC2 external multiplexer Control Output 1**
	SLSO32	O2		**SSC3 Output**
	Reserved	O3		**-**
T1	P7.6	I/O	A1+/ PU	**Port 7 General Purpose I/O Line 6**
	AD1EMUX0	O1		**ADC1 external multiplexer Control Output 0**
	SLSO33	O2		**SSC3 Output**
	Reserved	O3		**-**
U2	P7.7	I/O	A1+/ PU	**Port 7 General Purpose I/O Line 7**
	AD1EMUX1	O1		**ADC1 external multiplexer Control Output 1**
	SLSO34	O2		**SSC3 Output**
	Reserved	O3		**-**
Port 8				
H2	P8.0	I/O	A2/ PU	**Port 8 General Purpose I/O Line 0**
	IN40	I		**IN40 Line of GPTA0**
	IN40	I		**IN40 Line of GPTA1**
	SENT0	I		**SENT Digital Input**
	OUT40	O1		**OUT40 Line of GPTA0**
	COUT62	O2		**CCU61**
	TCLK1	O3		**MLI1 transmit Channel Clock Output**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
K2	P8.5	I/O	A2/ PU	**Port 8 General Purpose I/O Line 5**
	IN45	I		**IN45 Line of GPTA0**
	IN45	I		**IN45 Line of GPTA1**
	SENT5	I		**SENT Digital Input**
	CTRAPA	I		**CCU60**
	CTRAPB	I		**CCU62**
	CC60INC	I		**CCU60**
	T12HRE	I		**CCU61**
	CC61INC	I		**CCU61**
	OUT45	O1		**OUT45 Line of GPTA0**
	OUT45	O2		**OUT45 Line of GPTA1**
	RREADY1A	O3		**MLI1 Receive Channel ready Output A**
K3	P8.6	I/O	A1/ PU	**Port 8 General Purpose I/O Line 6**
	IN46	I		**IN46 Line of GPTA0**
	IN46	I		**IN46 Line of GPTA1**
	RVALID1A	I		**MLI1 Receive Channel valid Input A**
	SENT6	I		**SENT Digital Input**
	OUT46	O1		**OUT46 Line of GPTA0**
	COUT60	O2		**CCU61**
	T6OUT	O3		**GPT120**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
A21	P9.9	I/O	A1/ PU	**Port 9 General Purpose I/O Line 9**
	SENT0	I		**SENT Digital Input**
	Reserved	O1		**-**
	SENT0	O2		**SENT Digital Output**
	Reserved	O3		**-**
B21	P9.10	I/O	A1/ PU	**Port 9 General Purpose I/O Line 10**
	EMGSTOP	I		**Emergency Stop**
	SENT7	I		**SENT Digital Input**
	COUT63	O1		**CCU63**
	SENT7	O2		**SENT Digital Output**
	Reserved	O3		**-**
C21	P9.11	I/O	A1/ PU	**Port 9 General Purpose I/O Line 11**
	SENT2	I		**SENT Digital Input**
	Reserved	O1		**-**
	SENT2	O2		**SENT Digital Output**
	Reserved	O3		**-**
D21	P9.12	I/O	A1/ PU	**Port 9 General Purpose I/O Line 12**
	SENT5	I		**SENT Digital Input**
	Reserved	O1		**-**
	SENT5	O2		**SENT Digital Output**
	Reserved	O3		**-**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
V25	P13.8	I/O	B/ PU	**Port 13 General Purpose I/O Line 8**
	AD8	I		**EBU Address/Data Bus Line 8**
	OUT96	O1		**OUT96 Line of GPTA0**
	OUT96	O2		**OUT96 Line of GPTA1**
	OUT88	O3		**OUT88 Line of LTCA2**
	AD8	O		**EBU Address/Data Bus Line 8**
U24	P13.9	I/O	B/ PU	**Port 13 General Purpose I/O Line 9**
	AD9	I		**EBU Address/Data Bus Line 9**
	OUT97	O1		**OUT97 Line of GPTA0**
	OUT97	O2		**OUT97 Line of GPTA1**
	OUT89	O3		**OUT89 Line of LTCA2**
	AD9	O		**EBU Address/Data Bus Line 9**
Y26	P13.10	I/O	B/ PU	**Port 13 General Purpose I/O Line 10**
	AD10	I		**EBU Address/Data Bus Line 10**
	OUT98	O1		**OUT98 Line of GPTA0**
	OUT98	O2		**OUT98 Line of GPTA1**
	OUT90	O3		**OUT90 Line of LTCA2**
	AD10	O		**EBU Address/Data Bus Line 10**
AA26	P13.11	I/O	B/ PU	**Port 13 General Purpose I/O Line 11**
	AD11	I		**EBU Address/Data Bus Line 11**
	OUT99	O1		**OUT99 Line of GPTA0**
	OUT99	O2		**OUT99 Line of GPTA1**
	OUT91	O3		**OUT91 Line of LTCA2**
	AD11	O		**EBU Address/Data Bus Line 11**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AD24	P14.15	I/O	B/ PU	**Port 14 General Purpose I/O Line 15**
	AD31	I		**EBU Address/Data Bus Line 31**
	T3EUDC	I		**GPT120**
	T3EUDD	I		**GPT121**
	OUT111	O1		**OUT111 Line of GPTA0**
	OUT111	O2		**OUT111 Line of GPTA1**
	OUT111	O3		**OUT111 Line of LTCA2**
	AD31	O		**EBU Address/Data Bus Line 31**
Port 15				
AE21	P15.0	I/O	B/ PU	**Port 15 General Purpose I/O Line 0**
	T4INC	I		**GPT120**
	T4IND	I		**GPT121**
	CCPOS2B	I		**CCU60**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	CS0	O		**Chip Select Output Line 0**
AD21	P15.1	I/O	B/ PU	**Port 15 General Purpose I/O Line 1**
	T4EUDC	I		**GPT120**
	T4EUDD	I		**GPT121**
	CCPOS2B	I		**CCU61**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	CS1	O		**Chip Select Output Line 1**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AC2	AN4	I	D	**Analog Input 4: ADC0.CH4, ADC2.CH12** [5]
AA3	AN5	I	D	**Analog Input 5: ADC0.CH5, ADC2.CH13** [5]
AD1	AN6	I	D	**Analog Input 6: ADC0.CH6, ADC2.CH14** [5]
AB4	AN7	I	D	**Analog Input 7: ADC0.CH7, ADC2.CH15** [5]
AC1	AN8	I	D / S	**Analog Input 8: ADC0.CH8, SENT0** [5]
AB2	AN9	I	D / S	**Analog Input 9: ADC0.CH9, SENT1** [5]
Y3	AN10	I	D / S	**Analog Input 10: ADC0.CH10, SENT2** [5]
AA2	AN11	I	D / S	**Analog Input 11: ADC0.CH11, SENT3** [5]
AB1	AN12	I	D / S	**Analog Input 12: ADC0.CH12, SENT4** [5]
W3	AN13	I	D / S	**Analog Input 13: ADC0.CH13, SENT5** [5]
Y2	AN14	I	D / S	**Analog Input 14: ADC0.CH14, SENT6** [5]
AA1	AN15	I	D / S	**Analog Input 15: ADC0.CH15, SENT7** [5]
V4	AN16	I	D	**Analog Input 16: ADC1.CH0** [5]
W2	AN17	I	D	**Analog Input 17: ADC1.CH1** [5]
Y1	AN18	I	D	**Analog Input 18: ADC1.CH2** [5]
V3	AN19	I	D	**Analog Input 19: ADC1.CH3** [5]
W1	AN20	I	D	**Analog Input 20: ADC1.CH4** [5]
V2	AN21	I	D	**Analog Input 21: ADC1.CH5** [5]
V1	AN22	I	D	**Analog Input 22: ADC1.CH6** [5]
U1	AN23	I	D	**Analog Input 23: ADC1.CH7** [5]
AC8	AN24	I	D	**Analog Input 24: ADC1.CH8, FADC_FADIN0P** [6]
AD8	AN25	I	D	**Analog Input 25: ADC1.CH9, FADC_FADIN0N** [6]
AC7	AN26	I	D	**Analog Input 26: ADC1.CH10, FADC_FADIN1P** [6]

5.1.2 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the **Section 5.2.1**.

Table 8 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub Class	Speed Grade [1]	Load [1]	Leakage 150oC [1]	Termination
A	3.3 V	LVTTL I/O, LVTTL outputs	**A1** (e.g. GPIO)	6 MHz	100 pF	500 nA	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	1 µA	Series termination recommended
			A2 (e.g. serial I/Os)	40 MHz	50 pF	3 µA	Series termination recommended
B	3.3 V [2]	LVTTL I/O		75 MHz	35 pF	6 µA	Series termination recommended
	2.5 V [2]			75 MHz	35 pF		
F	3.3 V	LVDS	–	50 MHz	–	–	Parallel termination, 100 Ω ± 10% [3]
		CMOS	–	6 MHz	50 pF	–	
DE	5 V	ADC	–	–	–	–	
I	3.3 V	LVTTL (input only)	–	–	–	–	

1) These values show typical application configurations for the pad. Complete and detailed pad parameters are available in the individual pad parameter table on the following pages.

2) Supplied via V_{DDEBU}.

3) In applications where the LVDS pins are not used (disabled), these pins must be either left unconnected, or properly terminated with the differential parallel termination of 100 Ω ± 10%.

1) The port groups are defined in **Table 14**.

Table 13 Operating Conditions Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Modulated f_{CPU}	$f_{CPU\_modulated}$ SR	–	–	270	MHz	SAK-TC1793F-512F 270EB; SAK-TC1793F-512F 270EF; SAK-TC1793N-512F 270EF; SAK-TC1793S-512F 270EF
		–	–	200	MHz	SAK-TC1793F-512F 200EF SAK-TC1793F-512F 200EB
FPI bus frequency	f_{FPI} SR	–	–	100	MHz	
Modulated f_{FPI}	$f_{FPI\_modulated}$ SR	–	–	100-2*MA[1)]	MHz	MA = modulation amplitude
FSI frequency	f_{FSI} SR	–	–	150	MHz	
Modulated f_{FSI}	$f_{FSI\_modulated}$ SR	–	–	150-2*MA[1)]	MHz	MA = modulation amplitude
PCP Frequency	f_{PCP} SR	–	–	200	MHz	
Modulated f_{PCP}	$f_{PCP\_modulated}$ SR	–	–	200-2*MA[1)]	MHz	MA = modulation amplitude
SRI Frequency	f_{SRI} SR	–	–	270	MHz	SAK-TC1793F-512F 270EB; SAK-TC1793F-512F 270EF; SAK-TC1793N-512F 270EF; SAK-TC1793S-512F 270EF
		–	–	200	MHz	SAK-TC1793F-512F 200EF SAK-TC1793F-512F 200EB

Table 13 Operating Conditions Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ADC analog supply voltage	V_{DDM} SR	2.97	5	5.5[4)]	V	
Oscillator core supply voltage	V_{DDOSC} SR	1.17	1.3	1.43[3)]	V	for duration limitation see **Section 5.1.5.1**
Oscillator 3.3V supply voltage	V_{DDOSC3} SR	2.97	3.3	3.63[5)]	V	for duration limitation see **Section 5.1.5.1**
Digital supply voltage for IO pads	V_{DDP} SR	2.97	3.3	3.63 [5)]	V	for duration limitation see **Section 5.1.5.1**
E-Ray PLL core voltage supply	V_{DDPF} SR	1.17	1.3	1.43[3)]	V	for duration limitation see **Section 5.1.5.1**
E-Ray PLL 3.3V supply	V_{DDPF3} SR	2.97	3.3	3.63[5)]	V	for duration limitation see **Section 5.1.5.1**
VDDP voltage to ensure defined pad states[6)]	V_{DDPPA} CC	0.65	–	–	V	
Digital ground voltage	V_{SS} SR	0	–	–	V	
Analog ground voltage for V_{DDM}	V_{SSM} SR	-0.1	0	0.1	V	
Analog core supply	V_{DDAF} SR	1.17	1.3	1.43[3)]	V	for duration limitation see **Section 5.1.5.1**
FADC / ADC analog supply voltage	V_{DDMF} SR	2.97	3.3	3.63[5)]	V	for duration limitation see **Section 5.1.5.1**
Analog ground voltage for V_{DDMF}	V_{SSAF} SR	-0.1	0	0.1	V	

1) MA equals the modulation amplitude in percentage times the configured PLL clock out frequency.

2) Applicable for digital outputs.

3) Voltage overshoot to 1.7V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

Table 18 Standard_Pads Class_A2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis for A2 pads [1]	$HYSA2$ CC	0.1 x V_{DDP}	–	–	V	
Input Leakage current Class A2	I_{OZA2} CC	-6000	–	6000	nA	$V_i < V_{DDP}$ / 2 - 1 V; $V_i > V_{DDP}$ / 2 + 1 V; $V_i \geq 0$ V; $V_i \leq V_{DDP}$ V
		-3000	–	3000	nA	$V_i > V_{DDP}$ / 2 - 1 V; $V_i < V_{DDP}$ / 2 + 1 V
Ratio Vil/Vih, A2 pads	V_{ILA2} / V_{IHA2} CC	0.6	–	–		
On-Resistance of the class A2 pad, weak driver	R_{DSONW} CC	–	450	600	Ohm	$I_{OH} > -0.5$ mA; P_MOS
		–	210	340	Ohm	$I_{OL} < 0.5$ mA; N_MOS
On-Resistance of the class A2 pad, medium driver	R_{DSONM} CC	–	–	155	Ohm	$I_{OH} > -2$ mA; P_MOS
		–	–	110	Ohm	$I_{OL} < 2$ mA; N_MOS
On-Resistance of the class A2 pad, strong driver	R_{DSON2} CC	–	–	28	Ohm	$I_{OH} > -2$ mA; P_MOS
		–	–	22	Ohm	$I_{OL} < 2$ mA; N_MOS

Table 29 Power Supply Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum power dissipation	PD CC	–	–	1633	mW	power pattern= max; fCPU=270 MHz
		–	–	1488	mW	power pattern= realistic; fCPU=270 MHz
		–	–	1523	mW	power pattern= max; fCPU=200 MHz
		–	–	1403	mW	power pattern= realistic; fCPU=200 MHz

1) Infineon Power Loop: CPU and PCP running, all peripherals active. The power consumption of each customer application will most probably be lower than this value, but must be evaluated seperately.
2) This current includes the E-Ray module power consumption, including the PCP operation component.
3) The I_{DD} decreases typically by 97 mA if the f_{CPU} decreases by 50MHz, at constant T_J
4) The I_{DD} decreases typically by 105 mA if the f_{CPU} decreases by 50MHz, at constant T_J
5) D-Flash read, write, or erase opoeration in parallel to P-Flash operations name in Test Condition is covered already in the give current limits.
6) Relevant for the power supply dimensioning, not for thermal considerations.
7) In case of erase of Program Flash PFx, internal flash array loading effects may generate transient current spikes of up to 15 mA for maximum 5 ms per flash module.
8) For power supply dimensioning of V_{DDP} 30 mA have to added for flash programming case.

Note: In general current consumption for operations with data flash are always lower than the defined values for program flash read operation.

5.2.6.1 Calculating the 1.3 V Current Consumption

The current consumption of the 1.3 V rail compose out of two parts:

- Static current consumption
- Dynamic current consumption

The static current consumption is related to the device temperature T_J and the dynamic current consumption depends of the configured clocking frequencies and the software

application executed. These two parts needs to be added in order to get the rail current consumption.

(2)

$$I_0 = 3,75\left[\frac{mA}{C}\right] \times e^{0,02041 \times T_J[C]}$$

(3)

$$I_0 = 18,77\left[\frac{mA}{C}\right] \times e^{0,01825 \times T_J[C]}$$

Function 2 defines the typical static current consumption and Function 3 defines the maximum static current consumption. Both functions are valid for V_{DD} = 1.326 V.

For the dynamic current consumption using the real pattern and f_{SRI} = 3 / 2 * f_{PCP} = 3 * f_{FPI} the function 4 applies:

(4)

$$I_{Dym} = 1,22\left[\frac{mA}{MHz}\right] \times f_{CPU}[MHz]$$

For the dynamic current consumption using the real pattern and f_{SRI} = f_{PCP} = 2 * f_{FPI} the function 5 applies:

(5)

$$I_{Dym} = 1,305\left[\frac{mA}{MHz}\right] \times f_{CPU}[MHz]$$

and this finally results in

(6)

$$I_{DD} = I_0 + I_{DYM}$$

5.3.7 DAP Interface Timing

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 34 DAP Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period[1]	t_{TCK} SR	12.5	–	–	ns	
DAP0 high time	t_{12} SR	4	–	–	ns	
DAP0 low time[1]	t_{13} SR	4	–	–	ns	
DAP0 clock rise time	t_{14} SR	–	–	2	ns	
DAP0 clock fall time	t_{15} SR	–	–	2	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6.0	–	–	ns	
DAP1 hold after DAP0 rising edge	t_{17} SR	6.0	–	–	ns	
DAP1 valid per DAP0 clock period[2]	t_{19} CC	8	–	–	ns	C_L= 20 pF; f= 80 MHz
		10	–	–	ns	C_L= 50 pF; f= 40 MHz

1) See the DAP chapter for clock rate restrictions in the Active:IDLE protocol state.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

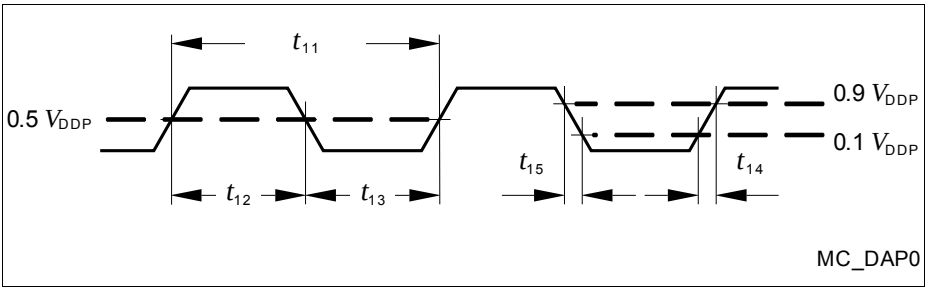


Figure 16 Test Clock Timing (DAP0)

Table 35 MLI Receiver

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RCLK clock period	t_{20} SR	1 / f_{FPI}	–	–	ns	
RCLK high time[1)2)]	t_{21} SR	–	0.5 x t_{20}	–	ns	
RCLK low time[1)2)]	t_{22} SR	–	0.5 x t_{20}	–	ns	
RCLK rise time[3)]	t_{23} SR	–	–	4	ns	
RCLK fall time[3)]	t_{24} SR	–	–	4	ns	
RDATA/RVALID setup time before RCLK falling edge	t_{25} SR	4.2	–	–	ns	
RDATA/RVALID hold time after RCLK falling edge	t_{26} SR	2.2	–	–	ns	
RREADY output delay time	t_{27} SR	0	–	16	ns	

1) The following formula is valid: t21 + t22 = t20.

2) Min and Max values for this parameter can be derived from the typ. value by considering the other receiver timing parameters.

3) The RCLK max. input rise/fall times are best case parameters for fSYS = 90 MHz. For reduction of EMI, slower input signal rise/fall times can be used for longer RCLK clock periods.

Table 36 MLI Transmitter

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCLK clock period	t_{10} CC	2 x 1 / f_{FPI}	–	–	ns	
TCLK high time[1)2)]	t_{11} CC	0.45 x t_{10}	0.5 x t_{10}	0.55 x t_{10}	ns	
TCLK low time[1)2)]	t_{12} CC	0.45 x t_{10}	0.5 x t_{10}	0.55 x t_{10}	ns	
TCLK rise time	t_{13} CC	–	–	0.3 x t_{10}[3)]	ns	
TCLK fall time	t_{14} CC	–	–	0.3 x t_{10}[3)]	ns	

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG